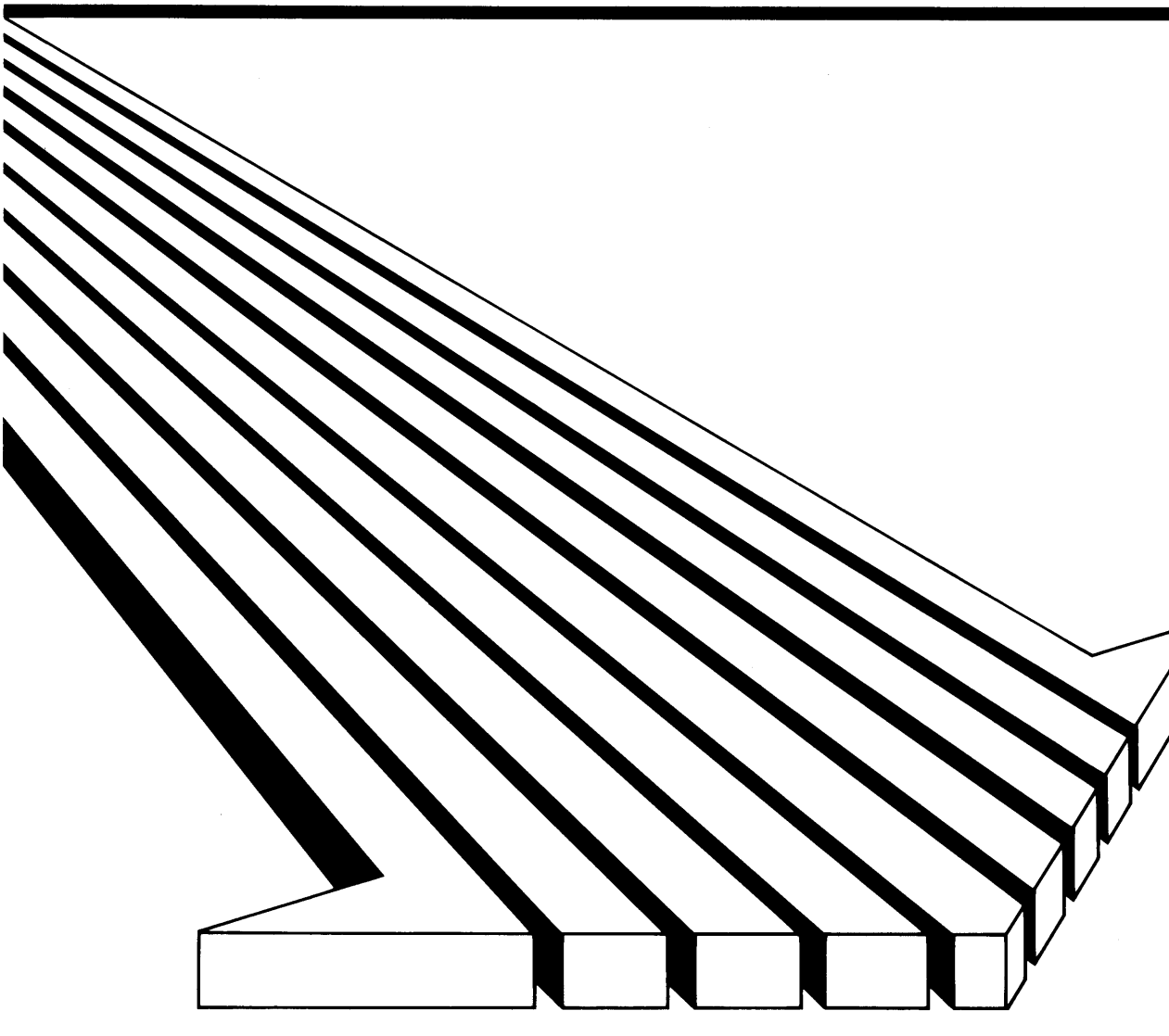
INTEL MULTIBUS® SPECIFICATION



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SECTION 1
INTRODUCTION

One of the most important elements in a computer system is the bus structure that holds all the hardware components together. This bus structure contains the necessary signals to allow the various system components to interact with each other, i.e., it allows memory and I/O data transfers, direct memory accesses, generation of interrupts, etc. This document has been written to provide a detailed description of all the Intel MULTIBUS elements and features.

The MULTIBUS interface is the flexible bus structure used to interface the family of Intel's 80/86 products which include 8- and 16-bit single board computer, memory expansion boards, digital and analog I/O boards and peripheral controllers. It supports direct addressability up to 16 megabytes through 24-bit addresses and 8- and 16-bit data transfers.

The bus structure is built upon the master-slave concept where the master device in the system takes control of the MULTIBUS interface and the slave device, upon decoding its address, acts upon the command provided by the master. This handshake between master and slave devices allows modules of different speeds to use the MULTIBUS interface and allows data rates up to five million transfers per second (bytes or words).

Another important MULTIBUS feature is the ability to connect multiple master modules for multiprocessing configurations. The MULTIBUS interface provides control signals for connecting multiple masters either in a daisy-chain priority fashion or in parallel. With this latter arrangement, up to sixteen masters may share MULTIBUS resources.

This document has been prepared for those users who intend to evaluate or design products that will be compatible with the MULTIBUS system bus structure. In addition to the detailed signal definitions, timing, electrical and mechanical specifications, this document also includes many design examples showing the reader how to implement the various control circuits associated with the MULTIBUS interface.

SECTION 2
FUNCTIONAL DESCRIPTION

2.0 INTRODUCTION

Section 2 will give the reader an overall understanding of how the MULTIBUS functions. The section contains information about the elements which connect to the bus, a description of the signals which provide the interface to the bus, and the different types of operations which are performed on the MULTIBUS interface.

In this section, as well as throughout the specification, a clear and consistent notation for signals has been used. The Memory Write Command (MWTC) will be used to explain this notation. The terms one: zero and true: false can be ambiguous, so their use will be avoided. In their place, we will use the terms electrical High and Low (H and L). A slash following the signal name (MWTC/) indicates that the signal is active low as shown:

MWTC/ = $\overline{\text{MWTC}}$ = MWTC − = Asserted at 0 volts

The signal (MWTC/) driven by a three state driver will be pulled up to Vcc when not asserted. Table 2-1 is used to further explain the notation used in this specification.

Table 2-1. Notational Summary

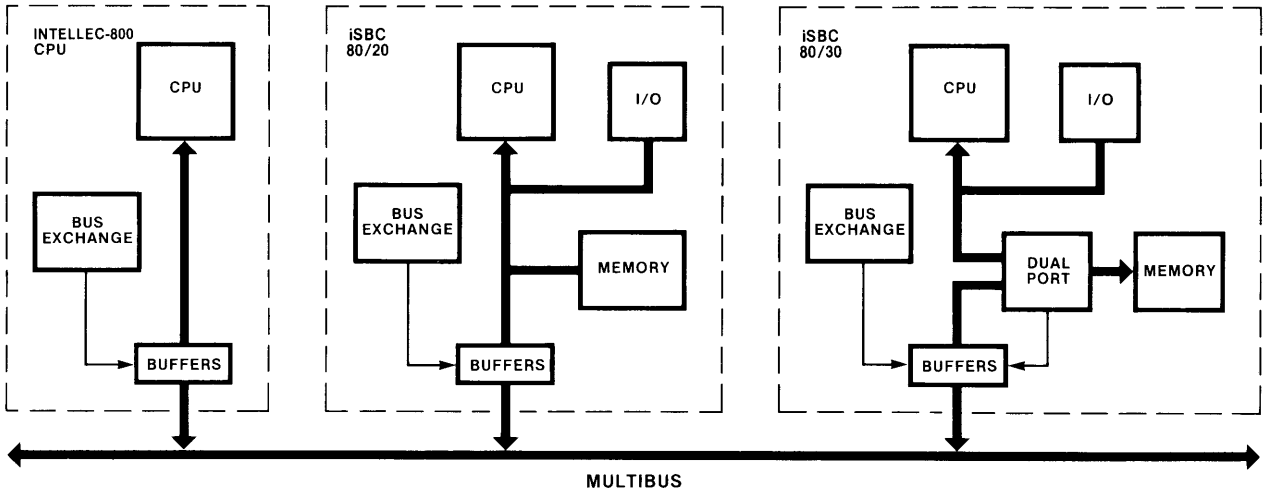
Function	Definition		
	Electrical	Logical	State
MWTC	H	1 True	Active, Asserted
	L	0 False	
MWTC/	L	1 True	Active, Asserted
	H	0 False	

2.1 MULTIBUS ELEMENTS

This section will describe the elements that interface to the bus (masters, slaves, and intelligent-slaves), and the MULTIBUS signal lines which make up this interface.

2.1.1 BUS MASTERS

A bus master is any module which has the ability to control the bus. The master exercises this control by acquiring the bus through bus exchange logic and then generating command signals, address signals, and memory addresses. There are many modules which fall into the class of bus master. The most basic type of masters, would include the INTELLEC-800 CPU Module. This module contains a processor and bus exchange logic as shown in figure 2-1. A more complex master would be the iSBC 80/20. This module contains a processor, memory,



input/output logic, and Bus Exchange logic. A complex master shown in figure 2-1, is the iSBC 80/30. This module contains a CPU, memory, input/output logic, bus exchange logic, and a next generation board architecture.

The MULTIBUS interface can support more than one master on the same system. In order to do this, there must be a means for each master to gain MULTIBUS control. This is done through bus exchange logic which will be explained in detail in Section 2.5. Figure 2-1 depicts a multi-master system, and shows some typical master configurations. This figure is for explanation purposes only.

2.1.2 BUS SLAVES

Another type of module which can use the MULTIBUS interface is the bus slave. The bus slaves decode the address lines and act upon the command signals from the bus masters. The slaves are not capable of controlling the MULTIBUS interface. Some examples of bus slaves are shown in figure 2-2.

2.1.3 INTELLIGENT SLAVE

The third type of module that can use the MULTIBUS interface is the intelligent slave. The intelligent slave has all the attributes of a slave module in that it decodes addresses and acts upon commands from master modules. However, the intelligent slave contains a micro processor which is programmed with software or firmware. The on-board processor is used to control the on-board memory and I/O and not the MULTIBUS interface. The combination of on-board processor, memory and I/O allows the intelligent slave to complete on-board operations without constant MULTIBUS access. In some cases, the intelligent slave's memory may be available to the system through on-board dual port logic.

2.1.4 MULTIBUS SIGNAL CLASSES

MULTIBUS signals can be grouped into several classes based on the functions which they perform. The classes are:

A. Control Lines
B. Address and Inhibit Lines
C. Data Lines
D. Interrupt Lines
E. Bus Exchange Lines
F. Power Failure Lines (Optional)

The following sub-sections will explain the different classes of MULTIBUS signals.

2.1.4.1 CONTROL LINES. The following signals are classified as control lines:

A. Clocks	Constant Clock (CCLK/) Bus Clock (BCLK/)
B. Commands	Memory Write (MWTC/) Memory Read (MRDC/) I/O Write (IOWC/) I/O Read (IORC/)
C. Acknowledge	Transfer Acknowledge (XACK/)
D. Initialize	INIT/
E. LOCK	LOCK/

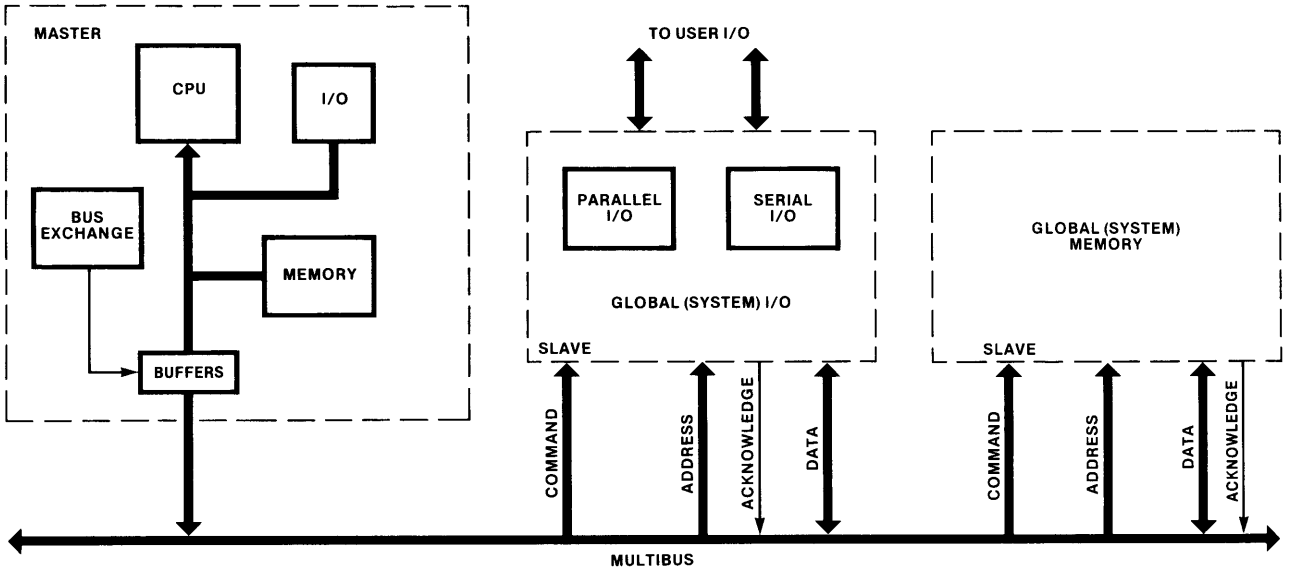


Figure 2-2. MULTIBUS Slave Examples

2.1.4.1.1 CLOCK LINES.

Bus Clock (BCLK/). - This clock signal is used to synchronize the bus contention logic. It may be slowed, stopped, or single stepped. If there is more than one master on the system, one and only one should be used to generate a master clock.

Constant Clock (CCLK/). - CCLK/ is a clock signal of constant frequency which may be used by bus masters or slaves as a master clock. If there is more than one master on the system, one and only one should be used to generate a master clock.

2.1.4.1.2 COMMAND LINES (MWTC/, MRDC/, IOWC/, IORC/). The command lines are the communication links between the bus masters and bus slaves. There are four command lines for memory and I/O reads and writes. An active command line indicates to the slave that the address lines are carrying a valid address, and that the slave should perform the specified operation.

2.1.4.1.3 TRANSFER ACKNOWLEDGE LINE (XACK/). This line is the slave's acknowledgement of the master's command. XACK/ indicates to the master that the requested action is complete, and that data has been placed on or accepted from the data lines.

2.1.4.1.4 INITIALIZE(INIT/). The INIT/ signal is generated to reset the entire system to a known internal state. This signal is usually generated prior to starting any operations on the system. INIT/ may be generated by any or all of the bus masters or by an external source such as a buffered and debounced front panel switch.

2.1.4.1.5 LOCK (LOCK/). The LOCK/ signal is generated by the master in control of the bus to indicate the bus is locked. LOCK/ is used to extend mutual exclusion to multiple-port ram designs.

2.1.4.2 ADDRESS AND INHIBIT LINES. The address and inhibit lines are made up of the following groups of signals:

A. Address Lines - ADR0/ - ADR17/ (0-9, A-F, 10-17); in Hex Notation.

B. Inhibit Lines - INH1/ and INH2/

C. Byte Control - BHEN/

2.1.4.2.1 ADDRESS LINES (24 LINES). ADR0/ - ADRF/ and ADR10/ - ADR17/ carry the address of the memory location or the I/O device that is being referenced. Twenty four address lines allow a maximum of 16 million bytes of memory to be accessed. When addressing an I/O device, sixteen address lines (ADR0/ - ADRF/) are used allowing the addressing of a maximum of 64K devices. There are various class of modules which use a subset of the address lines. These classes are defined in Section 6 of this specification. Design examples showing compatibility with various classes of modules are given in Chapter 5.

For I/O bus cycles, master modules have the option of generating 8 bit or 16 bit addresses. Because of this, all I/O slaves must be capable of being configured to decode 8 address bits (ADR0/ - ADR7/) and ignore the upper address bits or to decode all 16 bits of address (ADR0/ - ADRF/). Note that in a system using 8 bit I/O addresses, the value of the upper 16 bits of address is unknown. A master generating only 8 bit addresses may set the upper 16 address bits to any arbitrary value.

2.1.4.2.2 INHIBIT LINES. Two inhibit lines (INH1/ and INH2/) are provided on the MULTIBUS. INH1/ prevents RAM memory slave modules from responding to the memory address and command on the MULTIBUS. This effectively allows ROM memory modules or memory mapped I/O devices to override RAM memory modules when both are assigned the same memory addresses. INH2/ prevents ROM memory modules from responding to the memory address and command on the MULTIBUS. This effectively allows auxiliary ROM (e.g., a bootstrap program.) to override ROM memory modules when they both are assigned the same memory addresses.

2.1.4.2.3 BYTE CONTROL LINE. The byte control line (BHEN/) is used to select the upper byte (bits 8-F) of a 16 bit word. This signal is used only on systems that incorporate sixteen-bit memory and I/O modules.

2.1.4.3 DATA LINES (DAT0/ - DATF/). Sixteen bidirectional data lines (DAT0/ - DATF/) are used to transmit or receive information to or from a memory location or an I/O port (DAT0/ being the least significant bit). In eight bit systems, only lines DAT0/ - DAT7/ are used.

2.1.4.4 INTERRUPT LINES. The interrupt lines consist of the following signals:

A. Interrupt Requests - INT0/ - INT7/

B. Interrupt Acknowledge - INTA/

2.1.4.4.1 INTERRUPT REQUEST LINES. Interrupts are requested by activating one of the eight Interrupt Request Lines (INT0/ - INT7/). INT0/ has the highest priority and INT7/ has the lowest.

2.1.4.4.2 INTERRUPT ACKNOWLEDGE. Interrupt Acknowledge (INTA/) is generated by the bus master in response to an interrupt request to freeze interrupt status and request the placement of the interrupt vector address onto the MULTIBUS data lines.

2.1.4.5. BUS EXCHANGE LINES. The Bus Exchange lines are made up of the following signals:

A. Bus Request - BREQ/

B. Bus Priority - BPRN/, BPRO/

C. Bus Busy - BUSY/

D. Common Bus Request - CBRQ/

E. Bus Clock - BCLK/

A bus master gains control through the manipulation of these MULTIBUS signals.

2.1.4.5.1 BUS REQUEST. BREQ/ is used by the bus masters in a parallel priority resolution circuit to indicate a request for MULTIBUS control.

2.1.4.5.2 BUS PRIORITY. Bus Priority In (BPRN/) indicates to a particular master module that no higher priority module is requesting use of the MULTIBUS interface. The Bus Priority Out (BPRO/) signal is used with serial (daisy chain) bus priority resolution schemes. BPRO/ is passed to the BPRN/ input of the master with the next lower bus priority.

2.1.4.5.3 BUS BUSY. Bus Busy (BUSY/) is activated by the bus master in control, to indicate that the MULTIBUS interface is in use. This prevents other masters from gaining control of the bus.

2.1.4.5.4 COMMON BUS REQUEST. Common Bus Request (CBRQ/) is used to allow a bus master to retain control of the bus without contending for it each processor cycle, as long as no other master is requesting control of the bus. A bus master requesting control of the bus but not currently controlling it asserts CBRQ/. This causes the controlling bus master to relinquish control of the bus.

2.2 DATA TRANSFER OPERATION

The primary function of the MULTIBUS interface is to provide a path for the transfer of data between modules. The following sections will describe the different types of data transfers and the means by which they are implemented using the signals previously described in Section 2.1. Figure 2-3 can be referenced during the following discussions.

The discussion of the MULTIBUS data transfer operation will be covered in three parts: 1) an overview of the operation, 2) A detailed description of the signals used in the transfer, and 3) A discussion of the specifics pertaining to the different transfers.

It will be assumed that there is only one MULTIBUS master and therefore no MULTIBUS contention exists. The MULTIBUS Exchange logic will be discussed in a later section.

2.2.1 DATA TRANSFER OVERVIEW

A MULTIBUS data transfer is accomplished as follows. First the bus master places the memory or I/O port address on the address bus. If the operation is a write, the data would also be placed on the data bus at this time. The bus master then generates a command (I/O read or write, or memory read or write) which activates the appropriate bus slave. The slave accepts the data if it is a write operation, or places the data on the data bus if it is a read. A transfer acknowledge is then sent to the bus master by the bus slave allowing the bus master to complete its cycle, removing the command from the command line, and then removing the address and data from the MULTIBUS interface. Figures 2-4 and 2-5 show the basic timing for a read and write data transfer operation.

2.2.2 MULTIBUS SIGNAL DESCRIPTION

This section is a detailed description of the Multibus signals used for data transfer operations. It contains timing information, signal origination information, and information pertaining to the specific function that each signal performs in the data transfer operation.

2.2.2.1 INITIALIZATION (INIT/). Prior to any MULTIBUS data transfer operations, all the system modules should be reset to a known internal state. This can be accomplished by the INIT/ signal. This signal can be driven from many sources. The following are three examples:

A. A power-on clear circuit (RC network) which holds INIT/ low until the power supplies reach their specific voltage outputs.

B. A RESET button, sometimes provided on the system front panel for operator use. Note that this button must be debounced.

C. A software command which can be implemented to pull down the INIT/ line.

The INIT/ line is driven by open-collector gates.

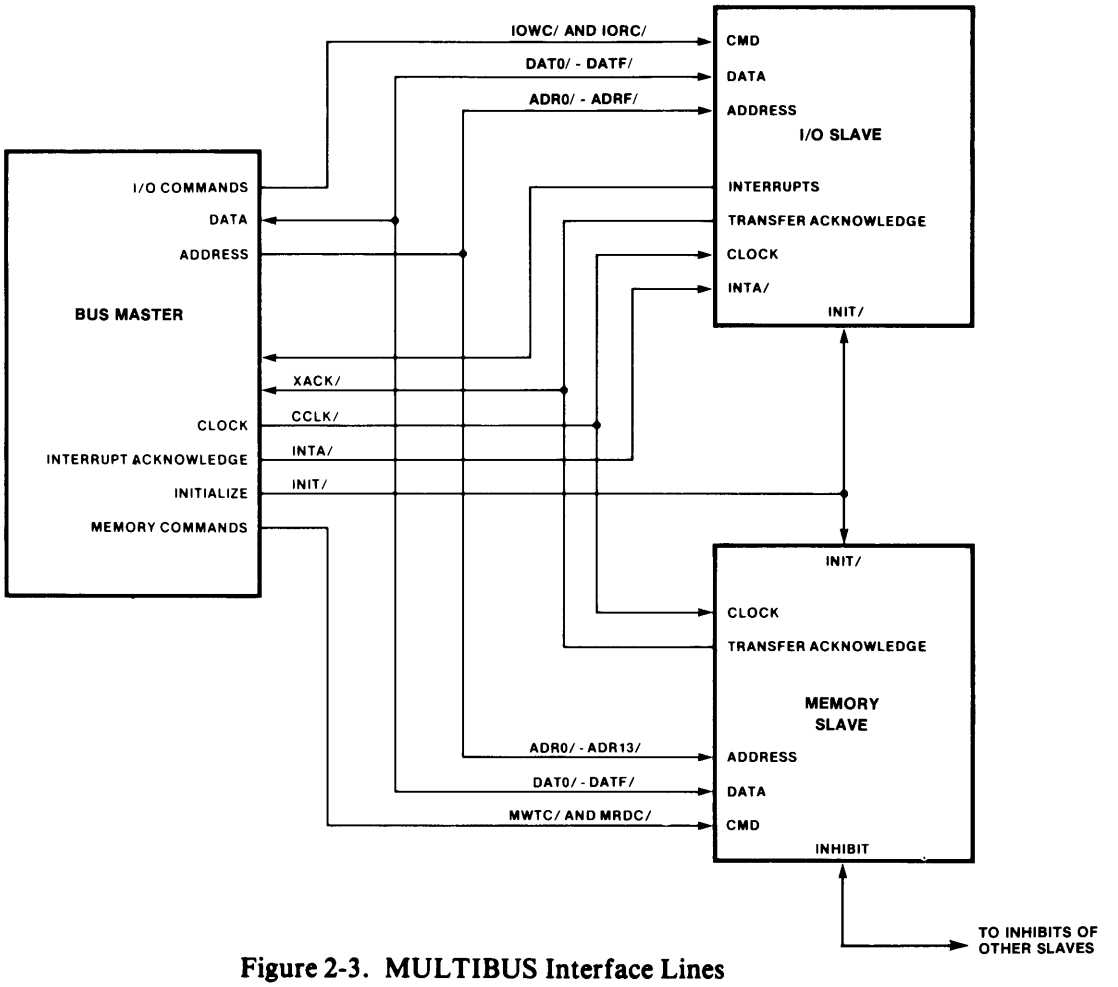


Figure 2-3. MULTIBUS Interface Lines

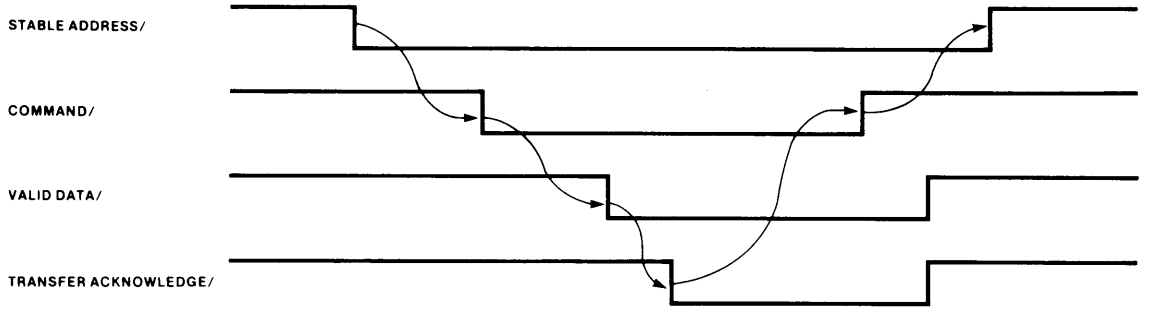


Figure 2-4. MULTIBUS Read Operation

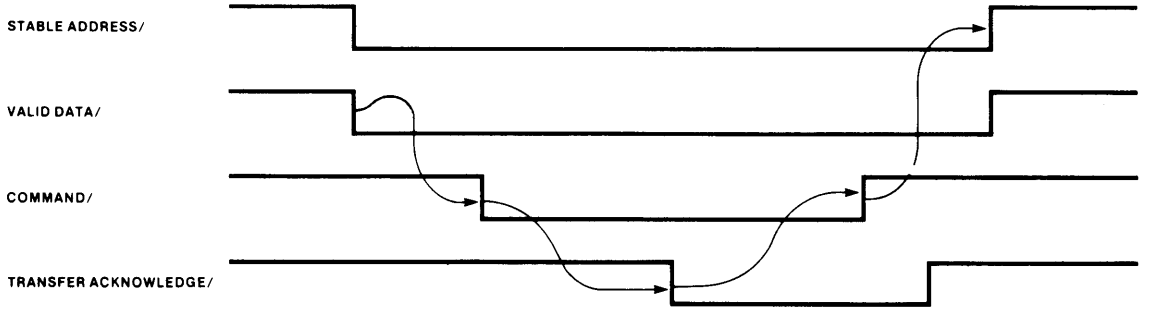


Figure 2-5. MULTIBUS Write Operation

2.2.2.2 CONSTANT CLOCK (CCLK/). The Constant Clock line is driven by only one bus module, and provides a timing source for the MULTIBUS which can be used by any module on the bus. CCLK/ is a symmetrical signal with a frequency of approximately 10 megahertz, driven by a clock driver circuit.

2.2.2.3 ADDRESS LINES (ADR0/ - ADR17/). The MULTIBUS Address lines are used to carry the address of the memory location or the I/O device that is being referenced by the command. There are 24 address lines, allowing up to 16 million bytes of memory to be referenced. These lines are driven by three state drivers and are always under control of the bus master which controls the bus.

During an I/O command, only the lower 16 address lines (ADR0/ - ADRF/) are used. This allows a bus master the capability of addressing a maximum of 64K I/O ports. The address bits are decoded to produce a select signal for each specific port.

Sections 5 and 6 may be referenced for an explanation of the various classes of modules which use a subset of the address lines. These sections also contain design information pertaining to the compatability of the various module classifications.

See figure 2-6 for an example of MULTIBUS address line use.

2.2.2.4 DATA LINES (DAT0/ - DATF/). The sixteen bi-directional data lines are used to transmit or receive information to or from a memory location or I/O port. The lines are driven by the bus master on write operations and by the addressed slave (memory or I/O) on read operations. Both sixteen bit and eight bit transfers are supported by the MULTIBUS. Eight bit transfers are accomplished by using lines DAT0/ - DAT7/ (with DAT0/ being the least significant bit) for eight bit or sixteen bit systems which are compatible with eight bit systems.

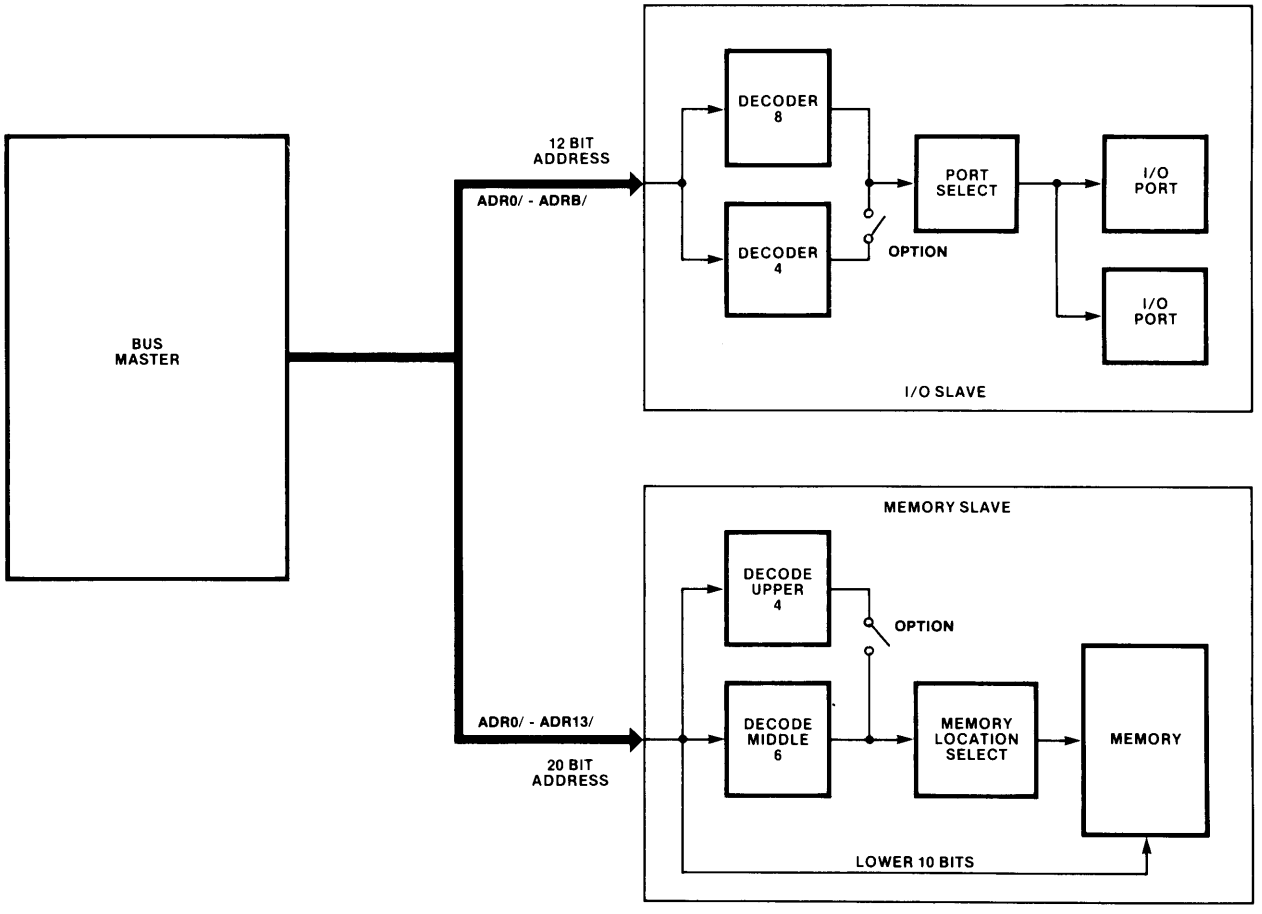


Figure 2-6. MULTIBUS Address Line Use

There are four types of transfers which can take place across the MULTIBUS:

1. Transfer of even byte on DAT0/ - DAT7/.
2. Transfer of odd byte on DAT0/ - DAT7/ (using swap byte buffer).
3. Transfer of 16 bit word.
4. Transfer of odd byte on DAT8/ - DATF/ (sixteen bit system only).

Figure 2-7 shows the MULTIBUS data lines, and the contents of these lines for the four types of transfers mentioned.

Two signals control the data transfers. Byte High Enable (BHEN/) active indicates that the MULTIBUS is operating in sixteen bit mode, and Address Bit 0 (ADR0/) defines an even or odd byte transfer.

On the first type of transfer, BHEN/ is inactive, and ADR0/ is inactive indicating the transfer of an even eight bit byte. The transfer takes place across data lines DAT0/ - DAT7/.

On the second type of transfer, BHEN/ is inactive, and ADR0/ is active indicating the transfer of an odd byte. On this type of transfer, the odd byte is transferred through the Swap Byte Buffer to DAT0/ - DAT7/. This makes eight bit and sixteen bit systems compatible.

The third type of transfer is a 16 bit (word) transfer. This is indicated by BHEN/ being active, and ADR0/ being inactive. On this type of transfer, the even byte is transferred on DAT0/ - DAT7/ and the odd byte is transferred on DAT8/ - DATF/.

The last type of transfer is used on systems which only employ sixteen bit modules. On this transfer BHEN/ is active, and ADR0 is active, indicating the transfer of the odd byte on DAT8/ - DATF/. This type of transfer eliminates the need for the Swap Byte Buffer. It should be noted however, that this is

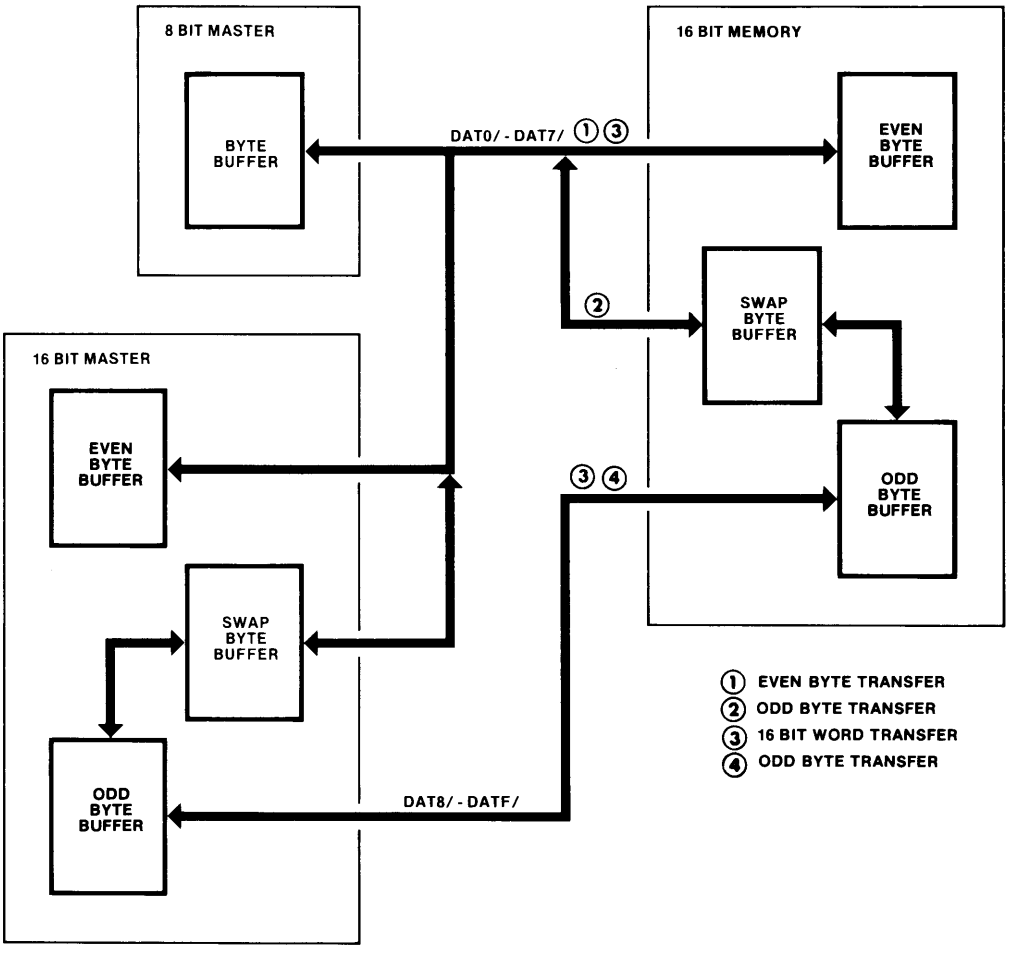


Figure 2-7. MULTIBUS Data Line Use

not a recommended transfer type, because it eliminates the capability of communicating with eight bit modules.

The MULTIBUS data lines are always driven by three state drivers.

2.2.2.5 MULTIBUS COMMANDS. In this section, we will discuss the command lines and how they work in conjunction with the lines explained in the previous sections to accomplish a read or a write operation.

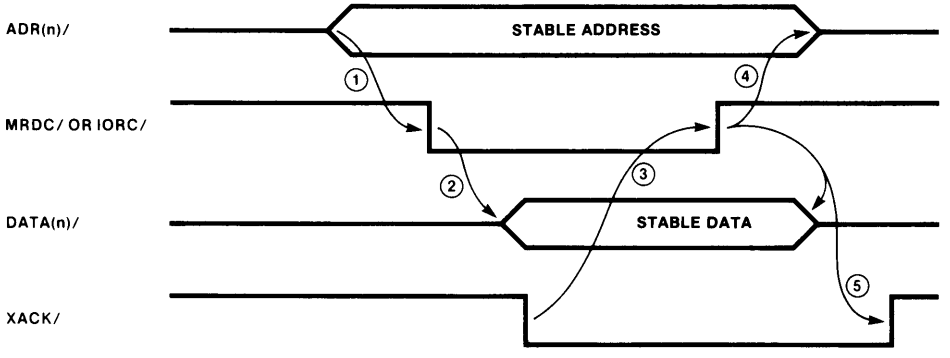
There are four MULTIBUS command lines.

Memory Read Command - MRDC/
I/O Read Command - IORC/
Memory Write Command - MWTC/
I/O Write Command - IOWC/

The command lines, which are driven by three state drivers on the bus master, indicate to the bus slave the action that is being requested.

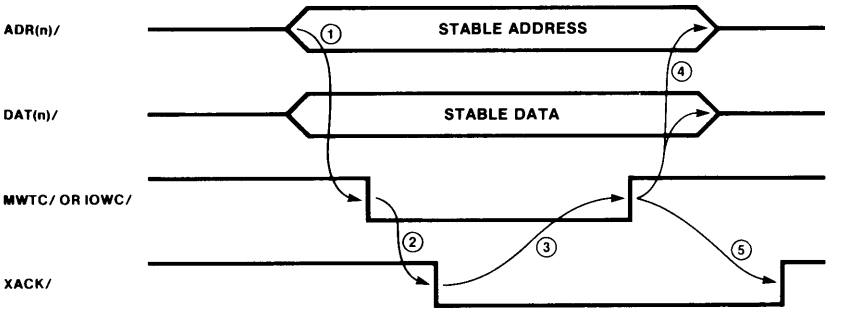
Read Operations. The two read commands (MRDC/ and IORC/) initiate the same basic type of operation. The only difference being that MRDC/ indicates that a memory address is valid on the MULTIBUS address lines, and IORC/ indicates that there is an I/O port address on the MULTIBUS address lines. This address (memory or I/O port) must be valid on the bus 50ns prior to the read command being generated. When the read command is generated, the slave module (memory or I/O port) puts the data on the MULTIBUS data lines and returns a Transfer Acknowledge (XACK/), indicating that the data has been placed on the bus. When the bus master receives the acknowledge, it strobes in the data and removes the command (MRDC/ or IORC/) from the MULTIBUS interface. The slave address (memory or I/O port) is removed from the bus a minimum of 50ns after the read command is removed. XACK/ must be removed from the MULTIBUS interface within 65nsec after the command is removed, to allow for the next bus cycle. Figure 2-8 shows the timing for the Memory Read or I/O Read command.

Write Operations. The write commands (MWTC/ and IOWC/) initiate basically the same type of operation. MWTC/ indicates that a memory address is valid on the MULTIBUS address lines, while IOWC/ indicates that there is an I/O port address on the MULTIBUS address lines. The address (memory or I/O) and data must be valid on the bus 50ns prior to the command being generated. This requirement allows data to be latched on either the leading or trailing edge of the command. When the write command (MWTC/ or IOWC/) is asserted, the MULTIBUS data is stable and can be accepted by the slave. The slave indicates acceptance of the data by returning a Transfer Acknowledge (XACK/), allowing the bus master to remove the address command, and data from the MULTIBUS interface. XACK/ must be removed from the MULTIBUS interface within 65nsec to allow for the next bus cycle. Figure 2-9 shows the timing for the Memory Write or I/O Write command.



(1) ADDRESS SETUP TIME, 50 NANO-SECOND MINIMUM.
(2) TIMED REQUIRED FOR SLAVE TO GET DATA ON TO BUS, XACK/ CAN BE ASSERTED AS SOON AS DATA IS ON BUS.
(3) TIME REQUIRED FOR MASTER TO REMOVE COMMAND.
(4) ADDRESS HOLD TIME, 50 NANO-SECOND MINIMUM.
(5) XACK/ AND DATA MUST BE REMOVED FROM THE BUS A MAXIMUM OF 65 NANOSECONDS AFTER THE COMMAND IS REMOVED.

Figure 2-8. Memory or I/O Read Timing

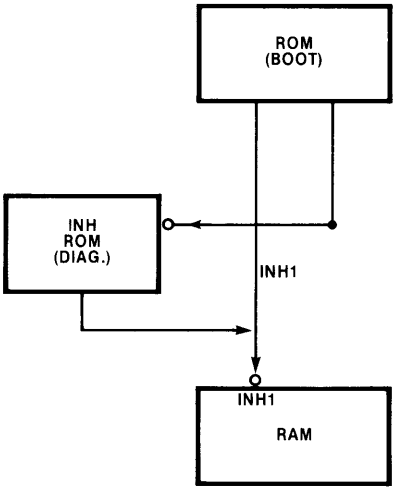


1 ADDRESS AND DATA SETUP, 50 NANO-SECOND MINIMUM.
2 TIMED REQUIRED FOR SLAVE TO ACCEPT DATA.
3 TIME REQUIRED FOR MASTER TO REMOVE COMMAND FROM BUS.
4 ADDRESS AND DATA HOLD TIME, 50 NANO-SECOND MINIMUM.
5 XACK/ MUST BE OFF THE BUS 65 NANO-SECONDS AFTER COMMAND.

Figure 2-9. Memory or I/O Write Timing

2.2.2.6 TRANSFER ACKNOWLEDGE LINE (XACK/). The transfer acknowledge (XACK/) is the response of the bus slave (memory or I/O) indicating that the commanded read or write operation is complete and that the data has been placed on or accepted from the MULTIBUS interface. This signal allows the bus master to proceed to the completion of the current bus cycle. If the bus slave does not generate XACK/, the bus master is not able to remove its command from the bus, and will not be able to terminate its bus cycle. The system therefore would be in an indeterminate state, and system operation could not proceed. This situation can be aleviated by providing a Bus Timeout function which will terminate the bus cycle after some fixed period of time (determined by designer) by generating an XACK/. The Bus Timeout function is a separate piece of logic which constantly monitors the MULTIBUS interface for the above mentioned condition.

2.2.2.7 INHIBIT OPERATION. The Inhibit Lines (INH1/ and INH2/) give different memory components the ability to occupy the same memory space under certain specified conditions. For example, RAM could occupy the whole memory space but during a bootstrap, ROM could be invoked which would overlay a portion of the memory occupied by RAM. In addition, a ROM card containing diagnostics could be inserted into a system overlaying RAM, but letting the bootstrap ROM overlay it. The following diagram illustrates the Inhibit lines.



NOTE

For bootstrap application both INH1/ and INH2/ must be generated.

The RAM inhibit signal (INH1/) prevents the RAM devices from responding to the address on the MULTIBUS address lines, allowing ROM or memory mapped I/O components with the same addresses to use the RAM's memory area.

The ROM inhibit signal (INH2/) is basically the same except that it allows auxiliary ROM components to overlay ROM devices using the same memory space.

The inhibit lines are intended to function only on read operations. During the read of an inhibited memory component, the inhibit signal must disable the acknowledge and data drivers of the component. The effect of an inhibit during a write operation is undefined.

The timing of the inhibit operation is critical. The inhibit signals must be generated within 100nsec after the address is stable. A command is generated 50nsec after the address is stable, therefore the inhibit occurs after the command has already been received by the inhibited component. Since the inhibited module has already started its cycle, it may be necessary for it to complete it to avoid destroying the contents

of RAM. For this reason the inhibiting component must generate an acknowledge (XACK/) which encompasses the acknowledge generated by the inhibited device with the longest cycle time. Also, to prevent false acknowledges, the inhibited device must not generate an acknowledge until the inhibit signals have had time to become valid (50 nsec after command).

Figure 2-10 shows the timing for an inhibit operation. In this example, both PROM and RAM have the same memory addresses, so the PROM inhibits the RAM.

After the address is stable, local selects are generated for both the PROM and the RAM. The PROM local select produces the INH1 signal which then removes the RAM local select, and driver enable. Because the slave RAM has been inhibited after it had already begun its cycle, the PROM XACK/ must be delayed (tXACKB) until after the latest possible acknowledgement from the RAM (tXACKA).

2.2.2.8 LOCK (LOCK/). The lock line is driven by the master in control of the bus when a locked bus access is required. A locked access is typically required in a read-modify-write semaphore operation to prevent another processor from accessing the memory between the read and the write. The busy line allows for this mutual exclusion on the MULTIBUS. The Lock line allows mutual exclusion to be extended off of the bus. The Lock signal (LOCK/) must be active 100 nanoseconds prior to the read or write command going away. It must remain active a minimum of 100 nanoseconds after the falling edge of the command signal for the last locked memory cycle. The slave locks its multiple-ported memory to the MULTIBUS when it is addressed and the lock line is asserted. The lock signal must not be asserted for more than 12 microseconds continuously. This assures the processor on the other side of the multiple-ported memory that it will gain access to the memory in a reasonable amount of time. The busy signal (BUSY/) must be active whenever the Lock line is asserted. Figure 2-12 shows the timing for the lock signal.

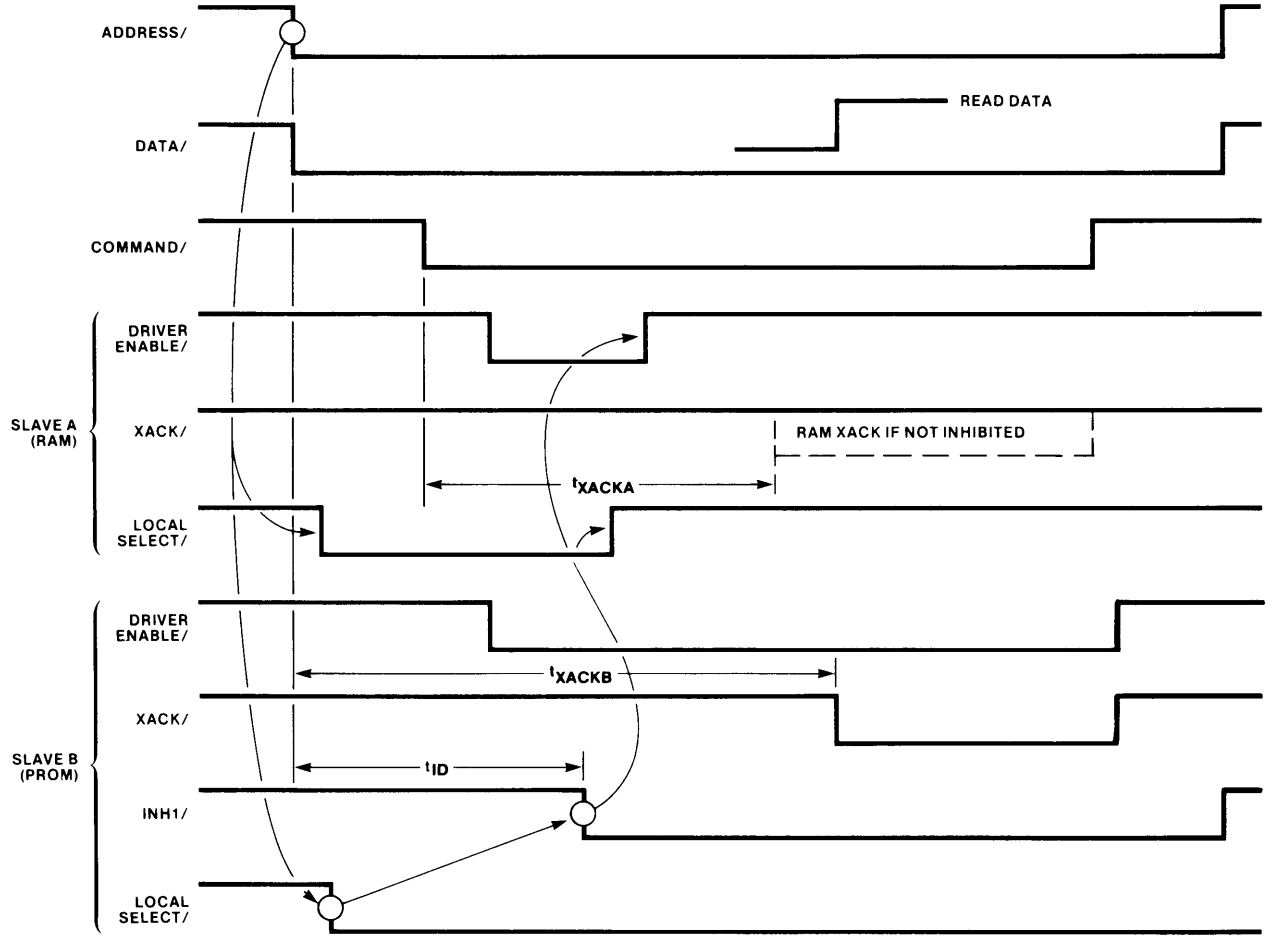


Figure 2-10. Inhibit Timing

2.3 INTERRUPT OPERATIONS

The following sections, will explain the Multibus signal lines used in the interrupt operation, and the two different types of interrupt implementation.

2.3.1 INTERRUPT SIGNAL LINES

2.3.1.1 INTERRUPT REQUEST LINES (INT0/ - INT7/). A set of MULTIBUS interrupt request lines (INT0/ - INT7/) is provided. An interrupt is generated by activating one of the eight interrupt request lines with an open collector driver. All interrupts are level triggered, rather than edge triggered. Requiring no edge allows several sources to be attached to each line. The interrupt request lines are prioritized, with INT0/ having the highest priority.

2.3.1.2 INTERRUPT ACKNOWLEDGE (INTA/). An interrupt acknowledge line (INTA/), driven by the bus master, requests the transfer of interrupt information onto the MULTIBUS interface. The specific information timed onto the bus

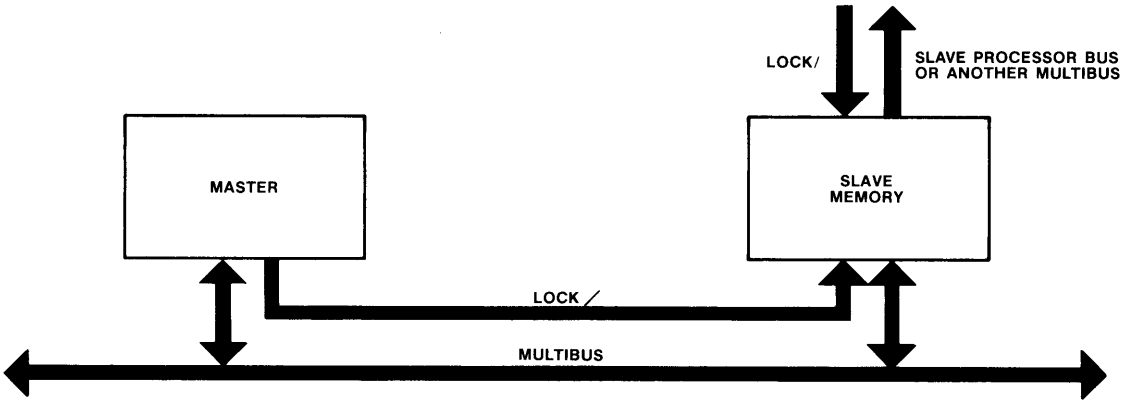


Figure 2-11. Lock Usage

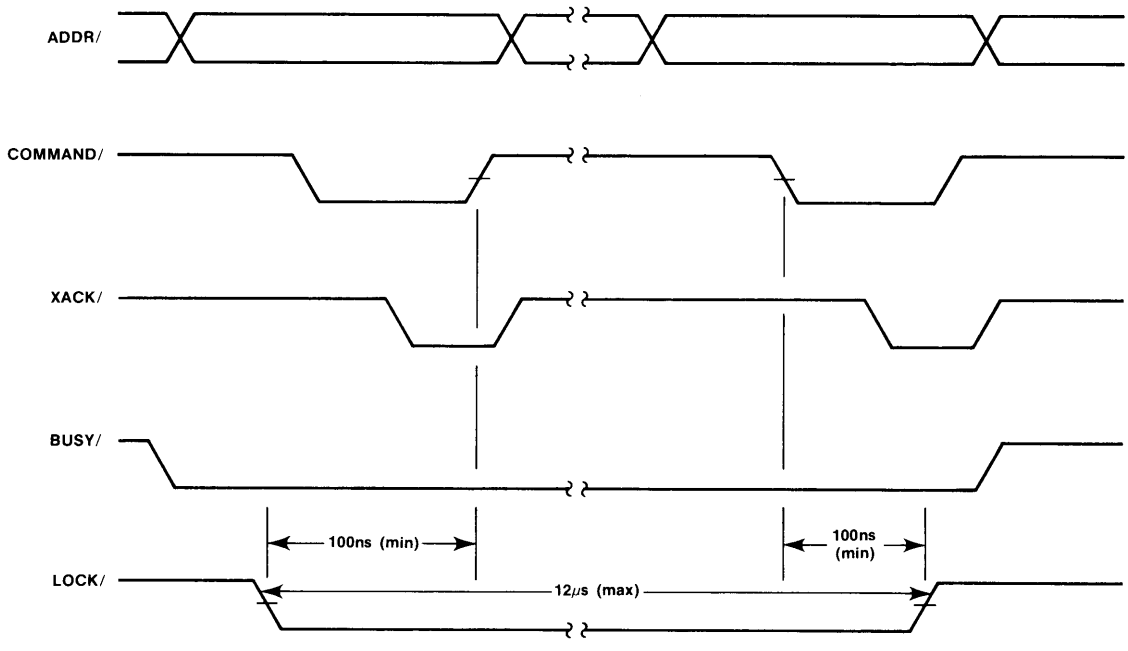


Figure 2-12. Lock Timing

depends upon the implementation of the interrupt scheme. In general, the leading edge of INTA/ indicates that the address bus is active while the trailing edge indicates that data is present on the data lines.

2.3.2 CLASSES OF INTERRUPT IMPLEMENTATION

There are two types of interrupt implementation schemes, Non Bus Vectored (NBV) and Bus Vectored (BV). The two schemes are explained in the following sections.

2.3.2.1 NON BUS VECTORED INTERRUPTS (NBVI). Non Bus vectored interrupts are those interrupts which are handled on the bus master and do not require the MULTIBUS interface for transfer of the interrupt vector address. The interrupt vector address is generated by the interrupt controller on the master and transferred to the processor over the local bus. The slave modules generating the interrupts can reside on the master module or on other bus modules, in which case they use the MULTIBUS interrupt request lines (INT0/ - INT7/) to generate their interrupt requests to the bus master. When an interrupt request line is activated, the bus master performs its own interrupt operation and processes the interrupt. Figure 2-11 shows an example of NBV interrupt implementation.

2.3.2.2 BUS VECTORED INTERRUPTS (BVI). Bus vectored interrupts are those interrupts which transfer the interrupt vector address along the MULTIBUS data lines from the slave to the bus master using the INTA/ command signal for synchronization.

When an interrupt request occurs, the interrupt control logic on the bus master interrupts its processor. The processor on the bus master generates an INTA/ command on the system bus, which freezes the state of the interrupt logic on all bus modules for priority resolution. The bus master also locks (retains the bus between bus cycles) the MULTIBUS to allow back to back bus cycles. After the first INTA command,

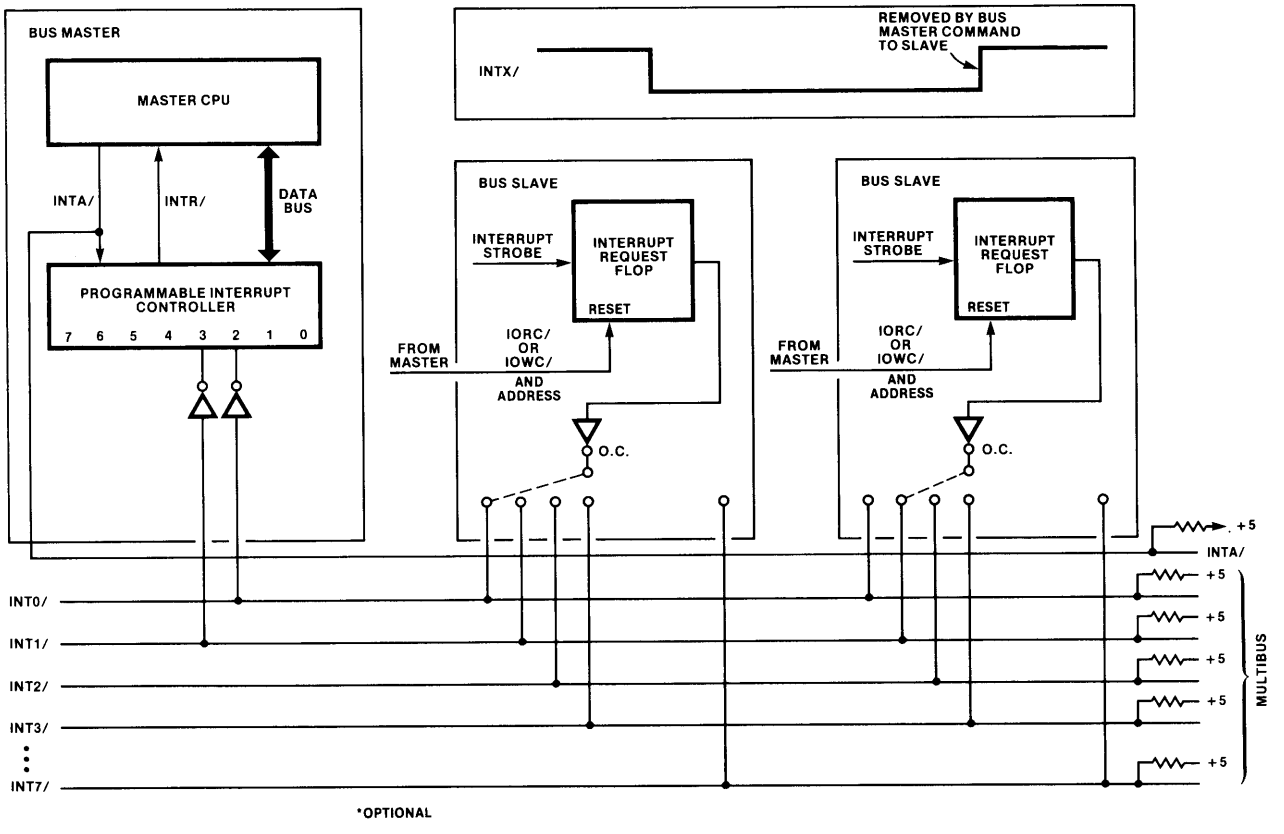


Figure 2-13. Non-Bus Vectored Interrupt Logic

the bus master's interrupt control logic puts an interrupt code on to the MULTIBUS address lines. The interrupt code is the address of the highest priority active interrupt request line. At this point in the BVI procedure, two different sequences could take place. The difference occurs, because the MULTIBUS can support masters which generate two INTAs or three INTAs.

If the bus master generates two INTAs, one more INTA command would be generated. This second INTA would cause the bus slave interrupt control logic to transmit its interrupt vector address on the MULTIBUS data lines. The address would be used by the bus master to service the interrupt.

If the bus master generates three INTAs, two more INTA commands would be generated. These two INTA commands would allow the bus slave to put its two byte interrupt vector address on to the MULTIBUS data lines (one byte for each INTA). The interrupt vector address would be used by the bus master to service the interrupt.

NOTE

The MULTIBUS interface can support only one type of Bus Vectored Interrupt in a given system. However the MULTIBUS interface can support Bus Vectored and Non-Bus Vectored Interrupts at the same time.

Figure 2-12 depicts an example of bus vectored interupt implementation.

2.4 MULTIBUS EXCHANGE

The MULTIBUS interface can accommodate several bus masters on the same system, each one taking control of the bus as it needs to affect data transfers. The bus masters request bus control through a bus exchange sequence.

The discussion of the MULTIBUS Exchange will be seperated into three parts. The first part will explain the signals involved, the second part will discuss the Bus Exchange Priority Techniques (serial and parallel), and the third part will explain the implementation of the Exchange Logic.

2.4.1 MULTIBUS EXCHANGE SIGNALS

A set of six signals is used to implement the MULTIBUS exchange operation.

2.4.1.1 BUS CLOCK (BCLK/). BCLK/ is used to synchronize the exchange logic, with synchronization occuring on the trailing (high to low) edge of the pulse. BCLK/ has a duty cycle of approximately 50 percent, a maximum frequency of 10MHz, and can be slowed, stepped, or stopped as called for by system design. There is no requirement for synchronization between BCLK/ and CCLK/, but they may be derived from the same source. The BCLK/ line is driven by a TTL clock driver.

2.4.1.2 BUS BUSY (BUSY/). BUSY/ is driven by the bus master in control of the bus. All other masters monitor BUSY/ to determine the state of the bus. This signal is bi-directional and is driven by an open collector gate. It is synchronized by BCLK/.

2.4.1.3 BUS PRIORITY IN (BPRN/). BPRN/ indicates to a master that no master of higher priority is requesting MULTIBUS control. BPRN/ is synchronized by BCLK/ and driven by TTL gates. In a serial resolution scheme, this is the master's input from the priority chain. In a parallel resolution scheme, this is the masters input from the parallel priority resolution circuit.

2.4.1.4 BUS PRIORITY OUT (BPRO/). The Bus Priority Out (BPRO/) line is only used in a serial resolution scheme. It is deactivated by a bus master when it requests the MULTIBUS interface, indicating to lower priority masters that a higher priority bus request exists. BPRO/ is driven by TTL gates. BPRO/ is synchronized by BCLK/.

2.4.1.5 BUS REQUEST (BREQ/). The Bus Request line (BREQ/) is used with the parallel priority resolution scheme, and is a request of a master for MULTIBUS control. The priorities of the BREQ/s from each master are resolved in a parallel priority resolution circuit. The highest priority request enables the BPRN/ input of that master, allowing it to gain control of the bus. BREQ/ is synchronized by BCLK/ and is a TTL output.

2.4.1.6 COMMON BUS REQUEST (CBRQ/) (optional). Any master which wants control of the MULTIBUS interface but does not control it, can activate CBRQ/ with an open collector gate. If CBRQ/ is high it indicates to the bus master that no other master is requesting the bus and therefore the present bus master can retain the bus. This saves the bus exchange overhead for the current master.

NOTE

All the bus exchange signals are synchronized by BCLK/.

2.4.2 BUS EXCHANGE PRIORITY TECHNIQUES

Two bus exchange priority techniques are discussed, a serial technique or a parallel technique. Figures 2-13 and 2-14 illustrate these two techniques. The bus exchange implementation discussed in Section 2.5 is the same for both techniques.

2.4.2.1 SERIAL PRIORITY TECHNIQUE. Serial priority resolution is accomplished with a daisy chain technique (see figure 2-13). The priority input (BPRN/) of the highest priority master is tied to ground. The priority output (BPRO/) of the highest priority master is then connected to the priority input (BPRN/) of the next lower priority master, and so on. Any master generating a bus request will raise the priority line to all the lower priority masters. In this implementation, the bus request line (BREQ/) is not used outside of the individual masters. A limited number of masters can be accomodated by this technique, due to the gate delays through the daisy chain.

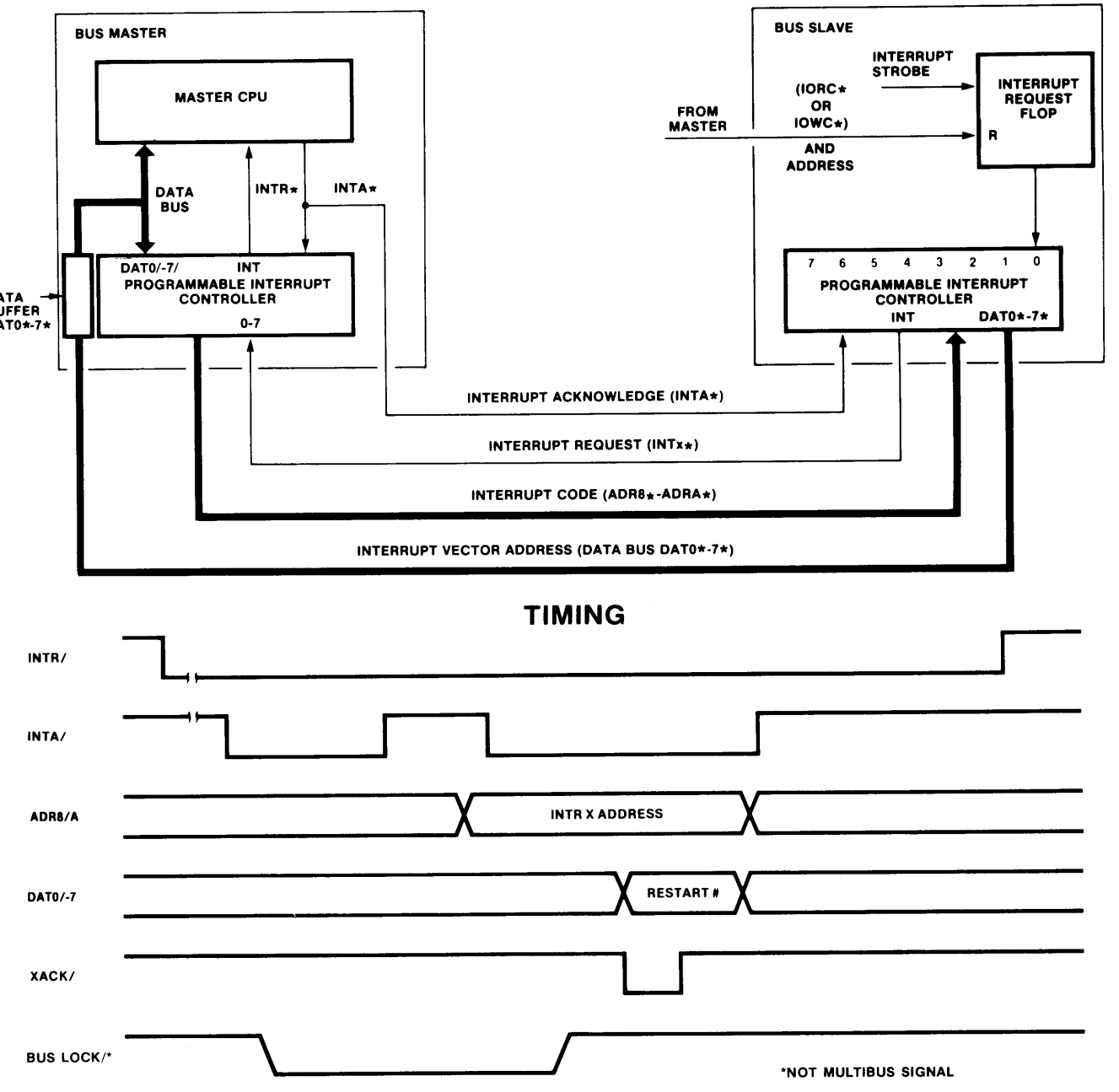


Figure 2-14. Bus Vectored Interrupt

2.4.2.2 PARALLEL PRIORITY TECHNIQUE. In the parallel priority technique, the priority is resolved in a priority resolution circuit in which the highest priority input is encoded at the chip outputs. This coded value is then decoded to activate the appropriate BPRN/ line. The BPRO/ lines are not used in the parallel priority scheme. Up to sixteen masters can be accomodated by the parallel priority technique.

2.4.3 MULTIBUS EXCHANGE IMPLEMENTATION

The MULTIBUS exchange implementation is shown in figure 2-15. This implementation example uses a parallel resolution scheme, however the timing would be basically the same for the serial resolution scheme.

In this example, master A has been assigned a lower priority than master B. The bus exchange occurs because master B generates a bus request during a time when master A has control of the bus.

The exchange process begins when master B requires the bus to access some resource such as an I/O or memory module. This internal request is synchronized with the trailing edge (high to low) of BCLK/ to generate a bus request (BREQ/). The bus priority in signal (BPRN/) to master A is inactive. Master A

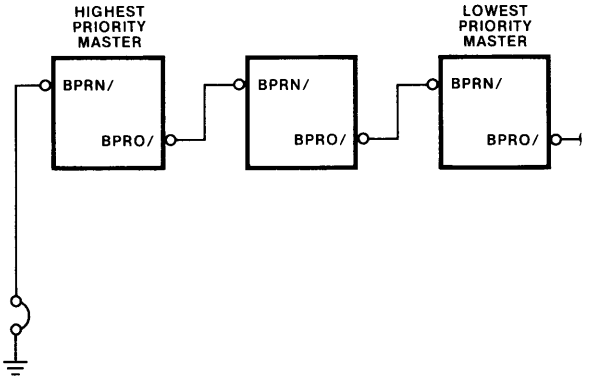


Figure 2-15. Serial Priority Technique

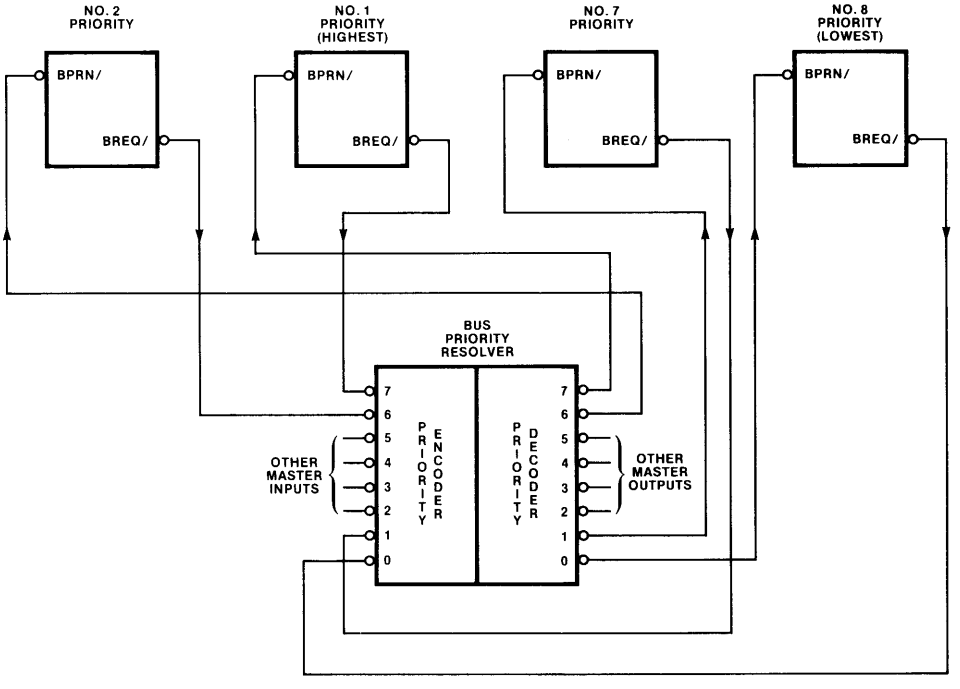


Figure 2-16. Parallel Priority Technique

must first complete the current bus command if one is in operation. After it completes the command, BUSY/ goes inactive on the next trailing edge of BCLK/. This allows the actual bus exchange to occur, because master A has relinquished control of the bus, and master B has been granted its BPRN/. During this time, the drivers for master A are disabled. Master B must take control of the bus with the next trailing edge of BCLK/ to complete the bus exchange. Master B takes control by activating BUSY/ and enabling its drivers.

It is possible for master A to retain control of the bus and prevent master B from getting control. Master A

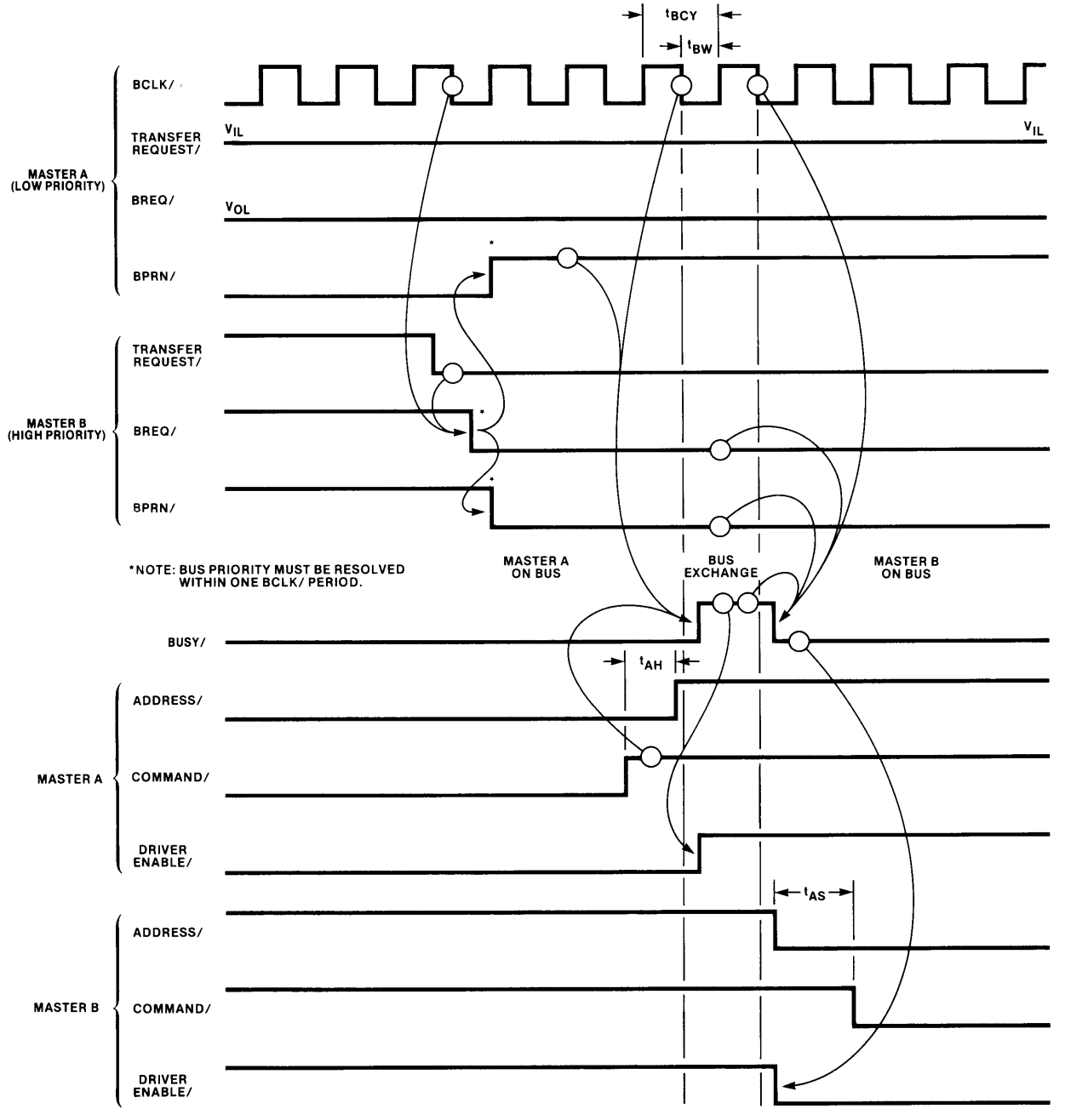


Figure 2-17. Bus Exchange Timing

activates an internal signal called Override (or Bus Lock) which keeps BUSY/ active allowing control of the bus to stay with master A. This guarantees a master consecutive bus cycles for such software functions as Test and Set.

2.5 POWER FAILURE CONSIDERATIONS

The MULTIBUS interface provides a means of handling power failures. The following sections, define the signals used for power failure handling, and the sequence of events followed when a power failure occurs. Figure 2-16 shows the timing of the power fail sequence.

NOTE

The power failure feature is optional. The signals used with this feature are on auxiliary connector P2.

2.5.1 MULTIBUS POWER FAILURE SIGNALS

2.5.1.1 AC LOW (ACLO). This signal, generated by the power supply, goes high when the AC line voltage drops below a certain voltage* indicating D.C. power will fail in a minimum of 3 msec. ACLO goes low when all D.C. voltages return to 95% of their indicated value. This line must be pulled up by the standby power source.

*NOTE

The value used depends upon supply voltage, and power supply design. A typical value for 120V AC is 100V AC.

2.5.1.2 POWER FAIL INTERRUPT (PFIN/). This signal interrupts the processor when a power failure occurs, as indicated by ACLO.

2.5.1.3 POWER FAIL SENSE (PFSN/). This line is the output of a latch which indicates that a power failure has occurred. It is reset by Power Failure Sense Reset (PFSR/) and must be powerd by the standby power source.

2.5.1.4 POWER FAIL SENSE RESET (PFSR/). This line is used to reset the power fail sense latch (PFSN/)

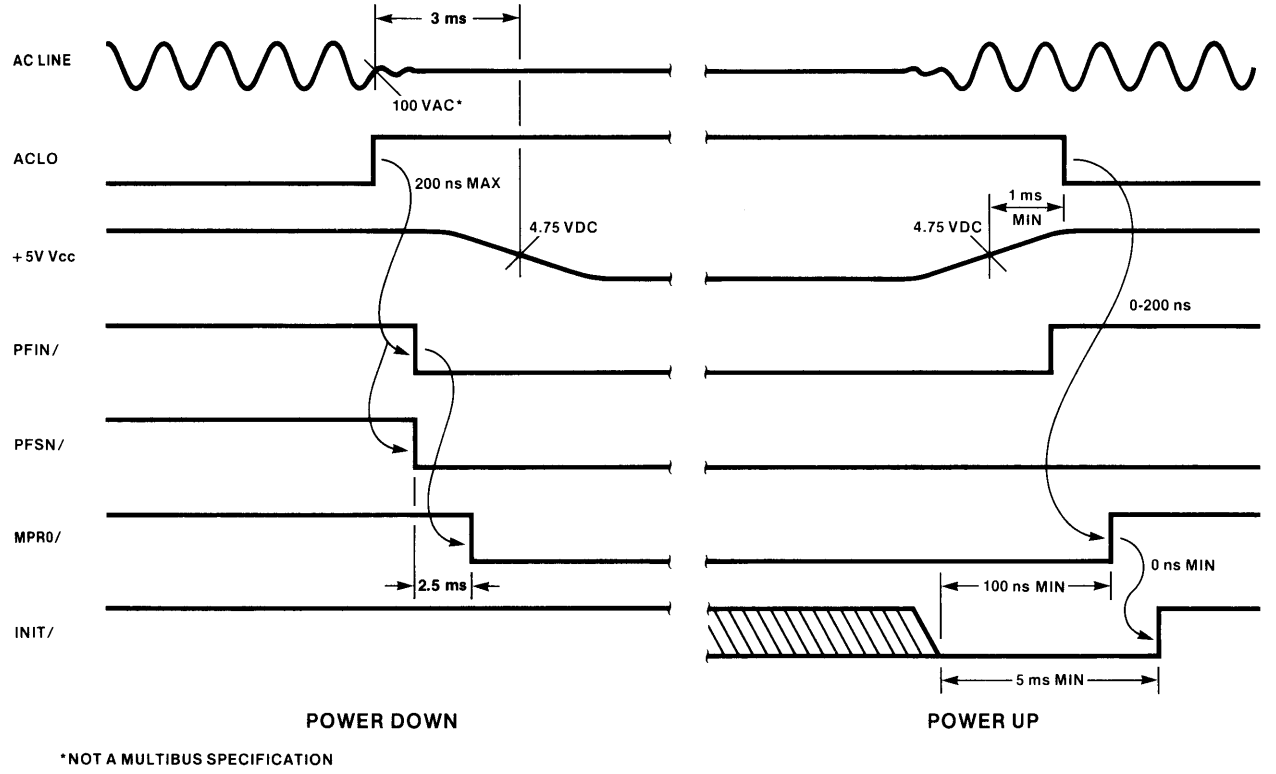


Figure 2-18. Power Fail Timing Sequence

2.5.1.5 MEMORY PROTECT (MPRO/). Prevents memory operation during periods of uncertain DC power by inhibiting memory requests.

2.5.1.6 INITIALIZE (INIT/). The INIT/ line resets the entire system to a known internal state.

2.5.2 POWER FAIL SEQUENCE

The power supply monitors the AC power level. When it drops below an acceptable value, the power supply raises ACLO which tells the power fail logic that a minimum of three milliseconds will elapse before power will fall below an operating level. The power fail logic sets a sense latch (PFSN/) and generates an interrupt to the processor so that it can store its environment. After a 2.5 millisecond timeout, the memory protect signal (MPRO/) is asserted, preventing any memory activity. As power falls, the memory goes on standby power. Note that the power fail logic must be powered from the standby source.

As the AC line revives, the power supply voltage level is monitored. After power has been at its operating level for one millisecond minimum, the signal ACLO goes low, beginning the restart sequence. First the memory protect line (MPRO/) then the initialize line (INIT/) become inactive. The bus master now starts running. The bus master(s) checks the power fail latch (PFSN/) and, if it finds it set, branches to a power up routine which resets the latch (PFSR/), restores the environment, and resumes execution.

Note that INIT/ is activated until power has risen to some operable level and must stay low for five milliseconds minimum before the system is allowed to restart. Alternatively, INIT/ may be held low through an open collector device by MPRO/.

How the power failure equipment is configured is left to the system designer. The backup power source may be batteries located on the memory boards or more elaborate facilities located off-board. The location of the power fail logic determines what lines appear on the MULTIBUS interface. Pins on the P2 connector have been specified for the power failure functions for use as needed.

SECTION 3
ELECTRICAL SPECIFICATION

3.0 INTRODUCTION

All electrical specifications for the MULTIBUS are presented in this chapter.

Section 3.1 presents the general bus consideration of State Relationships, Signal Line Characteristics, and Power Supplies.

Section 3.2 contains the timing specifications for the MULTIBUS.

The final Section, 3.3, contains specifications for the signal line drivers and receivers, as well as the electrical termination requirements.

When electrical specifications indicate minimum or maximum values for the MULTIBUS, they must be measurable at any point on the bus.

Note that a particular implemented bus could have any amount of bus propagation delay and ringing (before setup times), as long as all bus parameters (e.g.; setup, hold, and other times) were met at all points on the bus. However, in order to facilitate the design of a compatible set of modules (masters and slaves) that use the bus, the standard maximum bus propagation delay will be specified as t_{PD} (max).

Table 3-1 summarizes all of the key figures and tables in this chapter.

Table 3-1. Location of Key Information

Summary Information		Section
Figure 3-1	Setup, Hold, Ringing Summary	3.1.2
Figure 3-2	Coupling	3.1.2
Table 3-2	Power Supply Specifications	3.1.3
Table 3-3	Timing Specifications Summary	3.2
Table 3-4	Receivers, Bus Drivers, and Terminations	3.3

3.1 GENERAL BUS CONSIDERATIONS

3.1.1 LOGICAL AND ELECTRICAL STATE RELATIONSHIPS

Electrical state relationships apply to all bus signal lines as described functionally in Section 2.

The signal names indicate whether or not the signal lines on the MULTIBUS are active high or active low. If the signal name ends with a slash ("/"), then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	H = TTL high state	5.25V≥H≥2.0V	5.25V≥H≥2.4V
1	L = TTL low state	.8V≥L≥-.5V	.5V≥L≥0V

If the signal name has no slash (no "/"), then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L = TTL low state	.8V≥L≥-.5V	.5V≥L≥0V
1	H = TTL high state	5.25V≥H≥2.0V	5.25V≥H≥2.4V

These specifications are based on TTL where the power source is 5 volts ± 5%, referenced to logic ground (GND).

When specified, current flow into a node has a positive sign and out of a node a negative sign.

3.1.2 SIGNAL LINE CHARACTERISTICS

Described below are two types of requirements. The first includes the requirements on the signal line that are measured when the signal line is in use. The second type includes those that are measured under special test conditions.

3.1.2.1 IN-USE SIGNAL LINE REQUIREMENTS. During normal use the rise and fall times of the signals depend on which type of driver is used (refer to Table 3-4):

	Open Collector	Totem Pole	3-State
Rise Time (from low to high)	—	10ns	10 ns
Fall Time	10 ns	10ns	10ns

(where "high" is TTL high, minimum; and "low" is TTL low, maximum; see Section 3.1.1)

The typical signal propagation delay on the MULTIBUS is t_{PD}(typ). This is measured from the edge of any one board plugged into the MULTIBUS to any other board plugged into the MULTIBUS.

t_{PD}(typ) = 3ns

These dynamic signal requirements can be tested for acceptance by using 74S20 gates as drivers.

NOTE

For all boards plugged into the MULTIBUS the Setup, Hold, and any other times are measured at the edge of the board where it is plugged into the MULTIBUS. This means that all board-internal delays must be taken into account while still providing for the Setup, Hold, and other times.

After Power-Up, the following specifications apply.

The bus termination required for each signal line is given in Table 3-4,. Referenced for each signal is the section in which specific termination, receiver, and driver requirements are given. For physical locations for bus terminators refer to Design Guidelines and System Application Section 5.7.

The settling time for all command line signals (see Section 2.2.5) after a transition, is zero. On these lines the ringing cannot go beyond the noise immunity levels—i.e., high, minimum; or low, maximum. This also applies to all Acknowledge and Inhibit lines.

For all address lines (see Section 2.2.2) the signals must be stable (settled) at least 50ns before any command line goes active (setup time). This settling requirement means there can be no ringing beyond the noise immunity levels (High, min; Low, max). These requirements also apply to the Data lines (Section 2.2.2) during any write operations.

For all data lines, during read operations, the setup time is 0ns before the Transfer Acknowledge (XACK/) signal goes active; and the hold time is 0ns after the read-type command goes inactive.

The setup, hold, and command ringing is summarized and graphically presented in figure 3-1.

3.1.2.2 BACKPLANE SIGNAL TRACE CHARACTERISTICS. Requirements for line-to-line coupling characteristics are shown in Figure 3-2. The specific test conditons under which the specifications are to be met are shown.

Refer to Section 4 for mechanical restrictions on trace characteristics.

3.1.3 BUS POWER SPECIFICATIONS

Table 3-2 provides all Bus power specifications.

Table 3-2. Bus Power Specifications

	Standard (P1)				Optional (P2)					
					Analog Power		Battery Power Backup			
	Ground	+5	+12	-12	+15	-15	+5	+12	-12	-5
Mnemonic	GND	+5V	+12V	-12V	+15V	-15V	+5B	+12B	-12B	-5B
Bus Pins	P1+1,2, 11,12, 75,76, 85,86	P1+3,4 5,6,81, 82,83, 84	P1+7,8	P1+79, 80	P2+23,24	P2+25,26	P2+3,4, 5,6	P2+11, 12	P2+15, 16	P2-7, 8
Nominal Output	Ref.	+5.0V	+12.0V	-12.0V	+15.0V	-15.0V	+5.0V	+12.0V	-12.0V	-5.0V
Tolerance from Nominal[1]	Ref.	±5%	±5%	±5%	±3%	±3%	±5%	±5%	±5%	±5%
Ripple (Pk-Pk)[2]	Ref.	50mV	50mV	50mV	10mV	10mV	50mV	50mV	50mV	50mV
Transient Response Time[3]		500μs	500μs	500μs	100μs	100μs	500μs	500μs	500μs	500μs
Transient Deviation[4]		±10%	±10%	±10%	±10%	±10%	±10%	±10%	±10%	±10%

NOTES:
1. Tolerance is worst case, including initial voltage setting, line and load effects of power source, ripple, temperature drift, and any additional steady state influences.
2. As measured over any bandwidth not to exceed 0 to 5 MHz.
3. As measured from the start of a load change to the time an output recovers with ±0.1% of final voltage (50% load change).
4. Measured as the peak deviation from the initial voltage.

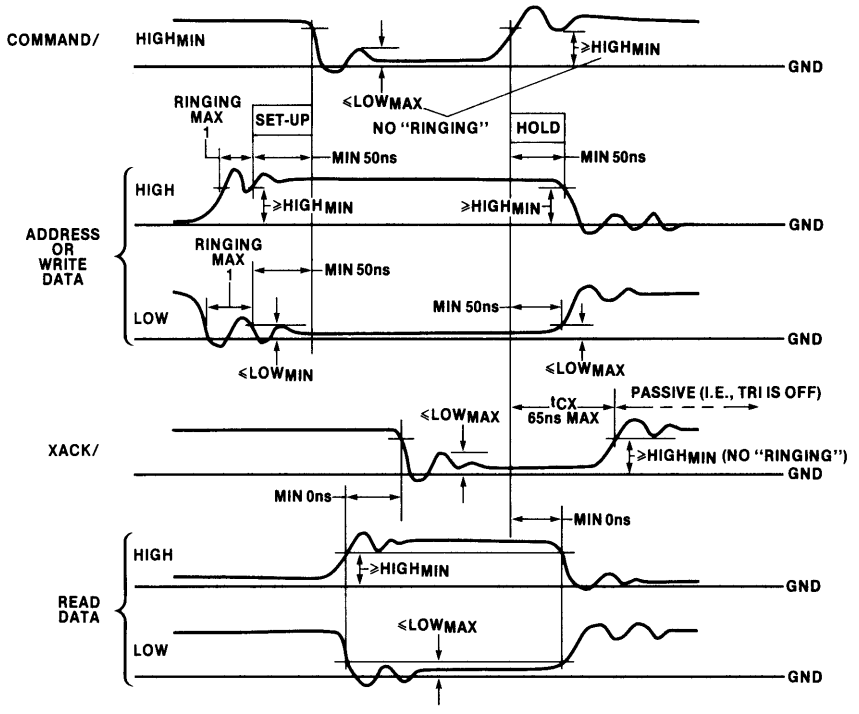


Figure 3-1. Setup, Hold, Ringing Summary

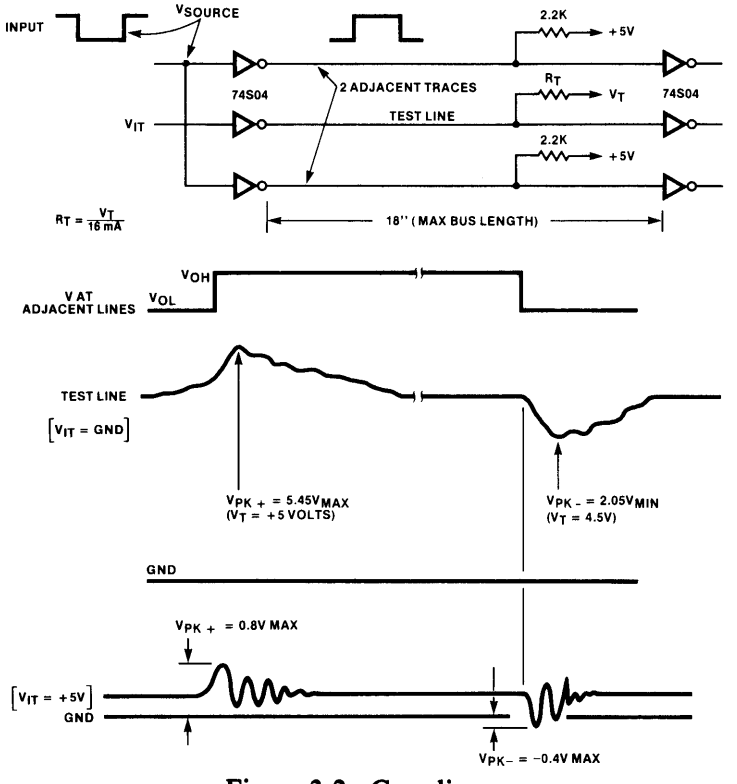


Figure 3-2. Coupling

All voltages not shown in table 3-2, that may be required on a board plugging into the MULTIBUS should be derived from one of the standard voltages (+5, ± 12).

See Section 5.4 for guidelines and examples of power failure circuitry. Section 5-6 describes on-board filter capacitors. Section 5.5 (Design Recommendation Summary) includes power supply guidelines.

Refer to Section 6.5.1 for power supply voltages that may exist in early MULTIBUS-type systems.

3.1.4 TEMPERATURE AND HUMIDITY

All bus specifications should be met while the temperature and humidity are within the following ranges:

Temperature: 0-55°C (32-150°F) Free moving air across modules and bus.

Humidity: 90% Max Relative (No Condensation)

These represent a standard environment for the MULTIBUS. It may be desireable to create more (or less) severe environmental restrictions in some applications.

3.2 TIMING

This section describes all timing specifications on the MULTIBUS. It does not present descriptions or functional relationships (which are given in Section 2). This section does imply the functionality when relating two signals. Section 2 should be referred to for all ambiguities.

Table 3-3 summarizes all of the timing specifications in this section. For detailed descriptions refer to the specific sections indicated in the table.

The timing diagrams shown in this section usually show the MIN or MAX values required for each parameter. However, for clarity in the diagrams, parameters usually do not have MINIMUMS and MAXIMUMS both indicated on the diagram. The Bus Timing Specification table (Table 3-3) should be referenced for completed MIN/MAX information. The timing diagrams show how all of the parameters are defined in relation to the signals involved. All timing is measured at 1.5V with loading capacitance C_O and terminations as specified in Table 3-4.

Table 3-3. Bus Timing Specifications Summary

Parameter	Description	Minimum	Maximum	Units	Sections To Reference
t_{BCY}	Bus Clock Period	100	∞ (D C)	ns	3.2.5
t_{BW}	Bus Clock Width	0.35 t_{BCY}	0.65 t_{BCY}	ns	3.2.5
t_{SKEW}	BCLK/skew		t_{PD}	ns	3.2.5
$t_{PD(typ)}$	Standard Bus Propagation Delay		3	ns	3.1.2, 3.2.5
t_{AD}	Address Disable	100		ns	
t_{AS}	Address Set-Up Time (at Slave Board)	50		ns	3.2.1, 3.2.2, 3.2.4
t_{DS}	Write Data Set Up Time	50		ns	3.2.2
t_{AH}	Address Hold Time	50		ns	3.2.1, 3.2.2, 3.2.4
t_{DHW}	Write Data Hold Time	50		ns	3.2.2
t_{DXL}	Read Data Set Up Time To XACK	0		ns	3.2.1, 3.2.4
t_{DHR}	Read Data Hold Time	0	65	ns	3.2.1, 3.2.4
t_{XAH}	Acknowledge Hold Time	0	65	ns	3.2.1, 3.2.2, 3.2.4

Table 3-3. Bus Timing Specifications Summary (Cont'd.)

Parameter	Description	Minimum	Maximum	UNITS	Sections To Reference
t_{XACK}	Acknowledge Time	0	8	μs	3.2.1,3.2.2, 3.2.4
t_{CMD}	Command Pulse Width	100	t_{TOUT}	ns	3.2.1, 3.2.2
t_{ID}	Inhibit Delay	0	100 (Recommend <100 ns)	ns	3.2.3
t_{XACKA}	Acknowledge Time of an Inhibited Slave	t_{IAD} + 50ns	1500	ns	3.2.3
t_{XACKB}	Acknowledge Time of an Inhibiting Slave	1.5	8	μs	3.2.3
t_{IAD}	Acknowledge Disable from Inhibit (An internal parameter on an inhibited slave; used to determine t_{XACKA} Min.)	0	100 (Arbitrary)	ns	2.3.2
t_{INTA}	INTA/ Width	250		ns	3.2.4
t_{CSEP}	Command Separation	100		ns	3.2.4, 3.2.6
t_{BREQL}	↓BCLK/ to BREQ/ Low Delay	0	35	ns	3.2.5
t_{BREQH}	↓BCLK/ to BREQ/ High Delay	0	35	ns	3.2.5
t_{BPRNH}	BPRN/ to ↓BCLK/ hold	5		ns	
t_{BPRNS}	BPRN/ to ↓BCLK/ Setup Time	22		ns	3.2.5
t_{BUSY}	BUSY/ delay from ↓BCLK/	0	70	ns	3.2.5
t_{BUSYS}	BUSY/ to ↓BCLK/ Setup Time	25		ns	3.2.5
t_{BPRO}	↓BCLK/ to BPRO/ (CLK to Priority Out)	0	40	ns	3.2.5
t_{BPRNO}	BPRN/ to BPRO/ (Priority In to Out)	0	30	ns	3.2.5
t_{CBRO}	↓BCLK/ to CBRQ/ (CLK to Common Bus Request)	0	60	ns	3.2.5
t_{CBRQS}	CBRQ/ to ↓BCLK/ Setup Time	35		ns	3.2.5
Serial Priority	See Section 3.2.5				
t_{XCD}	XACK↓ to Command↑ Delay	20		ns	3.21 3.2.2
t_{BSYO}	CBRQ/↓ or BUSY/↓ to BUSY/↑ Delay	—	12	μs	3.2.5
t_{LCKH}	LOCK/ hold time from Command/↓	100		ns	3.2.6
t_{LCKS}	LOCK/ to Command Setup Time	100		ns	3.2.6
t_{LOCK}	LOCK/ Width		12	μs	3.2.6
t_{CPM}	Central Priority Module Resolution delay. (Parallel Priority)	0	t_{BCY}-t_{BREQ} -2t_{PD} -t_{BPRNS} -t_{SKEW}		3.2.5

Table 3-3. Bus Timing Specifications Summary (Cont'd.)

Parameter	Description	Minimum	Maximum	Units	Sections To Reference
t_{CCY}	C-clock Period	100	110	ns	3.2.6
t_{CW}	C-clock Width	$0.35t_{CCY}$	$0.65t_{CCY}$	ns	3.2.6
t_{INIT}	INIT/ Width	5		ms	3.2.6 3.2.7
t_{INITS}	INIT/ to MPRO/ Setup Time	100		ns	3.2.7
t_{PBD}	Power Backup Logic Delay	0	200	ns	3.2.7
t_{PBDI}	Power Backup Logic Delay	200		ns	3.2.7
t_{PFINW}	PFIN/ Width	2.5		ms	3.2.7
t_{MPRO}	MPRO/ Delay	2.0	2.5	ms	3.2.7
t_{ACLOW}	ACLO/ Width	3.0		ms	3.2.7
t_{PFSRW}	PFSR/ Width	100		ns	3.2.7
t_{TOUT}	Timeout Delay	1	∞ (DC)	ms	—
t_{DCH}	D.C. Power Supply Hold from ACLO/	3.0		ms	3.2.7
t_{DCS}	D.C. Power Supply Setup to ACLO/	1		ms	3.2.7

* = is maximum t_{XACK} of all inhibited boards.

3.2.1 READ OPERATIONS (I/O AND MEMORY)

A Read operation transfers data from memory or from I/O to the master that is controlling the bus. For detailed functional descriptions refer to Section 2.2. The lines involved and timing specifications for a Read Operation are as follows (figure 3-3):

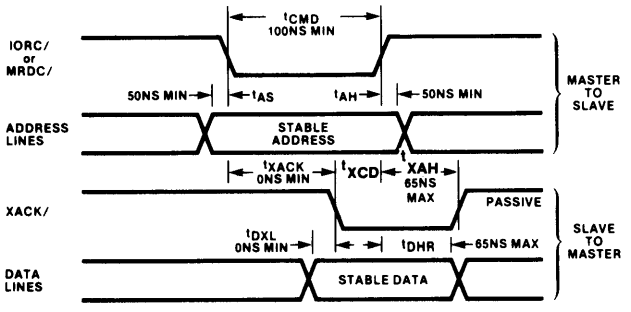


Figure 3-3. Read AC Timing

See Section 5.1 for guidelines and examples. See also the special inhibit operation in Section 3.2.3. For system anomalies with respect to read commands see Section 6.5.

3.2.2 WRITE OPERATIONS (I/O AND MEMORY)

A Write Operation transfers data from the master (that is controlling the bus) to the memory or I/O. For detailed functional descriptions refer to Section 2.2. Timing for a Write Operation is as follows (figure 3-4):

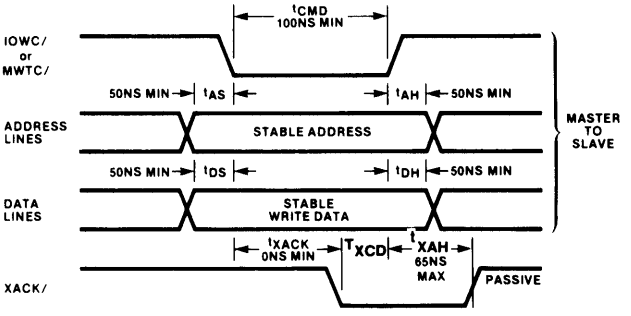


Figure 3-4. Write AC Timing

See Section 5 for guidelines and examples, Section 6.5 for Write-related system anomalies, and Section 3.2.3 for inhibit operations.

3.2.3 INHIBIT OPERATIONS

An Inhibit operation may accompany any Memory Read or Memory Write operation. This allows one slave to inhibit another slave from driving the data lines and from returning (driving) an acknowledge (XACK/). Although inhibit signals may be generated during IORC/, IOWC/, or INTA/ operations, these signals are ignored by other slaves (including the slave that should respond to the INTA/, IORC/, or IOWC/). Inhibit timing is as follows (figure 3-5):

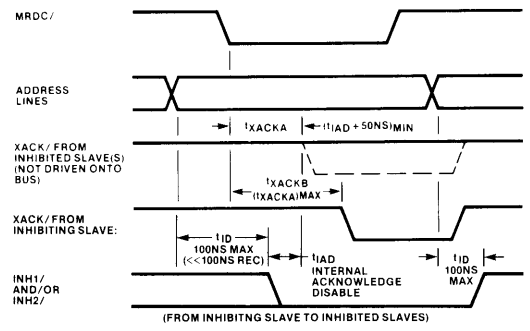


Figure 3-5. Inhibit AC Timing

Related sections are:

Functional Descriptions	2.2.2.7
Timing Specification Summary	3.2
Guidelines and Examples	5
Read Operations	3.2.1
Write Operations	3.2.2
Interrupt Operations	3.2.4

3.2.4 INTERRUPT IMPLEMENTATIONS

There are two types of interrupt implementation schemes, Non Bus Vectored (NBV) and Bus Vectored (BV). The two schemes are explained in the following sections.

3.2.4.1 NON BUS VECTORED INTERRUPTS (NBVI) Non Bus vectored interrupts are those interrupts which are handled on the bus master and do not require the MULTIBUS interface for transfer of the interrupt vector address. The interrupt vector address is generated by the interrupt controller on the master and transferred to the processor over the local bus. The slave modules generating the interrupts can reside on the master module or on other bus modules, in which case they use the MULTIBUS interrupt request lines (INT0/ - INT7/) to generate their interrupt requests to the bus master. When an interrupt request line is activated, the bus master performs its own interrupt operation and processes the interrupt.

3.2.4.2 BUS VECTORED INTERRUPTS (BVI) Bus vectored interrupts are those interrupts which transfer the interrupt vector address along the MULTIBUS interface from the slave to the bus master using the INTA/ command signal (see figure 3-6).

When an interrupt request occurs, the interrupt control logic on the bus master interrupts its processor. The processor on the bus master generates an INTA/ command which freezes the state of the MULTIBUS interrupt logic for priority resolution. The bus master also locks (retains the bus between bus cycles) the MULTIBUS interface to guarantee itself back to back bus cycles. After the first INTA command, the bus master's interrupt control logic puts an interrupt code on to the MULTIBUS address lines. The interrupt code is the address of the highest priority active interrupt request line. At this point in the BVI procedure, two different sequences could take place. The difference occurs, because the MULTIBUS interface can support masters which generate two INTAs or three INTAs.

If the bus master generates two INTAs, one more INTA command would be generated. This second INTA would cause the bus slave interrupt control logic to transmit its interrupt vector address on the MULTIBUS data lines. The address would be used by the bus master to service the interrupt.

If the bus master generates three INTAs, two more INTA commands would be generated. These two INTA commands would allow the bus slave to put its two byte interrupt vector address on to the MULTIBUS data lines (one byte for each INTA). The interrupt vector address would be used by the bus master to service the interrupt.

NOTE

The MULTIBUS interface can support only one type of Bus Vectored Interrupt in a given system. However, the MULTIBUS interface can support Bus Vectored and Non-Bus Vectored Interrupts at the same time. At INIT time, the master must program the slave interrupt controller to the correct type.

Related Sections:

Functional Descriptions	2.3
Timing Specification Summary	3.2
Guidelines and Examples	5

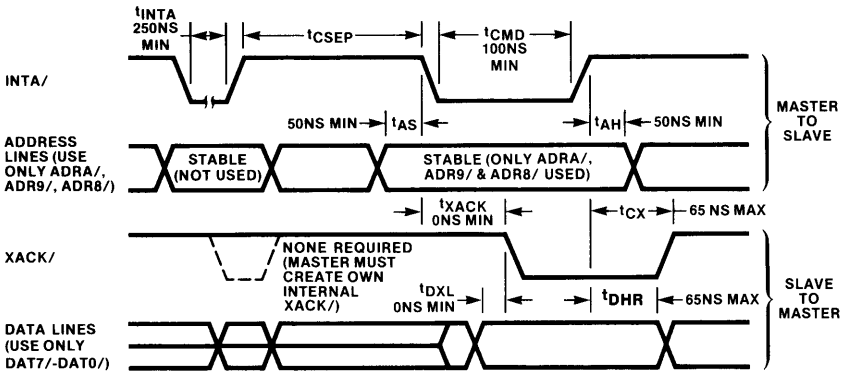


Figure 3-6. Bus Vectored Interrupt AC Timing

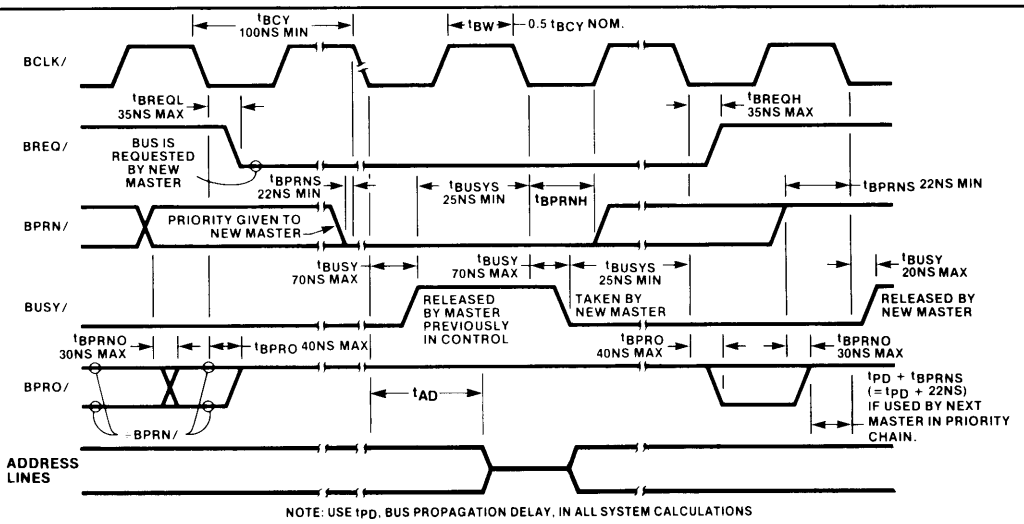


Figure 3-7. Bus Exchange AC Timing

3.2.5 BUS CONTROL EXCHANGES

A Bus Control Exchange takes control of the bus (i.e., the ability to do Bus Read, Write, and Interrupt Acknowledge operations) from one master and gives it to another master. See Section 2.4 for a functional description of this process.

For a master that does not use the bus signal CBRQ/(Common Bus Request) the timing specifications shown in figures 3-7 and 3-9 apply.

For a system using CBREQ/ (Common Bus Request) each master must also satisfy the following timing requirements (figure 3-8):

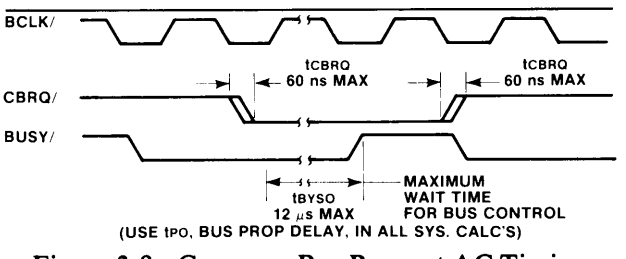


Figure 3-8. Common Bus Request AC Timing

Note that before "releasing the bus" (i.e., releasing BUSY/) the hold times, etc., of any ending cycle must still be met as per the previous sections of this chapter. Likewise, after "taking the bus" (i.e., driving BUSY/ low) it is necessary to satisfy all applicable set-up and other timing parameters for a cycle just beginning. See the functional description Section 2.5

3.2.5.1 SERIAL PRIORITY. For a system that uses a serial priority scheme (i.e., daisy chain BPRO/'s to BPRN/'s, see Section 2.4) the timing specifications shown in figure 3-9 apply.

3.2.5.2 PARALLEL PRIORITY. For a system that uses a parallel priority scheme (i.e., a central priority resolver, see Section 2.4) the system and CPM (cental priority module) timing specifications shown in figure 3-10 apply.

3.2.6 MISCELLANEOUS TIMING

The following timing diagrams (figures 3-11, 3-12, 3-13, 3-14) show the timing of Constant Clock (CCLK/), Command Separation (t_{CSEP}), Initialize (t_{INIT}), and Lock (LOCK/).

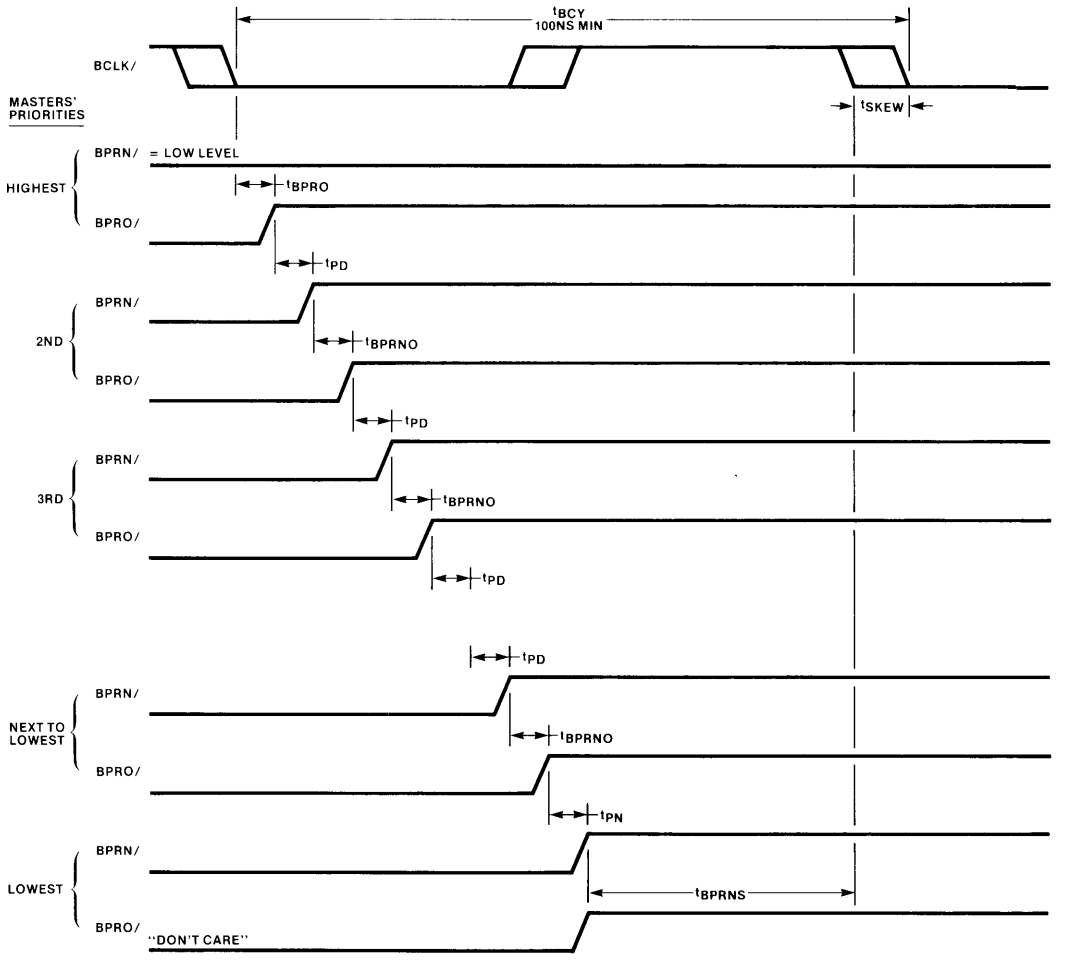


Figure 3-9. Serial Priority AC Timing

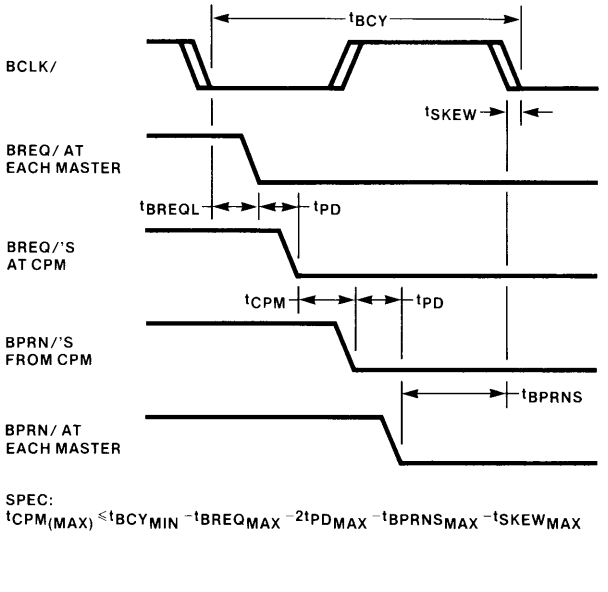


Figure 3-10. Parallel Priority AC Timing

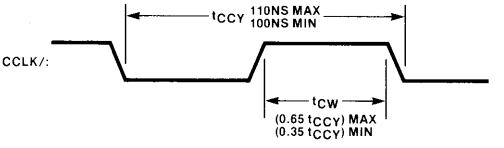


Figure 3-11. CCLK AC Timing

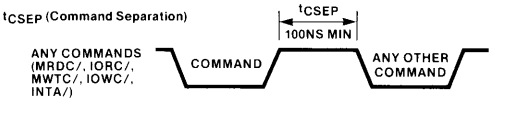


Figure 3-12. Command Separation AC Timing

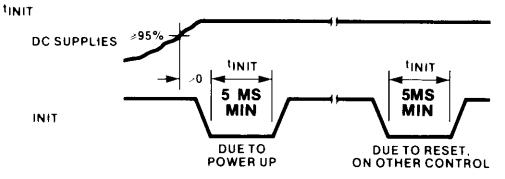


Figure 3-13. Initialize AC Timing

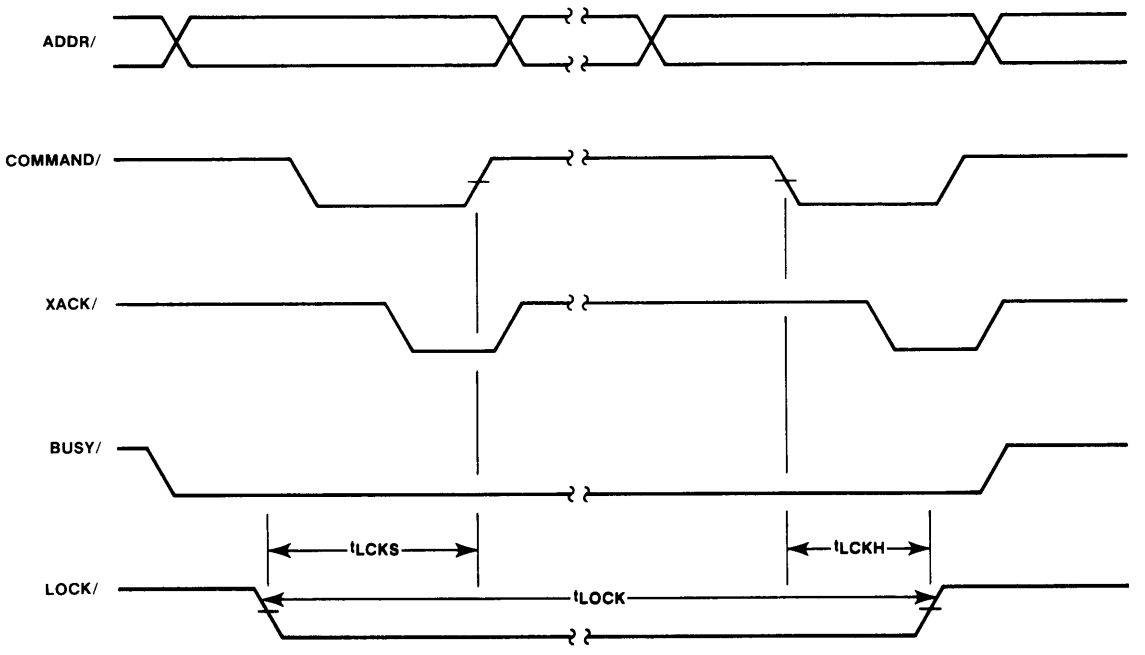


Figure 3-14. Lock AC Timing

3.2.7 POWER BACK-UP (OPTION)

For systems employing off-board Power Back-Up the following specifications apply (figure 3-15):

3.3 ELECTRICAL SPECIFICATIONS: RECEIVERS, DRIVERS, TERMINATIONS

This section provides non-timing specifications that are unique to each signal line or to groups of signal lines. Given are the requirements for the signal lines' receivers, drivers, and bus terminations. The locations of the receiver, driver, and termination are stated for each signal. Table 3-4 lists all of these specifications.

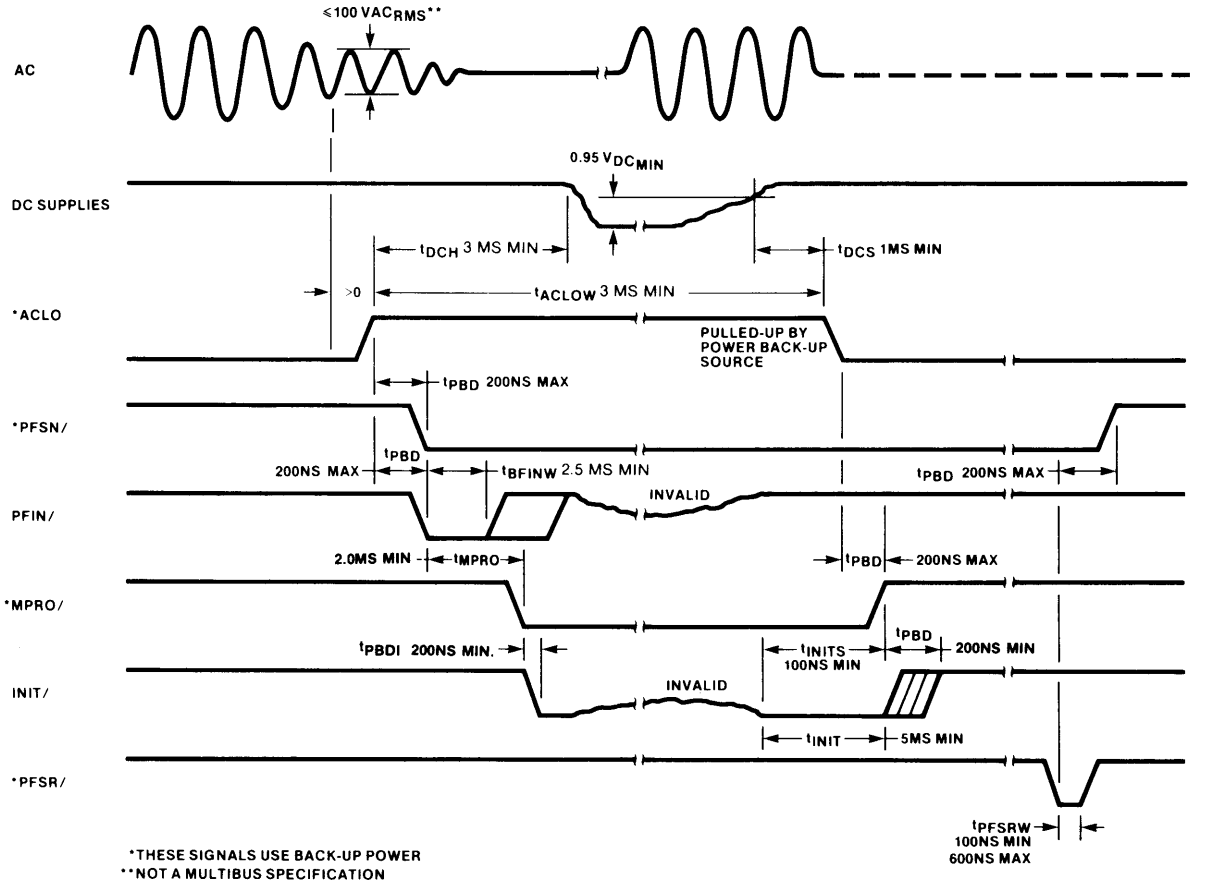


Figure 3-15. Power Backup AC Timing

Table 3-4. Bus Drivers, Receivers, and Terminations

	Driver 1,3					Receiver 2,3				Termination			
Bus Signals	**Location**	**Type**	I_{OL} Min_{ma}	I_{OH} $Min_{\mu a}$	C_O Min_{pf}	**Location**	I_{IL} Max_{ma}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	**Location**	**Type**	**R**	**Units**
DAT0/→DATF/ (16 lines)	Masters and Slaves	TRI	16	-2000	300	Masters and Slaves	-0.8	125	18	Motherboard	Pullup	2.2	KΩ
ADR0/-ADR17/, BHEN/ (25 lines)	Masters	TRI	16	-2000	300	Slaves	-0.8	125	18	Motherboard	Pullup	2.2	KΩ

Table 3-4. Bus Drivers, Receivers, and Terminations (Cont'd.)

Driver 1,3						Receiver 2,3				Termination			
Bus Signals	Location	Type	I_{OL} Min_{ma}	I_{OH} $Min_{\mu a}$	C_O Min_{pf}	Location	I_{IL} Max_{ma}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	Location	Type	R	Units
MRDC/,MWTC/	Masters	TRI	32	−2000	300	Slaves (Memory; memory-mapped I/O)	−2	125	18	Mother-board	Pull up	1	KΩ
IORC/,IOWC/	Masters	TRI	32	−2000	300	Slaves (I/O)	−2	125	18	Mother-board	Pull up	1	KΩ
XACK/	Slaves	TRI	32	−2000	300	Masters	−2	125	18	Mother-board	Pull up	510	Ω
INH1/,INH2/	Inhibiting Slaves	O.C.	16	—	300	Inhibited Slaves (RAM, PROM, ROM, Memory Mapped I/O)	−2	50	18	Mother-board	Pull up	1	KΩ
BCLK/	1 place (Master)	TTL	48	−3000	300	Master	−2	125	18	Mother-board	To +5V To GND	220 330	Ω Ω
BREQ/	Each Master	TTL	10	−200	60	Central Priority Module	−2	50	18	Central Priority Module (not req)	Pull up	1	KΩ
BPRO/	Each Master	TTL	3.2	−200	60	Next Master in Serial Priority Chain at its BPRN/	−3.2	100	18	(not req)			
BPRN/	Parallel: Central Priority Module Serial: Prev Masters BPRO/	TTL	3.2	−200	60	Master	−3.2	100		(not req)			
LOCK/	Master	TRI	32	−2000	300	All	−2	125	18	Mother-board	Pull up	1	KΩ
BUSY/,CBRQ/	All Masters	O.C.	20	—	300	All Masters	−2	50	18	Mother-board	Pull up	1	KΩ
INIT/	Master	O.C.	32	—	300	All	−2	50	18	Mother-board	Pull up	1	KΩ
CCLK/	1 place	TTL	48	−3000	300	Any	−2	125	18	Mother-board	To +5V To GND	220 330	Ω Ω
INTA/	Masters	TRI	32	−2000	300	Slaves (Interrupting I/O)	−2	125	18	Mother-board	Pull up	1	KΩ
INT0/ → INT7/ (8 lines)	Slaves	O.C.	16	—	300	Masters	−1.6	40	18	Mother-board	Pull up	1	KΩ
PFSR/	User's Front Panel	TTL	16	−400	300	Slaves, Masters	−1.6	40	18	Driver	Pull up	1	KΩ
PFSN/	Power Back-Up Unit	TTL	16	−400	300	Masters	−1.6	40	16	Driver	Pull up	1	KΩ
ACLO	Power Supply	O.C.	16	−400	300	Slaves, Masters	−1.6	40	18	Power Supply	Pull up	1	KΩ
PFIN/	Power Back-Up Unit	O.C.	16	−400	300	Masters	−1.6	40	18	Driver	Pull up	1	KΩ
MPRO/	Power Back-Up Unit	TTL	16	−400	300	Slaves Masters	−1.6	40	18	Driver	Pull up	1	KΩ

Table 3-4. Bus Drivers, Receivers, and Terminations (Cont'd.)

Driver 1,3						Receiver 2,3				Termination			
Bus Signals	**Location**	**Type**	**I_{OL} Min_{ma}**	**I_{OH} $Min_{\mu a}$**	**C_O Min_{pf}**	**Location**	**I_{IL} Max_{ma}**	**I_{IH} $Max_{\mu a}$**	**C_I Max_{pf}**	**Location**	**Type**	**R**	**Units**
MPRO/	Power Back-Up Unit	TTL	16	−400	300	Slaves Masters	−1.6	40	18	Driver	Pullup	1	KΩ
Aux Reset/	User's Front Panel	Switch to GND (Note 4)	–	–	–	Masters	−2	50		Note 5			

Notes:

1. Driver Requirements

   I_{OH} = High Output Current Drive
   I_{OL} = Low Output Current Drive
   C_O = Capacitance Drive Capability
   TRI = 3-State Drive
   O.C. = Open Collector Driver
   TTL = Totem-pole Driver

2. Receiver Requirements

   I_{IH} = High Input Current Load
   I_{IL} = Low Input Current Load
   C_I = Cap acitive Load

3. For Low and High Voltages specifications (see Section 3.1.1).

4. Recommend a 47 Ω resistor in series with switch.

5. Typically a 100 KΩ 5% to +5V and 10μf to ground on the board.

SECTION 4
MECHANICAL SPECIFICATIONS

4.0 INTRODUCTION

This section describes all the physical and mechanical specifications that a designer must concern himself with when designing a MULTIBUS backplane or when designing printed circuit boards that will plug into the MULTIBUS interface.

4.1 BACKPLANE CONSIDERATIONS

This section is a discussion of the things that the designer must consider when designing a MULTIBUS backplane.

4.1.1 BOARD TO BOARD RELATIONSHIPS

The following printed circuit board specifications must be adhered to when designing MULTIBUS compatible boards which are to operate in a .6 inch board to board spacing backplane.

a. *Board to Board Spacing* (L_C)-center to center of boards when plugged into backplane must be at least 0.6 inches ± .02.

b. *Board Thickness* (L_T)-the typical board thickness is .062 ± .005 inches.

c. *Component Lead Length* L_L-the length of the component leads below the printed circuit board can not exceed .093 inches.

d. *Component Height* (L_H)-the following equation is used to determine the maximum height of the components above the printed circuit board:

$L_H < L_C - L_T - L_L$

$L_H < .58" - .067" - .093"$

$L_H < .420$ inches (including board warpage)

Electrically conductive components require L_H to be decreased to .40 inches.

An example of a typical backplane and the components necessary to implement it are shown in figure 4-2.

CAUTION

This section contains only the mechanical specifications for designing a MULTIBUS interface. The designer must also take into consideration the electrical specifications in Section 3 and the termination specifications in Section 5.

4.1.2 MULTIBUS PIN ASSIGNMENTS

Printed circuit boards which are designed to interface to the MULTIBUS have two connectors which plug into the backplane. These connectors, P1 (Primary) and P2 (Auxiliary), have specific signal/pin assignments. Because of this, the designer must insure that the MULTIBUS backplane he designs is compatible (pin for pin) with these two connectors.

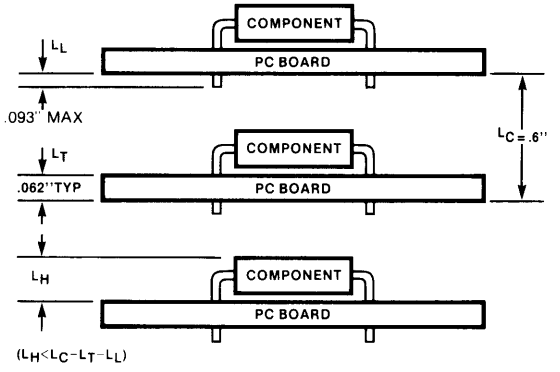


Figure 4-1. Multibus Backplane Card to Cage Separation

Tables 4-1 and 4-2 show the pin/signal assignments for the P1 and P2 connectors on the printed circuit boards.

The P2 connector signal/pin assignments are in two groups: the non-bussed pins (1-40) and the bussed pins (41-60). If a board does not require the signals on the non-bussed pins shown in Table 4-2, the design can use those pins for other uses. A board which does not follow the pin assignments shown will not be "slot independent" in a system but will require special backplane wiring. Because pins 41-60 are bussed across the backplane it is not recommended that any of the reserved pins be used for special signals.

4.2 MULTIBUS BOARD FORM FACTORS

Certain MULTIBUS characteristics must be taken into consideration when designing printed circuit boards that interface to it. The designer will ensure himself of MULTIBUS compatibility if the specifications discussed in this chapter are followed.

4.2.1 CONNECTOR NAMING AND PIN NUMBERING STANDARDS

The connectors on the printed circuit boards designed for the MULTIBUS interface should adhere to the following standards (see figure 4-3):

a. The connectors on the bus side of the board will be called P1, P2. P1 is the 86 pin main connector, and P2 is the 60 pin auxiliary connector.

b. Pins should be numbered with odd number pins on the component side of the board, and in ascending order when going counterclockwise around the board (as shown in figure 4-3).

c. The connectors on the non-bus side of the board will be called J1, J2, J3, etc. An attempt should be made to number these connectors in ascending order when going clockwise around the board (as viewed from component side).

4.2.2 STANDARD OUTLINE OF PRINTED WIRING BOARD

Figure 4-4 shows the standard outline for MULTIBUS - compatible boards (Printed Wire Boards and Printed Circuit Boards). The non-bus edge of the board is not restricted, and could be designed as discussed in section 4.2.4. The remainder of the board including connectors P1 and P 2 must adhere to the dimensions shown in figure 4-4.

4.2.3 BUS CONNECTORS

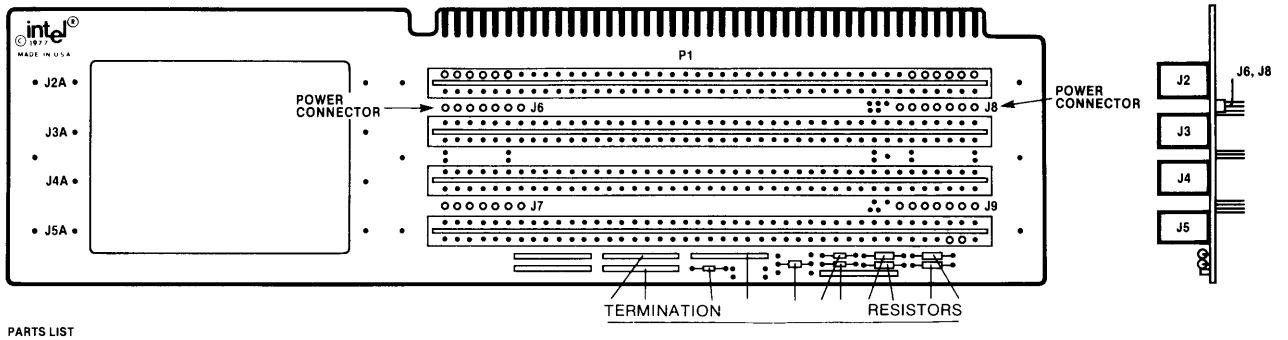
The MULTIBUS backplane has connectors that mate to the P1 (43/86 pin) board edge connector. The backplane uses 43/86 pin on 0.156" centers connectors (INTEL MDS-985). Table 4-3 is a list of compatible connectors.

The backplane uses a 30/60 pin on 0.1" centers connector (INTEL MDS-980) to mate with the P2 auxiliary board edge connector. Table 4-3 is a list of compatible connectors. See Section 4.2.6 for connector key slot information.

Table 4-4 is a list of vendor addresses, telephone numbers, and TWX numbers. The information is for convenience only. Intel does not represent these vendors, guarantee availability, or guarantee quality of their products.

CAUTION

Insure that the connector you are ordering fits your design needs. Verify part numbers with vendor.



PARTS LIST

1 PWB TERMINATION BACKPLANE
2 7 POST WAFER CONNECTORS (.156" PIN CENTERS) (J6 AND J8)
4 EDGE BOARD CONNECTORS, 43/86 PINS ON .156" CENTERS (J2-J5)
12 WIRE WRAP POSTS
4 10 PIN, 2.2K, 9 RES, 1.5W RESISTOR PACKS (RP1-RP4)
1 10 PIN, 1K, 9 RES, 1.5W RESISTOR PACK (RP5)
1 10 PIN, 1.1K, 9 RES, 1.5W RESISTOR PACK (RP6)
1 1K RESISTOR, 1/8W, ±5% (R1)
1 2.2K RESISTOR, 1/8W, ±% (R5)
2 220Ω RESISTORS, 1/4W, ±5% (R9, R11)
2 330Ω RESISTORS, 1/4W, ±5% (R10, R12)
2 510Ω RESISTORS, 1/8W, ±5% (R7, R8)

Figure 4-2. Typical MULTIBUS Backplane

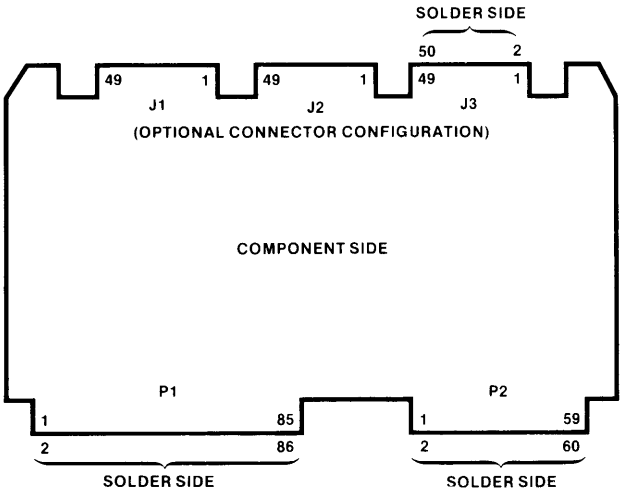


Figure 4-3. Connector and Pin Numbering

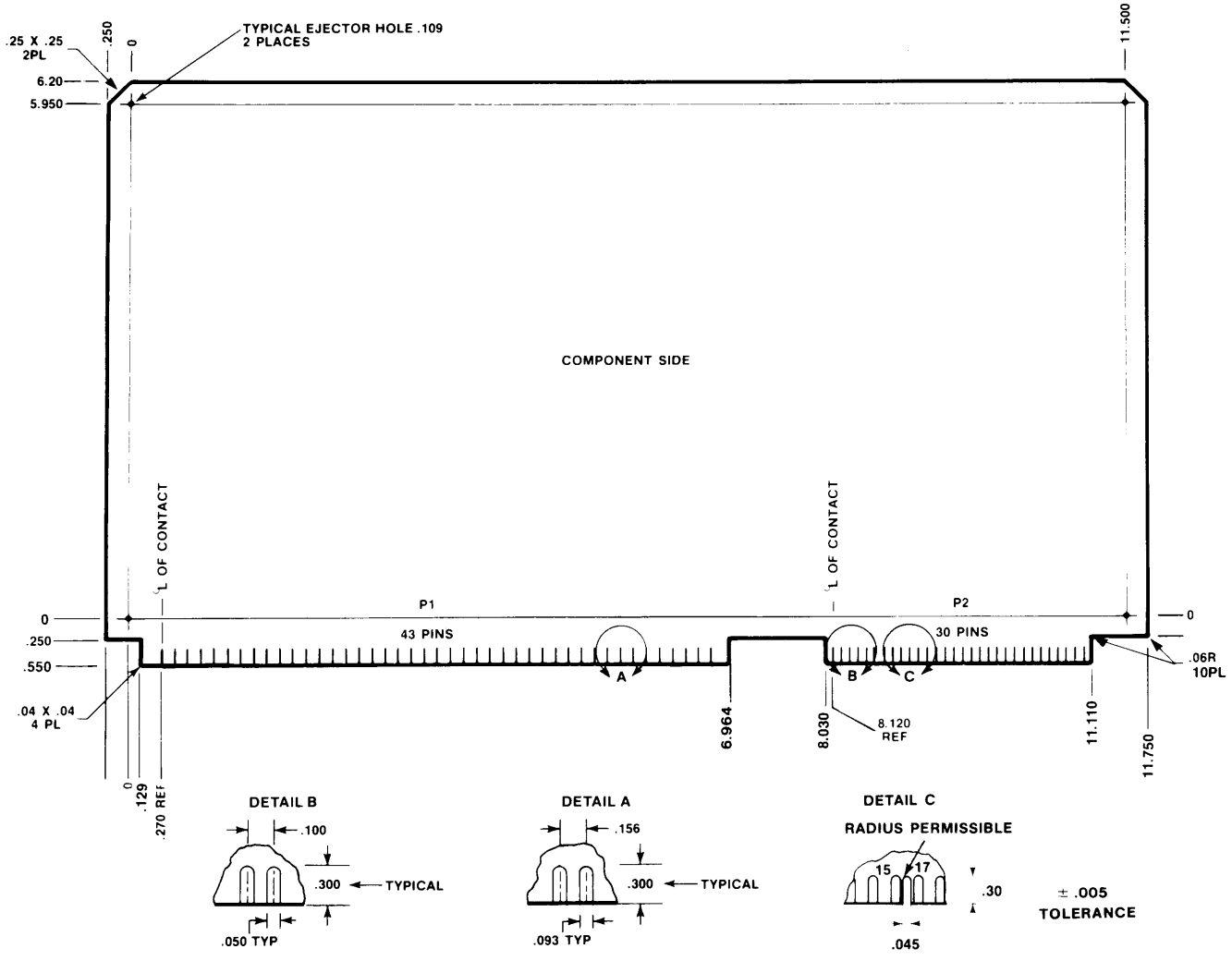


Figure 4-4. Standard Printed Wiring Board Outline

Table 4-1. Pin Assignment of Bus Signals on Multibus Board Connector (P1)

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+ 5Vdc	4	+5V	+ 5Vdc
	5	+5V	+ 5Vdc	6	+ 5V	+ 5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9		Reserved, bussed	10		Reserved, bussed
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 disable RAM
BUS CONTROLS AND ADDRESS	25	LOCK/	Lock	26	INH2/	Inhibit 2 disable PROM or ROM
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Intr Acknowledge	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	−12V	−12Vdc	80	−12V	−12Vdc
	81	+5V	+ 5Vdc	82	+5V	+ 5Vdc
	83	+5V	+ 5Vdc	84	+5V	+ 5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Table 4-2. P2 Connector PIN Assignment of Bus Signals

(COMPONENT SIDE)			(CIRCUIT SIDE)		
PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	GND	Signal GND	2	GND	Signal GND
3	5VB	+ 5V Battery	4	GVB	+ 5V Battery
5		Reserved, not bussed	6	EEVPP	E^2 PROM Power
7	-5VB	- 5V Battery	8	-5VB	- 5V Battery
9		Reserved, not bussed	10		Reserved, not bussed
11	12VB	+12V Battery	12	12VB	+12V Battery
13	PFSR/	Power Fail Sense Reset	14		Reserved, not bussed
15	-12VB	-12V Battery	16	-12VB	-12V Battery
17	PFSN/	Power Fail Sense	18	ACLO	AC Low
19	PFIN/	Power Fail Interrupt	20	MPRO/	Memory Protect
21	GND	Signal GND	22	GND	Signal GND
23	+15V	+15V	24	+15V	+15V
25	-15V	-15V	26	-15V	-15V
27	PAR1/	Parity 1	28	HALT/	Bus Master HALT
29	PAR2/	Parity 2	30	WAIT/	Bus Master WAIT STATE
31	PLC	Power Line Clock	32	ALE	Bus Master ALE
33			34		Reserved, not bussed
35		Reserved, not bussed	36	BD RESET/	Board Reset
37			38	AUX RESET/	Reset switch
39			40		Reserved, not bussed
41			42		
43			44		
45		Reserved, bussed	46		Reserved, bussed
47			48		
49			50		
51			52		
53			54		
55	ADR16/	Address	56	ADR17/	Address
57	ADR14/	Bus	58	ADR15/	Bus
59		Reserved, bussed	60		Reserved, bussed

Notes:
1. PFIN, on slave modules, if possible, should have the option of connecting to INT0/ on P1.
2. All undefined pins are reserved for future use.

4.2.4 NON-BUS EDGE OF PRINTED WIRING BOARD

The bus side of the standard PWB is fixed as to dimensions, form factors, and connectors. The non-bus edge is not fixed. For consistency, however, it is recommended that one of the following types be used whenever possible:

a. One 50-pin connector
b. Two 50-pin connectors
c. Three 50-pin connectors
d. Two 50-pin connectors and one 26-pin connector.
e. Five 26-pin connectors
f&g. One 26-pin and One 50-Pin connector
h. One 100-pin connector.

Figure 4-5 shows the different connector combinations.

Mating connectors for these board-edge connectors are discussed in section 4.2.5.

4.2.5 NON-BUS EDGE CONNECTORS

This section describes the mating connectors recommended for use with the board edge connectors described in section 4.2.4. Table 4-5 is a list of these connectors. The pin conventions on some of the connectors may not be consistent with the recommended standard. Whenever possible, connectors with the recommended standard should be used.

Table 4-3. Compatible Bus Connectors

Function	# Of Pins	Centers Inches	Connector Type	Vendor	Vendor #	Intel #
Multibus Connector (P1)	43/86	0.156	Soldered[1]	VIKING ELFAB	2KH43/9AMK12 BS1562D43PBB	102247-001
Multibus Connector (P1)	43/86	0.156	Wire wrap[1,2]	ELFAB ELDAC	BW1562D43PBB 3370860540201	102248-001
				ELFAB EDAC	BW1562A43PBB 337086540202	102273-001[1]
Auxiliary Connector (P2)	30/60	0.1	Soldered[1]	ELFAB EDAC	BS1020A30PBB 345060524802	102238-001
Auxiliary Connector (P2)	30/60	0.1	Wire wrap[1,2]	TI VIKING	H421121-30 3KH30/9JNK	N/A[3]
				EDAC ELFAB	345060540201 BW1020D30PBB	102241-001

Notes:
1. Connector heights are not guaranteed to conform to Intel packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to Intel packaging equipment.
3. With mounting ears with .128 mounting holes.

Table 4-4. Vendor Information

CDC CONNECTOR DIVISION
31828 W. LaTienda Drive
Westlake Village, CA 91361

213-889-3535
TWX 910-494-1224

VIKING INDUSTRIES, INC.
21001 Nordhoff Street
Chatsworth, CA 91311

213-341-4330
TWX 910-494-2094

Connector Systems
TEXAS INSTRUMENTS, INC.
34 Forest Street
Attleboro, MA 02703

617-222-2800

AMP INCORPORATED
P.O. Box 3608
Harrisburg. PA 17105

717-564-0100
TWX 510-657-4110

T&B ANSLEY Subsidiary of Thomas & Betts Corp.
3208 Humbolt Street
Los Angeles, CA 90031

213-223-2331
TWX 910-321-3938

STANFORD APPLIED ENG., INC.
340 Martin Street
Santa Clara, CA 95050

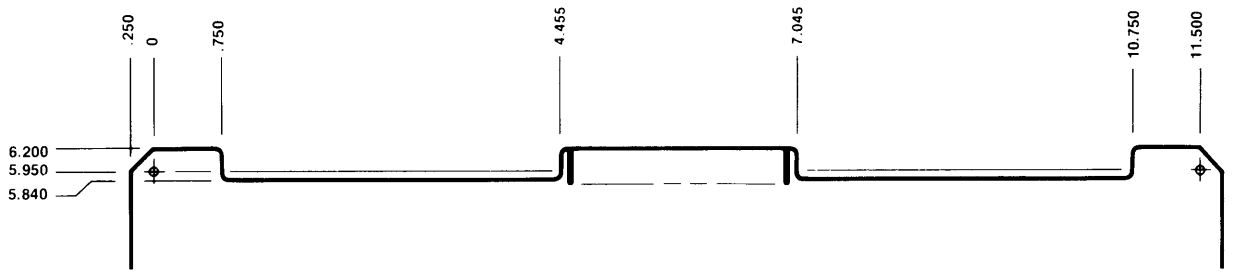
408-243-9200
TWX 910-338-0132

3M Connectors
Electronics Products Div.,
Bldg. 223-4E, 3M COMPANY, 3M Center
St. Paul, MN. 55101

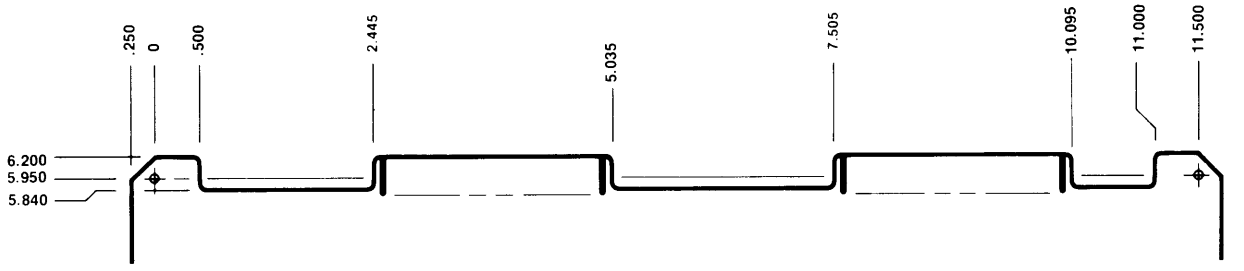
612-733-1110

ITT CANNON ELECTRIC
666 E. Dyer Road
Santa Ana, CA 92702

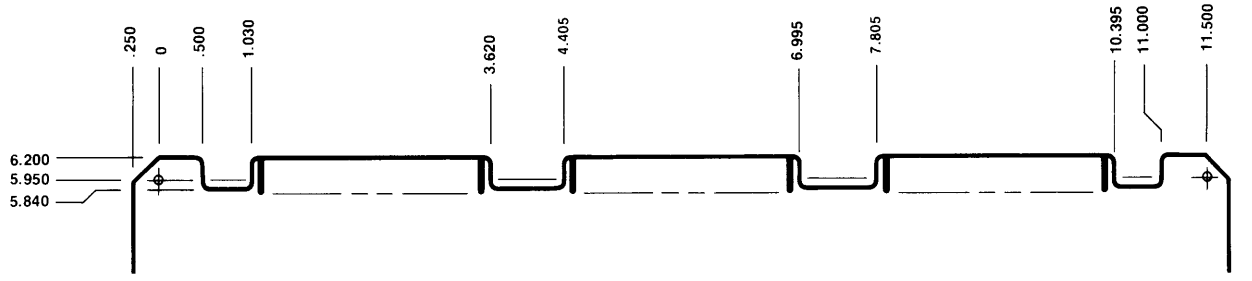
800-854-3573
800-432-7063 (in CA)



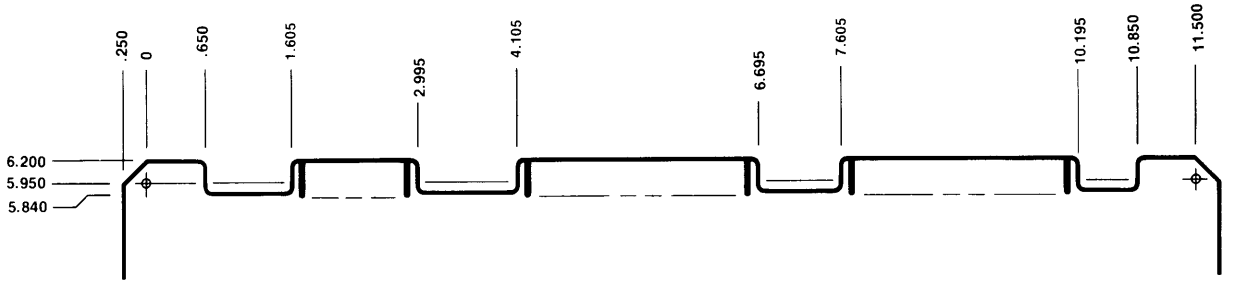
A. One 50-Pin Connector



B. Two 50-Pin Connectors



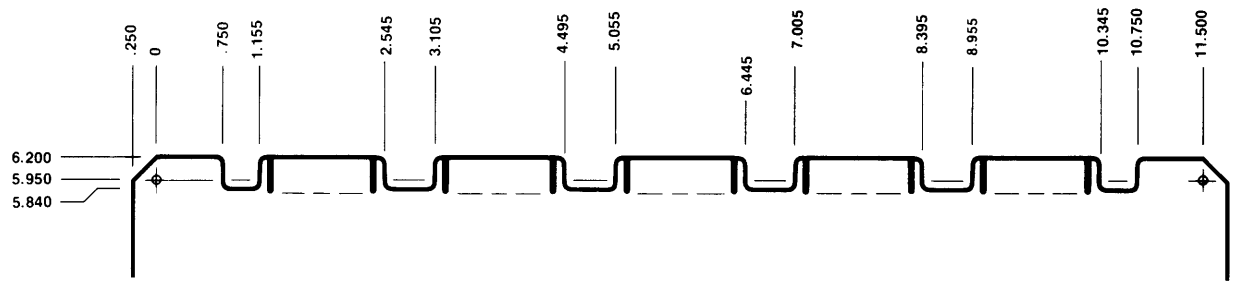
C. Three 50-Pin Connectors



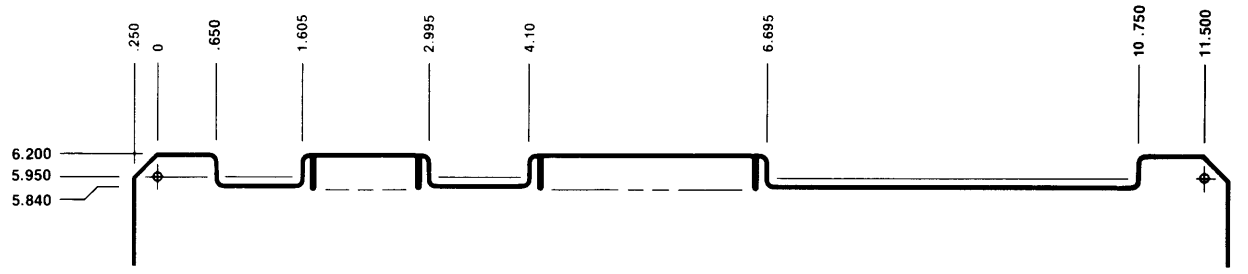
D. Two 50-Pin And One 26-Pin Connectors

NOTE:
1. All dimensions are Referenced to reference tooling hole. See Fig. 4-4.
2. All dimensions are in inches and unless otherwise specified tolerances are: .xx±.01, .xxx±.005

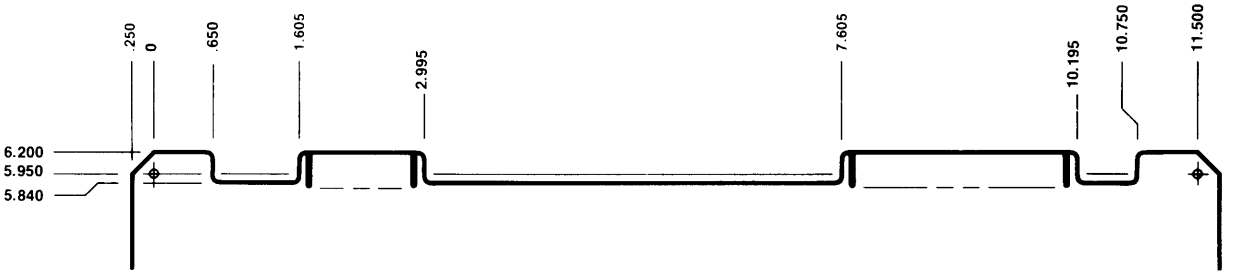
Figure 4-5. Non-Bus Edge PWB Connector Examples



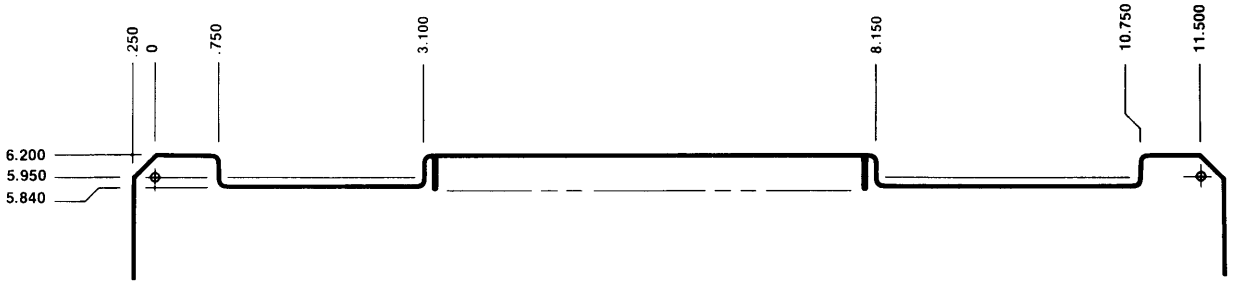
E. Five 26-Pin Connectors



F. One 26-Pin And One 50-Pin Connector



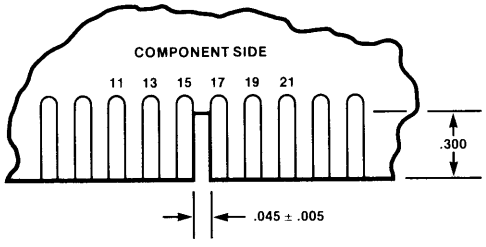
G. One 26-Pin And One 50-Pin Connector (Centered)



H. One 100-Pin Connector

NOTE:
1. All dimensions are Referenced to reference tooling hole. See Fig. 4-4.
2. All dimensions are in inches and unless otherwise specified tolerances are: .xx±.01, .xxx±.005

Figure 4-5. Non-Bus Edge PWB Connector Examples (Cont.)



A list of vendors addresses, telephone numbers, and TWX numbers can be found in table 4-4.

4.2.6 Connector Key Slots

A connector keying slot on the auxilliary connector (P2) is required on all boards employing external (i.e., off-board) battery back-up. The slot is located between pins 15-16 and 17-18 as shown in figure 4-6.

CAUTION

Insure that the connector you are ordering fits your design needs. Verify part numbers with vendors.

Table 4-5. Top Edge Compatible Connector Hardware (Recommended)

# OF PINS	CENTERS (inches)	CONNECTOR TYPE	VENDOR	VENDOR PART #	INTEL PART #
25/50	0.1	FLAT CRIMP	3M 3M AMP ANSLEY SAE	3415-0000 WITH EARS 3415-0001 W/O EARS 88083-1 609-5015 SD6750 SERIES	iSBC-956 (CABLE ASSY.)
13/26	0.1	FLAT CRIMP	3M AMP ANSLEY SAE	3462-0001 CRIMP 88106-1 609-2615 SD6726 SERIES	iSBC-955 (CABLE ASSY.)
25/50	0.1	SOLDERED	AMP VIKING TI	2-583485-6 3VH25/1JV5 H312125	N/A
13/26	0.1	SOLDERED	TI AMP	H312113 1-583485-5	N/A
43/86	0.156	SOLDERED	CDC MICRO PLASTICS ARCO VIKING	VPB01E43D00A1 MP-0156-43-BW-4 AE443WP1 LESS EARS 2VH43/1AV5	N/A
25/50	0.1	WIREWRAP	TI VIKING CDC ITT CANNON	H311125 3VH25/1JND5 VPB01B25D00A1 EC4A050A1A	N/A
13/26	0.1	WIREWRAP	TI	H311113	N/A
50/100	0.1	SOLDER TAIL	VIKING	3VH50/1JN5	MDS-990
		SOLDER PAK (RAYCHEM)	CDC	VPB04B50E00A1E	N/A

Notes:
1. Connector heights are not guaranteed to conform to Intel packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to Intel packaging equipment.

Note: See Table 4-4 for vendor addresses, telephone numbers and TWX numbers.

SECTION 5
DESIGN GUIDELINES AND SYSTEM APPLICATIONS

5.0 INTRODUCTION

Section 5 will give the design engineer examples of various MULTIBUS interface circuits. The MULTIBUS can interface to basically two classifications of bus modules: 1) Masters - modules which generate commands, and 2) Slaves - modules which respond to commands. Each of these modular types is discussed, and detailed implementation examples are given. Table 5-1 is a list of the topics covered in this section.

Table 5-1. Location of Key Information

Summary Information	Section
Introduction	5.0
Master Design Examples	5.1
Slave Design Example	5.2
Bus Exchange Implementation Examples	5.3
Power Failure Backup Methods	5.3
Design Recommendation Summary	5.5
AC and DC Specification Recommendation	5.6
Bus Termination Considerations	5.7
Miscellaneous Considerations	5.8

5.1 MASTER DESIGN EXAMPLE

A MULTIBUS Master is a bus module which can access bus resources. The MDS CPU and SBC 80/30 are examples of Master Modules.

A MULTIBUS Master interface can be divided into five basic elements:

1. Control
2. Address
3. Data
4. Interrupts
5. Bus exchange

Figure 5-1 shows the basic interface of each element to the MULTIBUS interface. A brief explanation is given, followed by a detailed implementation.

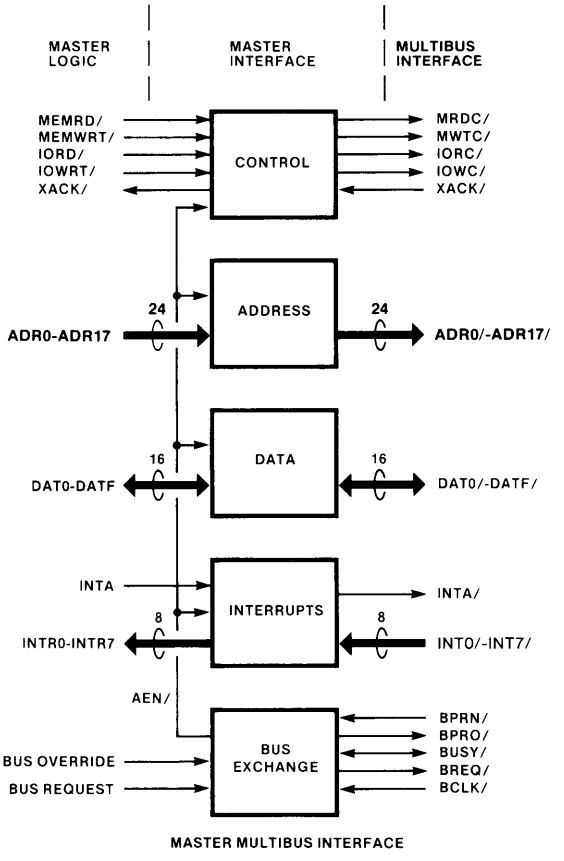


Figure 5-1. Master Multibus Interface

5.1.1 CONTROL LOGIC

The control logic consists of a variety of signals which control MULTIBUS operations. These signals are:

1) Command lines - MRDC/
MWTC/
IORC/
IOWC/

2) Transfer acknowledge - XACK/

3) C CLOCK - CCLK/

4) Initialize - INIT/

5) LOCK - LOCK/

5.1.1.1 BUS COMMAND LINES Figure 5-2 shows two types of MULTIBUS command drivers which provide high drive and three-state characteristics. Important attributes of command drivers are:

1. Glitch-free when tri-state is enabled or disabled.
2. When changing state, the over/under shoot cannot go back through the logic level it went through last.
3. Capacitive coupling of other signals must be minimized.
4. The signal trace from driver to bus must be as short as possible. Total length should be less than 4 inches (10cm).

The AC timing of the command lines is shown in Figure 5-6.

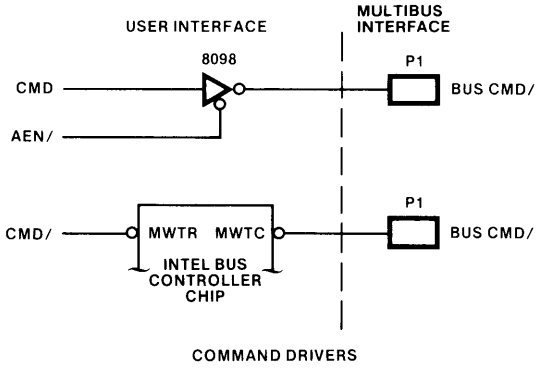


Figure 5-2. Command Drivers

5.1.1.2 CCLK This clock provides a MULTIBUS timing source which can be used by slave modules to generate internal timing such as XACK/. The design example is found in Figure 5-3. The master derives a 2X clock source which is divided by 2 using a 7474 Flip-flop. This is done to provide a 50% duty cycle to the clock driver chip (74S140). The output of the clock driver must go to a jumper so that the user has the option to disconnect the signal if another source is available. The AC characteristics are shown in Figure 5-6.

NOTE

BCLK and CCLK may be derived from the same source but must have separate bus drivers. Also the two clocks should be 180° out of phase to reduce noise on the system bus.

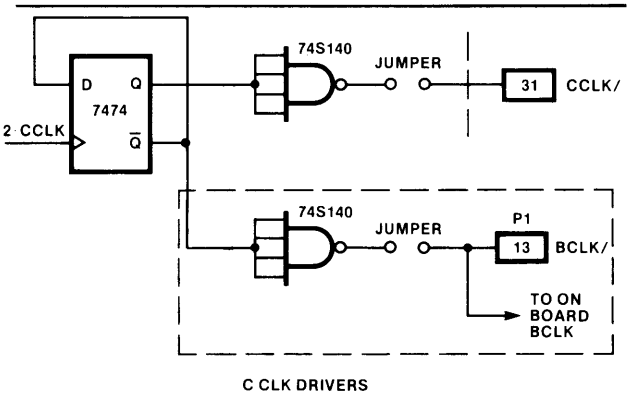


Figure 5-3. C CLK DRIVERS

5.1.1.3 TRANSFER ACKNOWLEDGE The Transfer Acknowledge signal (XACK/) informs the MULTIBUS master that the operation it required on the bus is completed. The transfer acknowledge (XACK/) circuitry shown in Figure 5-4 is a simple negative true AND gate (74S32). The XACK/ signal is gated through (and is inverted) only if the MULTIBUS master has control (AEN/ is active, see Bus Exchange - Section 5.1.5.). The trace routing of XACK/ on the PC board should avoid command and clock lines to minimize capactive coupling, and the trace length should be as short as possible. The important AC parameters are shown in Figure 5-6.

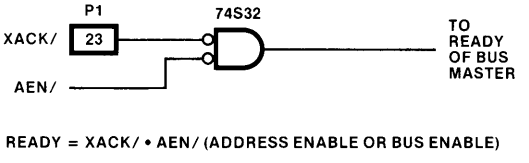


Figure 5-4. XACK/ Design Example

5.1.1.4 INITIALIZATION The initialize signal (INIT/) puts the system into a known state of operation. It consists of two parts; a power up reset source and a bus receiver for INIT/ as shown in Figure 5-5. The power up reset circuit can be an RC network into a hysteresis receiver. The time from +5 turning on until the hysteresis input reaches V_{IH} should exceed 500ms after all the power supplies are within spec. The output of the hysteresis gate is buffered by an open collector driver and connected to the MULTIBUS INIT/ pin. The bus master must also receive the INIT/ through a buffer to reset itself.

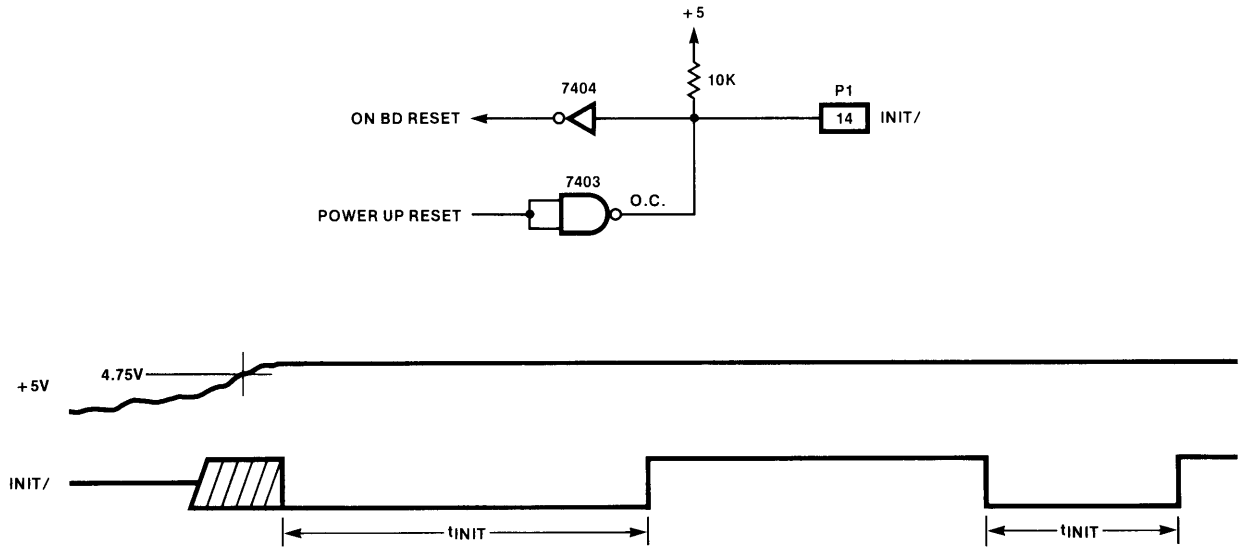


Figure 5-5. Initialize Logic

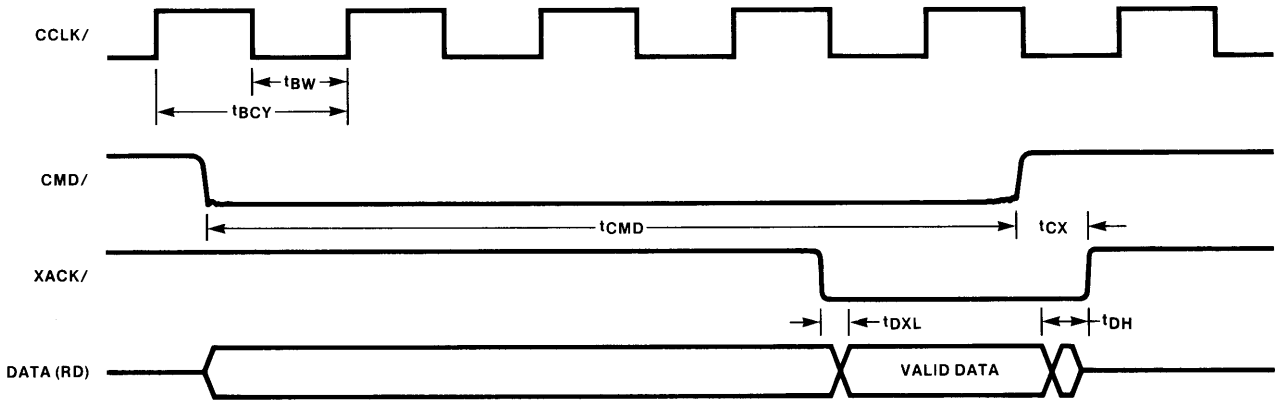


Figure 5-6. Control Logic AC Characteristics

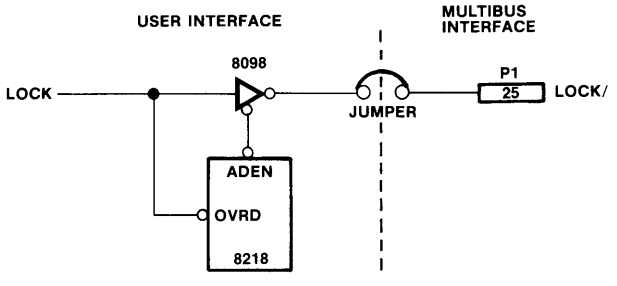


Figure 5-7. LOCK/ Design Example

5.1.1.5 LOCK. The Lock signal (LOCK/) informs all modules on the bus that the master has locked the bus for back-to-back cycles on the bus. Figure 5.7 shows a design example for a master. The jumper is provided to allow use with older boards which had advanced acknowledge (AACK/) on P1-25.

5.1.2 ADDRESS LOGIC

The address logic controls the MULTIBUS address lines, ADR0/ - ADR17/. Two different types of address logic will be discussed. The first example uses unidirectional drivers. These drivers are used on masters which do not permit access to on board

resources such as the iSBC 80/20 or MDS-800 CPU Module. The second example uses bidirectional drivers that allow on board resources to be accessed from the MULTIBUS interface. The iSBC 86/12 and iSBC 80/30 are examples of masters which permit access of on board RAM (Dual Port) from the processor as well as from the MULTIBUS interface.

5.1.2.1 UNI-DIRECTIONAL DRIVERS. The MULTIBUS interface requires three-state drivers on the address lines. Figure 5-8 provides a straight forward design for masters which only drive the address lines (no dual port memory). The buffers are enabled only if the master has control of the bus (AEN/ active, see Bus Exchange).

5.1.2.2 Bi-Directional Drivers. For masters which drive and receive the address lines, bidirectional drivers are used. The example given in Figure 5-9 is part of a dual port memory. The buffers are enabled and drive the bus if the master has control of the bus (AEN/ active). The buffers are enabled and receiving if the MULTIBUS interface has addressed the dual port memory and the dual port controller has enabled the dual port slave RQT/ signal. The AEN/ and dual port slave RQT/ are mutually exclusive signals.

5.1.2.3 Address Line Requirements. The address drivers should be as close to the bus as possible to minimize capacitive coupling on the bus address lines. Figure 5-10 shows the AC parameters associated with the address lines. The most important parameters are set-up times and hold times. In order to guarantee the 50ns of MULTIBUS address set-up time (relative to command), the following set-up time must be provided on the master.

$t_{on\ BD\ set\text{-}up}$ = address driver enable delay (max) − CMD driver delay (min) + bus settle time + bus propagation + $t_{set\text{-}up}$ (min - MULTIBUS spec).
= (30—2 + 2 + 2 + 50)ns
= 82ns

$t_{on\ BD\ hold}$ = − address driver delay (min) + CMD driver Delay (max) + t_{hold} (min MULTIBUS spec)
= −2 + 30 + 50ns
= 78ns

5.1.3 DATA LOGIC

The MULTIBUS data lines require three-state drivers. Two examples are given; one is for an 8 bit data system and the second is for a 16 bit data system.

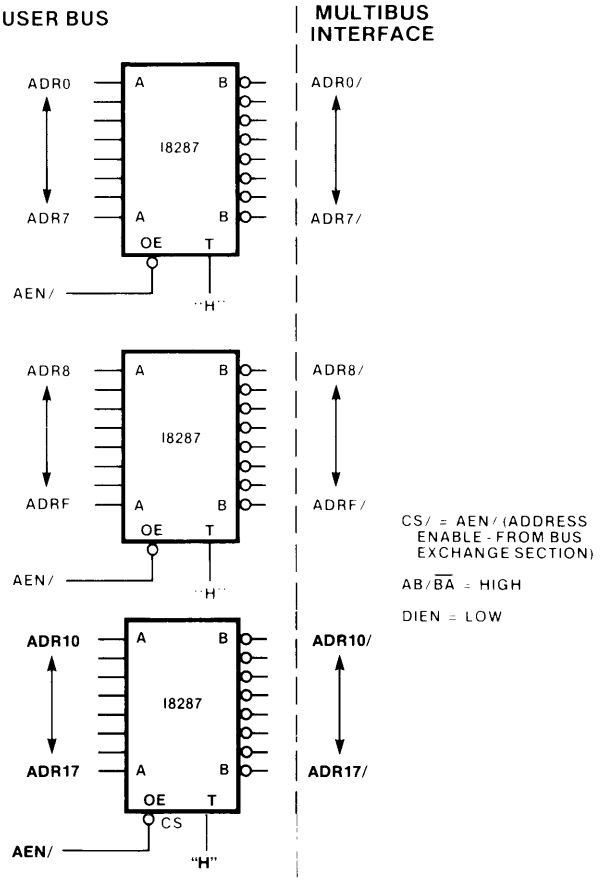


Figure 5.8 24 Bit Uni-Directional Bus Drivers

5.1.3.1 8-BIT DATA SYSTEM. The 8 bit data system example is shown in Figure 5-11. The chip select is controlled by AEN/ (address enable), and the direction is controlled by the unbuffered bus read command or by the S1 term of an 8085 micro processor.

5.1.3.2 16-Bit Data System. The 16 bit data system example is shown in Figure 5-12. In the 16 bit system there are 3 sets of buffers; the lower data buffers which buffer DAT0-DAT7, the upper data buffers which buffer DAT8-DATF, and the swap byte buffer which takes the data from DAT0-DAT7 on the MULTIBUS interface and puts it on the on board data bus, D8-DF.

The data buffers are controlled by the state of three signals: Byte High Enable, (BHEN/), which controls the high data byte buffer; Address Bit 0 (ADR0/), which controls the low data byte buffer; and address enable, (AEN/), which indicates that the master has

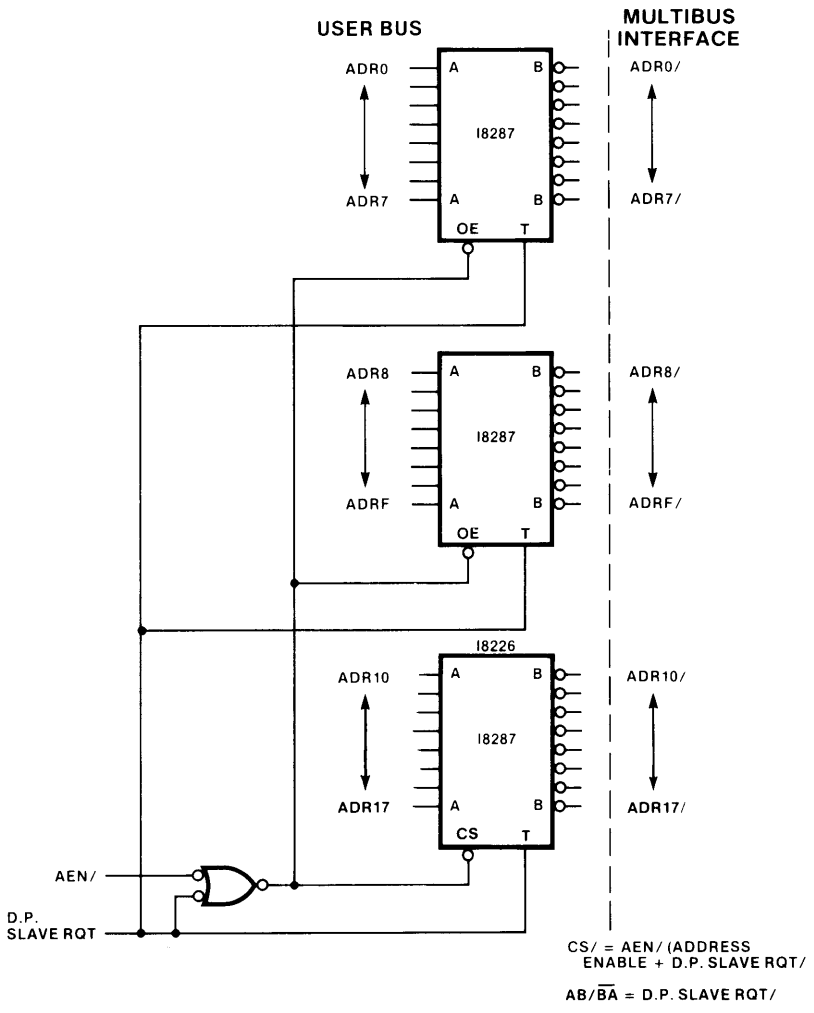


Figure 5-9. 24 Bit Bidirectional Address Bus Drivers

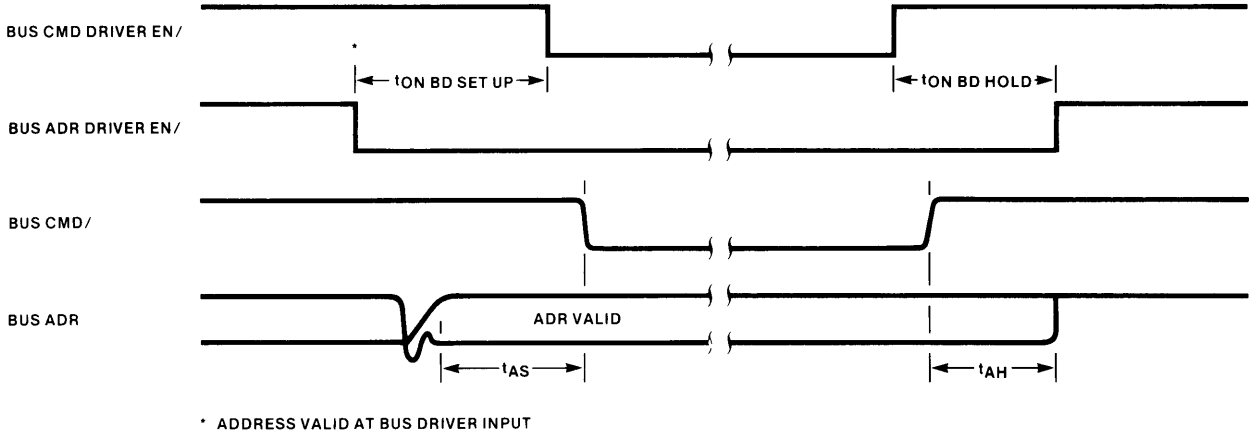


Figure 5-10. Address Timing

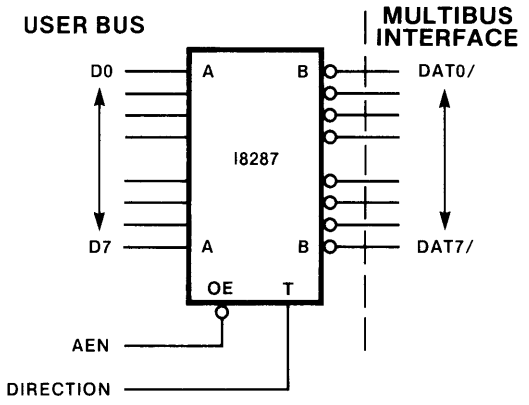


Figure 5-11. 8 Bit Data Drivers

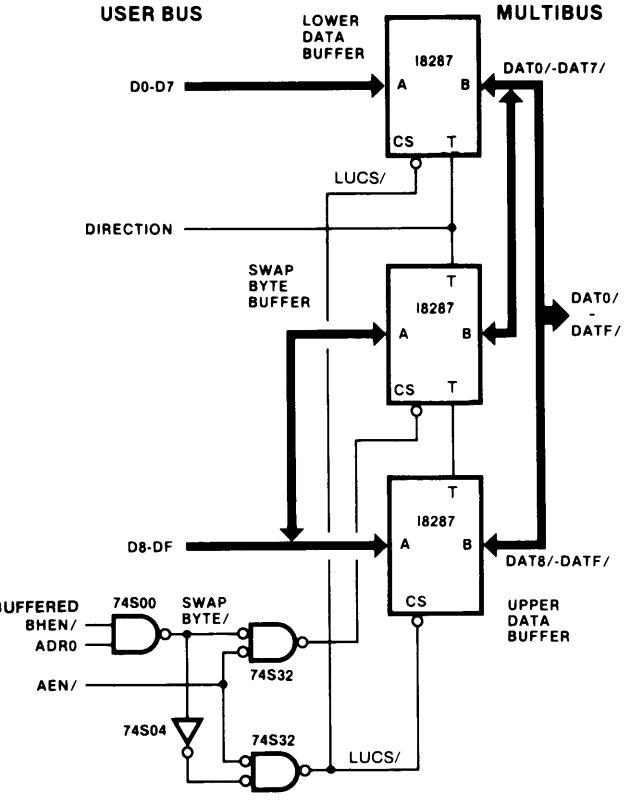


Figure 5-12. 16/8 Bit Data Drivers

MULTIBUS control. ADR0/ is equivalent to Byte Low Enable (BLEN). Figure 5-13 shows how 16 bit and 8 bit operations occur, if assumed that AEN/ is always active. BHEN/ and ADR0/ must adhere to address A.C. parameters.

Two control signals must be derived for each of the data buffers, the chip select and the direction. The direction for all three buffers is the same, and identical to the 8 bit data system. The truth tables for each of the chip selects shown in table 5-2, are derived from information shown in Figure 5-12.

The CS for the swap byte buffer is:

swap byte = BHEN/ · ADR0 (Table 5-2c)

swap byte CS = AEN · swap byte

A 16 bit master will ignore the other byte of its 16 bit data word during a byte operation. This permits use of the don't care terms in tables 5-2a and 5-2b which make the two tables equivalent. The CS term for the Lower and Upper data buffers (LU CS/) is the same.

LU CS/ = (BHEN/ • ADR0) = swap byte (Table 5-2a)

LU CS/ = swap byte • AEN/

5.1.3.3. DATA BUFFER REQUIREMENTS.

The important A.C. parameters associated with the data buffers are shown in Figure 5-14. The set up and hold time calculations are as shown:

$t_{on\ BD\ hold}$ = CMD driver delay (max)- address driver delay (min)
= t_{hold} (min-MULTIBUS spec)
= 30 − 2 + 50
= −78ns

$t_{on\ DB\ set\text{-}up}$ = Address driver enable delay (max)-
CMD driver delay (min)
+ bus settle time + bus propagation
+ $t_{set\text{-}up}$ (min-MULTIBUS spec)
= 30ns − 2 + 5 + 3 + 50
= 86ns

The data buffers should be located on the P.C. board as close as possible to the bus connectors in order to minimize trace distance.

NOTE

All 8 bit data operations must occur over the D0-D7 (lower) MULTIBUS data path to accommodate 8/16 bit systems.

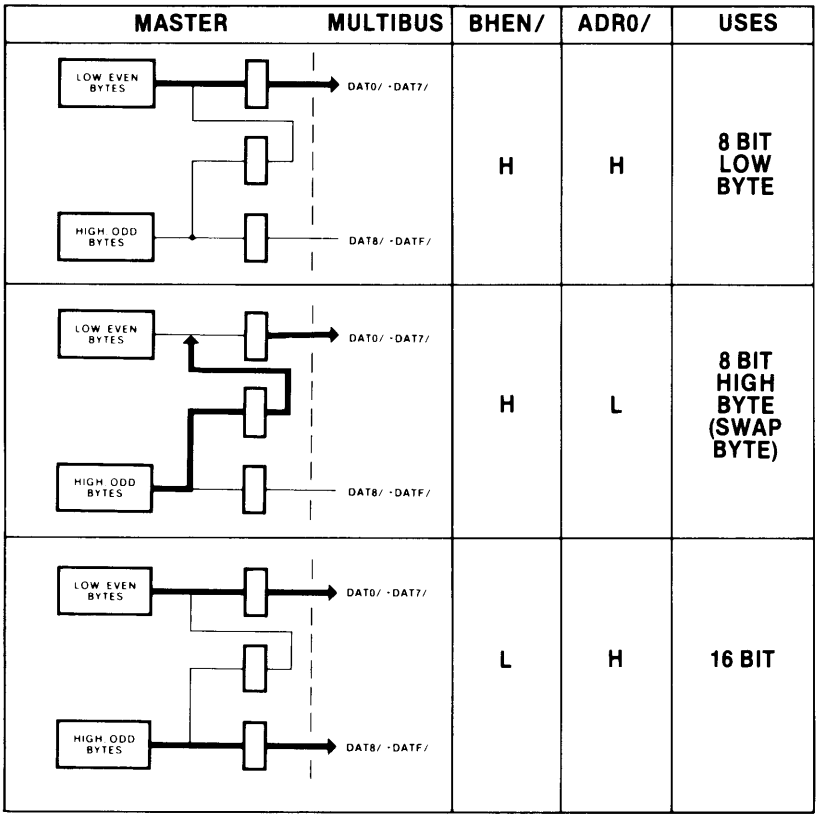


Figure 5-13. Memory-Operation (Master)

Table 5-2. Data Buffer Chip Select Truth Table

BHEN/ \ ADR0/ = BLEN	L	H
L	X	L
H	H	L

CS/ FOR BUFFER DAT0-DAT7 (A)

BHEN/ \ ADR0/ = BLEN	L	H
L	L	L
H	X	X

CS/ FOR BUFFER DAT8-DATF (B)

BHEN/ \ ADR0/ = BLEN	L	H
L	H	H
H	L	H

CS/ FOR SWAP BYTE BUFFER (C)

L = ⩽ 0.8V
H = ⩾ 2.0V

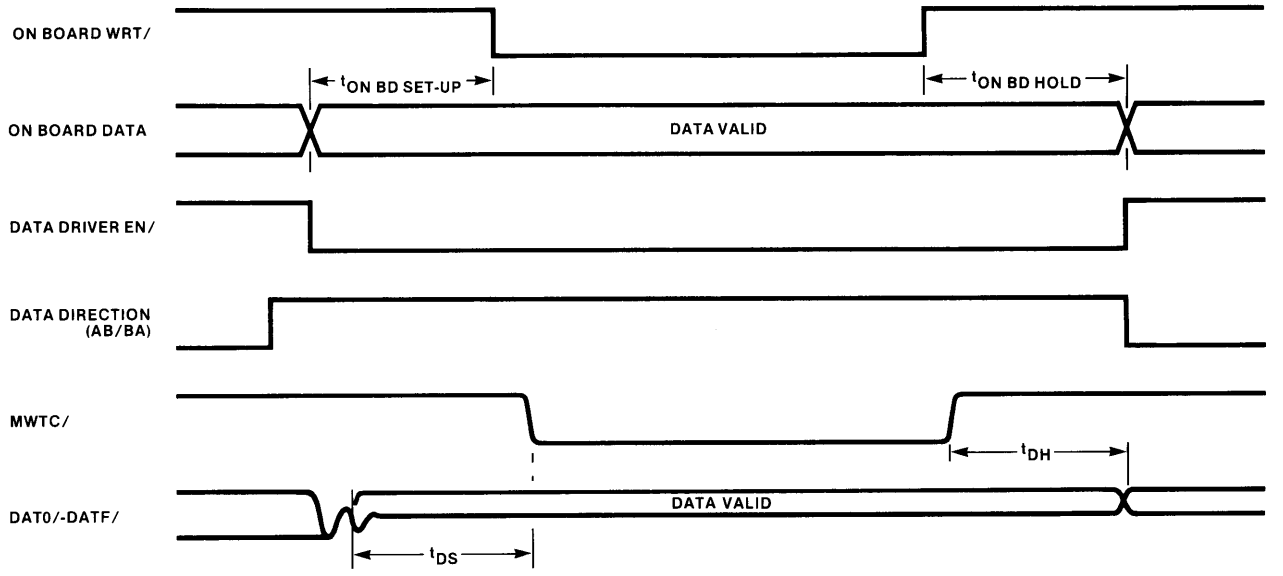


Figure 5-14. Data Signals AC Timing

5.1.4 INTERRUPT LOGIC

The MULTIBUS interface can support two type of interrupt operations, Non-Bus Vectored interrupts and Bus Vectored interrupts. The MULTIBUS master can generate its own interrupt restart address (Non-Bus Vectored-NBV interrupt) or require that the interrupting bus slave generate its own interrupt restart address (Bus Vectored-BV interrupt). Both types of interrupts permit only one master to respond to a given MULTIBUS interrupt line.

NOTE

Each level on the 8259/8259A can be programmed for NBV or BV interrupts individually.

5.1.4.1 Non-Bus Vectored Interrupts. The NBV interrupt design example is given in Figure 5-15. The bus interrupt lines (INT0/ -INT7/) are buffered by standard TTL receivers. The buffered interrupts go to optional jumprs which can be used to connect bus interrupt lines to different interrupt levels on the 8259/8259A. Once a bus interrupt line is activated, the 8259/8259A on the bus master will generate a local (internal) interrupt (INTR) to its CPU. The bus master will then generate local INTA's that will cause the local 8259/8259A to generate instruction data which will send the bus master to the appropriate address. The interrupt service routine will reset the interrupt with bus commands, as required by the interrupting source, and service the interrupt. This method limits the total number of bus interrupts a bus master can handle to eight.

5.1.4.2 BUS VECTORED INTERRUPTS. There are two designs which can be used to accommodate bus vectored interrupts (BVI). One is designed around the 8086 CPU, and the second around the 8080 or 8085 CPU. The following paragraphs will describe the two designs.

Figure 5-16 shows a design for an 8086 system which can accommodate both non-bus vectored and bus vectored interrupts. The bus interrupts (INT0/-INT7/) are buffered and routed to the master 8259A (the one on the bus master). When a bus slave generates an interrupt (INT0/-INT7), the master 8259A generates a local interrupt (INTR) to the 8086 CPU. The CPU on the bus master generates two back to back INTA commands which are sent out on the MULTIBUS interface. The first INTA command tells all the 8259As on the MULTIBUS interface to freeze the internal state of their interrupts for priority resolution. The first INTA also causes a request to be made to the master 8259A to issue the interrupt address on its C0-C2 pins at the end of the command. The bus master responding to the interrupt, puts the MULTIBUS interface into the override mode (to guarantee back to back INTAs), and generates its own acknowledge for the first INTA. The second INTA command is used to request the restart address from the bus slave. The interrupt number from the master 8259A (C0-C2), is put on the MULTIBUS address lines (ADR8-ADRA) by the responding bus master. The master 8259A will turn on the bus master's MULTIBUS receivers (with bus INTA DEN/) to receive the restart address. The bus slave will put the restart address on the lower data bus (DAT0-DAT7) and activate its acknowledge (XACK/). The bus master takes this address (which is on the data lines), and performs the necessary functions.

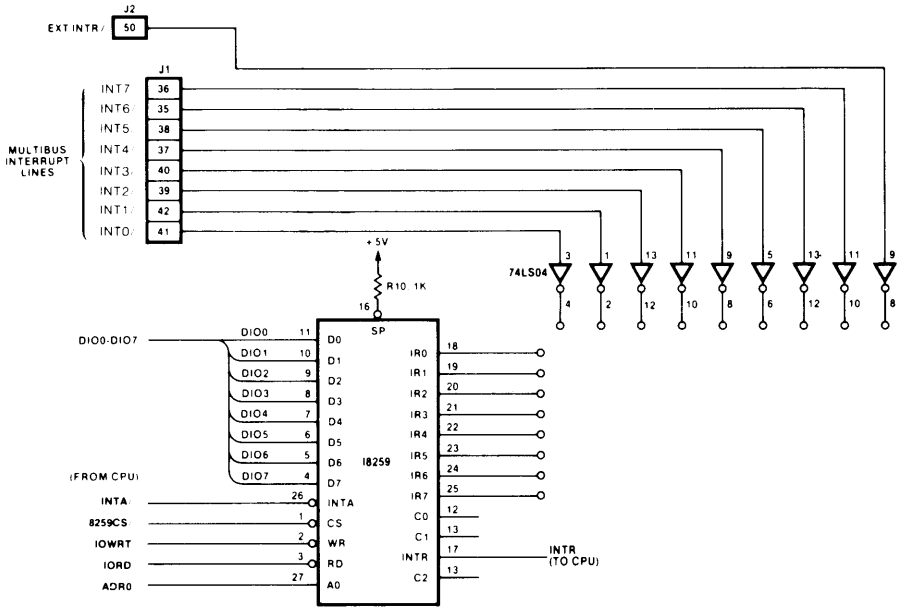


Figure 5-15. 8080/8085 Non Bus Vector Interrupt Logic

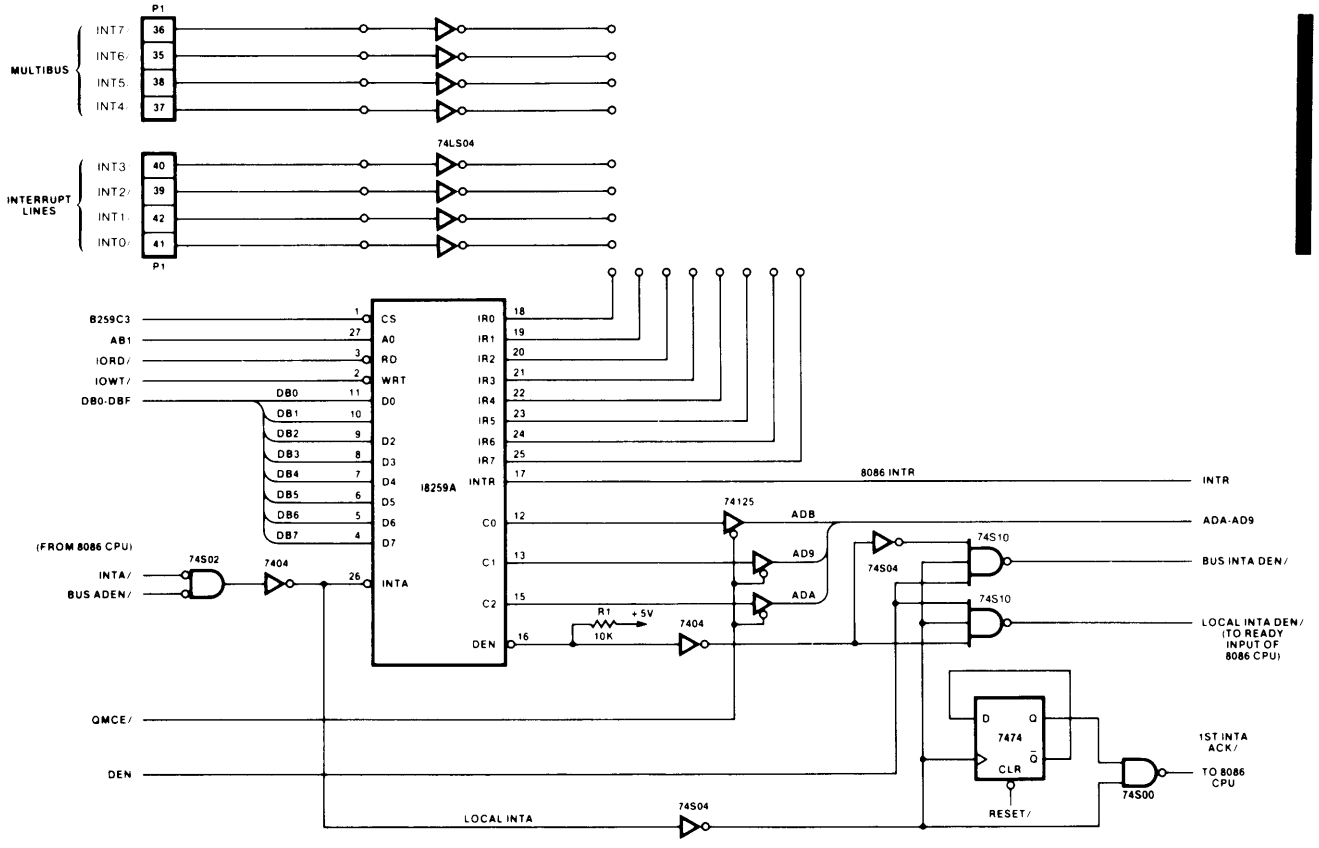


Figure 5-16. 8086 Bus Vectored Interrupt Logic

If the master 8259A was programmed for non-bus vectored interrupts (NBVI), the master 8259A would generate the restart address and its own acknowledge by generating DEN/ and feeding it to the READY input of the CPU.

The second type of design used for the bus vectored interrupts (BVI) works with an 8080 or an 8085 CPU. The 8259 on the bus slave generates an interrupt to the bus master's 8259 via the IR0-IR7 interrupt lines. The master 8259 generates an interrupt to its CPU, which in turn puts an INTA on the MULTIBUS interface. This first INTA commands all the 8259s on the MULTIBUS interface to freeze the internal state of their interrupts for priority resolution. The first INTA also causes the master 8259 to generate a call instruction to the CPU, which generates its own acknowledge. After the first INTA, the master 8259's C0-C2 lines (interrupt numbers) are valid and are sent out on the MULTIBUS address lines (ADR8-ADRA). The CPU then generates two more INTAs. This causes the slave 8259 who's number was on the ADR8-ADRA lines to transfer two 8 bit address bytes (on the data lines—DAT0-DAT7) to the bus master. The slave also generates an acknowledge (XACK/) to the bus master each time it sends an 8 bit address byte. The bus master takes the 16 bits of address and performs the necessary functions.

Both BVIs and NBVIs require control of the system bus to process the interrupt requests. This is required because at the time of the first INTA command, it is not known if the interrupt is a BVI or an NBVI type.

NOTE

The MULTIBUS interface can not support 2 INTA and 3 INTA boards on the same system.

Bus Vectored Interrupts with an 8086 CPU require an 8259A (not 8259) PIC on both the master and slave.

5.1.4.3 INTERRUPT LOGIC REQUIREMENTS. The important AC parameters associated with BV interrupts are shown in Figure 5-17 and 5-18. The interrupt line receivers should be as close to the bus pin as possible. Bus masters should also have the option to generate a MULTIBUS interrupt.

5.1.5 BUS EXCHANGE LOGIC

The bus exchange logic provides the means by which a master gains controls of the bus. The following signals are used to implement a bus exchange: Bus Clock (BCLK/); Bus Priority In (BPRN/); Bus Priority Out (BPR0/); Bus Request (BREQ/); Bus Busy (BUSY/); and common Bus Request (CBRQ/). The example of how the bus exchange logic can be implemented is shown in Figures 5-19.

The example shown in Figure 5-19 uses discrete logic to perform the bus exchange. Flip-flops A and B are used to synchronize the transfer request to the clock. The Q output of flop B becomes the bus request (BREQ). The Q output of flop B ANDs with BUSY/ (not active), and BPRN/ (Bus Priority In) to set flop

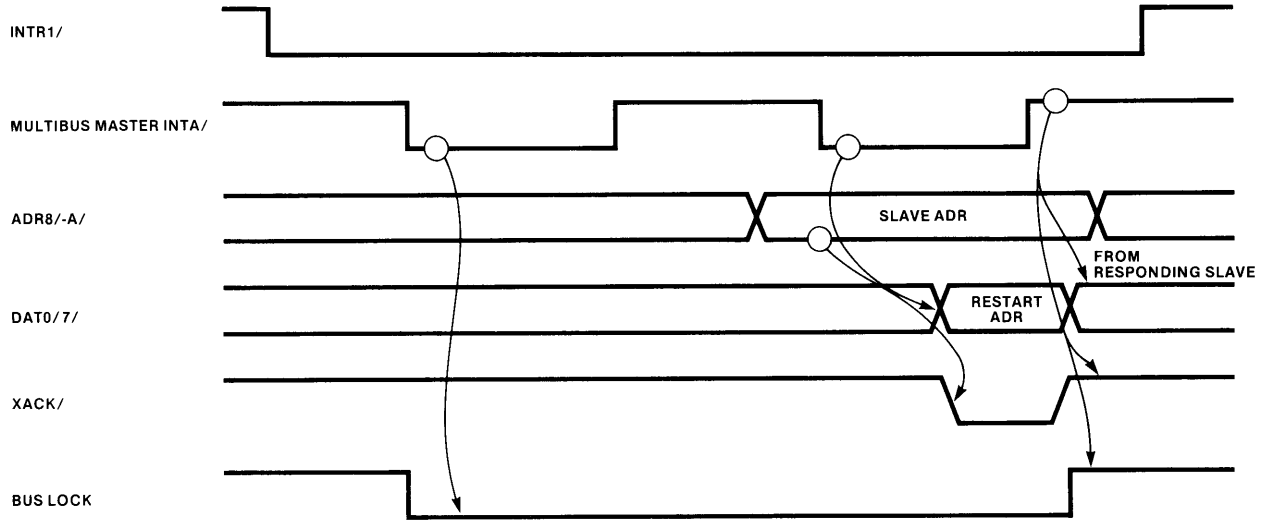


Figure 5-17. 2 INTA Bus Vectored Interrupt AC Timing

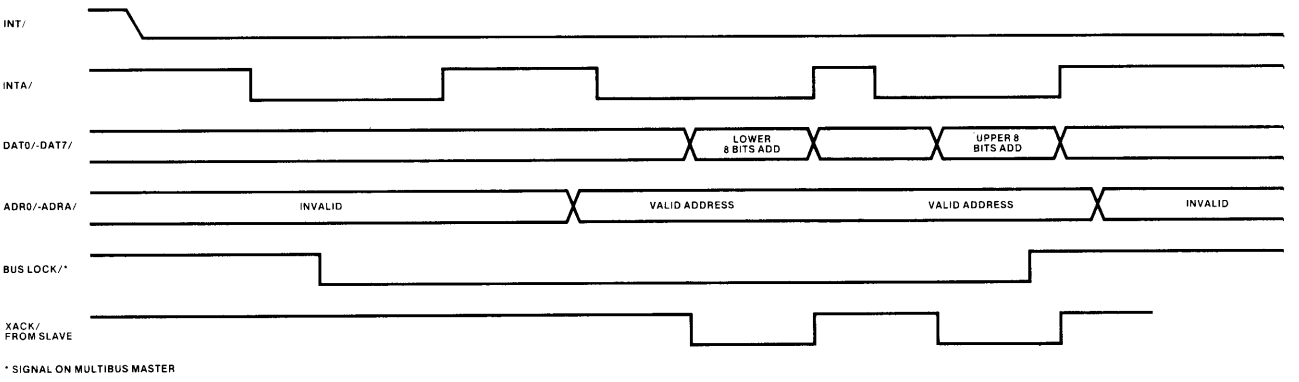


Figure 5-18. 3 INTA Bus Vectored Interrupt AC Timing

C and take the bus. When flop C sets, BUSY/ goes active making the bus busy to any other master, AEN/ goes active enabling the address onto the bus, and the Retain Bus circuits is satisfied locking up the bus until the Transfer Request is removed. BPR0/ is activated, to tell lower priority modules that the bus is being used. CMD EN/ goes active 1 Bus Clock after the address is put on the bus, to gate the command on to the bus. CBRQ/ is pulled low at the beginning of the bus request to indicate that this master wants the bus.

NOTE

Flip-flop A is synchronizing an asynchronous event, and it must resolve its output in less than one bus clock. Both flip-flops A and B must be high speed and have high resolution. Standard TTL flip-flops from high quality vendors can be purchased.

When the addressed slave device accepts the command, it generates an acknowledge (XACK/), causing the Transfer Request to terminate. When this occurs, the bus exchange logic for this master releases the busy by allowing BUSY/ to go inactive. If a master wishes to retain the bus for consecutive requests, it must generate the OVERRIDE signal. The timing for the bus exchange is shown in Figure 5-20.

An alternate design implementation of the MULTIBUS exchange logic uses a bus controller chip in place of the discrete logic shown in Figure 5-19.

It should be noted that BPR0/ should always be provided with a jumper because it is only used for a serial priority scheme. In a parallel scheme it must be removed from the bus because many backplanes connect BPR0/ of one board to BPRN/ of the next board.

It is recommended that CBRQ/ be provided with a jumper such that either CBRQ/ is used as shown in Figure 5-19 or, optionally, it can be tied to ground to always force a board to release the bus between cycles.

5.2 SLAVE DESIGN EXAMPLE

Modules which respond to bus commands and can not control the MULTIBUS interface are classified as bus slaves. The MULTIBUS interface of these modules can be divided into four basic elements:

1. Control
2. Address
3. Data
4. Interrupts

These elements and their functional relationship to the MULTIBUS interface are shown in Figure 5-21. A brief explanation and then a detailed implementation is given for each element.

5.2.1 CONTROL LOGIC

The control logic consists of the circuits that forward the I/O and memory READ/WRITE commands to their respective destinations, and provide the bus with transfer acknowledge responses.

5.2.1.1 COMMAND RECEIVERS. The MULTIBUS command lines (MRDC/, MWTC/, IORC/, IOWC/) should be buffered with high speed devices such as a Schotky type gates. High speed gates are recommended to minimize turn on and turn off

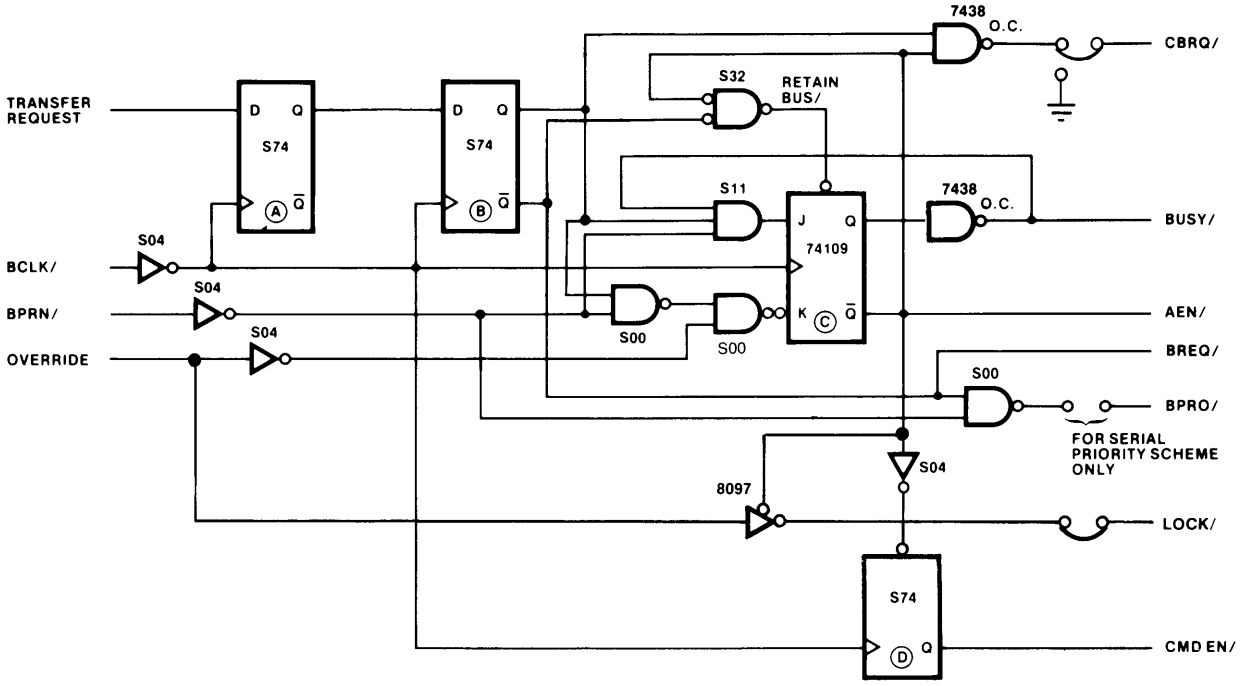


Figure 5-19. Bus Exchange Logic

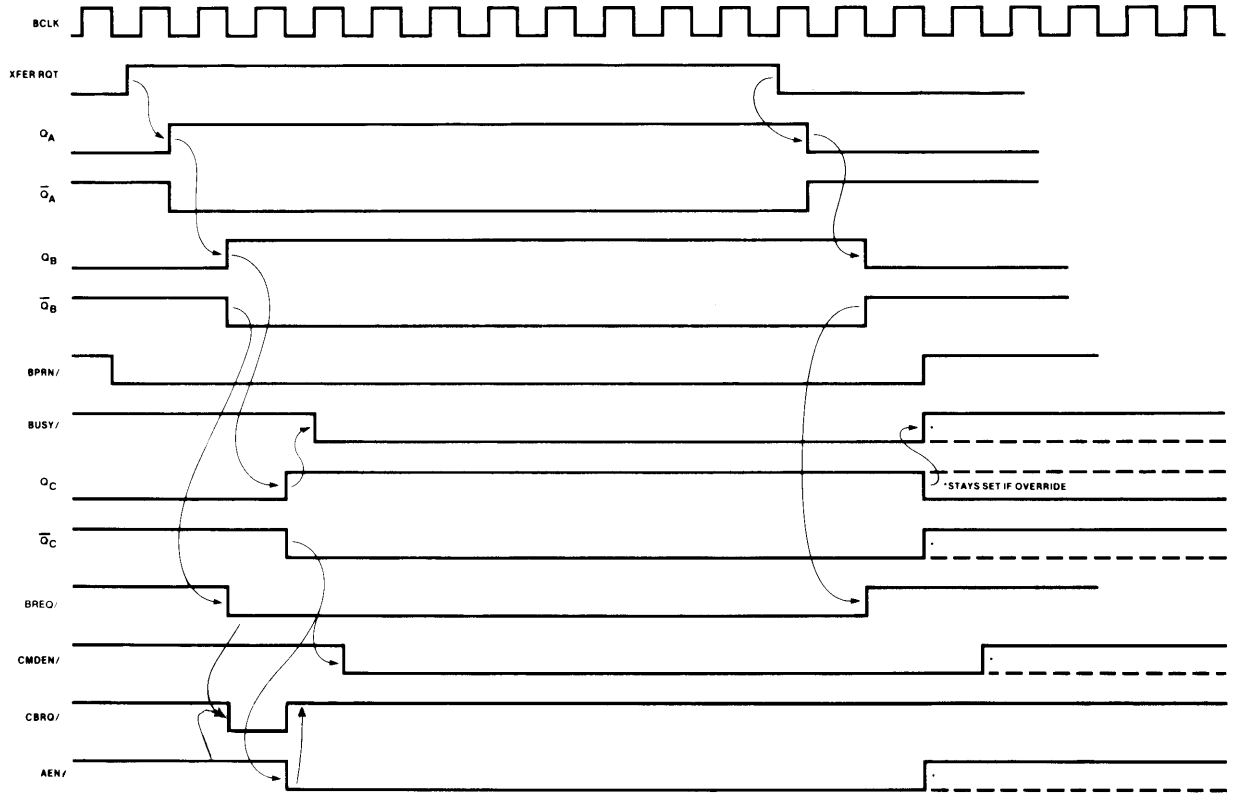


Figure 5-20. Bus Exchange Timing

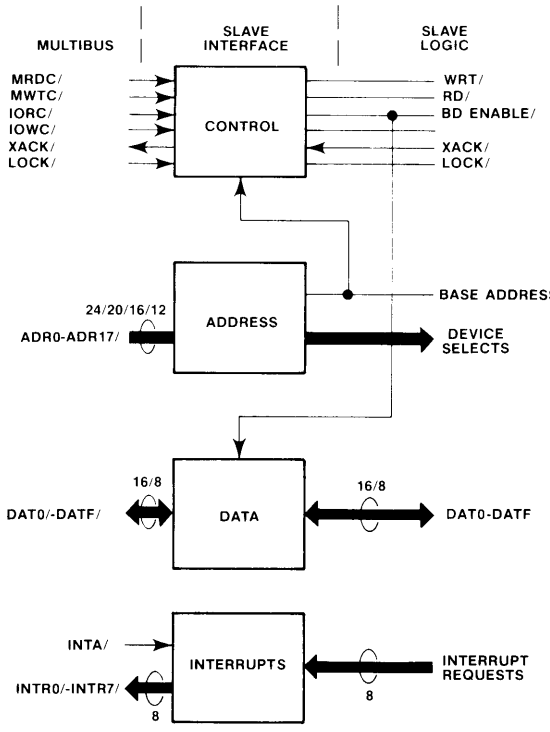


Figure 5-21. Slave MULTIBUS Interface

delays, as these signals are used to control devices which drive the MULTIBUS interface (see Figure 5-22).

5.2.1.2 TRANSFER ACKNOWLEDGE (XACK/) DRIVER. The user interface acknowledge logic provides a transfer acknowledge response, (XACK/), to notify the bus master that write data, provided by the bus master, has been accepted or that read data requested is available on the MULTIBUS. XACK/ allows the bus master to conclude its current bus cycle. Thus, the slave controls the access time, permitting each MULTIBUS slave to have different access times. The access time of a slave should never exceed 1 μsec. Although this is not a MULTIBUS requirement, longer access times may cause system errors. Many masters request bus control (such as a floppy disk controller) periodically to transfer data, and if they do not get the bus in time, they will lose data.

In the example, (Figure 5-22), the XACK/ driver is a three state driver enabled by the board enable (BDEN/) signal. This signal is a combination of 3 signals; the slave board is addressed (Address Select), a bus command to that module is active (MRDC/ or MWTC/), and the inhibit signals (INHIBIT/) is not active (this signal is used only on memory slave modules).

The board enable signal (BDEN/), which also enables the data drivers, must be generated as quickly as possible to meet MULTIBUS specifications for the data and XACK/ signals (see Figure 5-23).

The transfer acknowledge (XACK/) timing in this example (Figure 5-22) is generated by a shift register (74164) clocked with CCLK/. When a command is received by the board, the clear signal to the shift register is removed and the shift register begins shifting in ones. The shift register outputs produce different length delays (with respect to the command) which can be jumpered to the XACK/ circuit to produce the proper timing of XACK/ with respect to the incoming commands. For example, if we wanted XACK/ to occur app. 300-400 nsec (CCLK/ = 10 MHz) after the reception of the command we would connect the circuit as shown in Figure 5-22. The shift register would be cleared and XACK/ deactivated) as soon as the MULTIBUS command (MRDC/ or MWTC/) is removed.

5.2.1.3 CONSTANT CLOCK (CCLK/) RECEIVER. The trace length between the MULTIBUS and the CCLK/ receiver must be kept to a minimum. The designer also should not use LS gates for CCLK/, because LS gates cannot tolerate negative overshoot.

5.2.2 ADDRESS DECODING

The address decoding logic decodes the appropriate MULTIBUS address bits into RAM requests, ROM requests, or I/O selects. Care must be taken in the design of the address decode logic to ensure flexibility in the selection of base address assignments. Without this flexibility, severe restrictions may be placed upon various system configurations. Ideally, switches and jumper connections should be associated with the decode logic to permit field modification of base address assignments.

The initial step in designing the address decode portion of a MULTIBUS interface is to determine the required number of unique address locations. This decision is influenced by the fact that address decoding is usually done in two stages. The first stage decodes the base address, producing an enable for the second stage which generates the actual device selects for the user logic. A convenient implementation of this two stage decoding scheme utilizes a single decoder driven by the high order bits of the address for the first stage and a second decoder for the low order bits of the address bus. This technique forces the number of unique address locations to be a power of two, based at the address decoded by the first stage.

Address decoding must be completed before the arrival of a command. Since the command may become active within 50 ns after stable address, the decode logic should be kept simple with a minimal number of layers of logic. Furthermore, the timing is extremely critical in systems which make use of the inhibit lines.

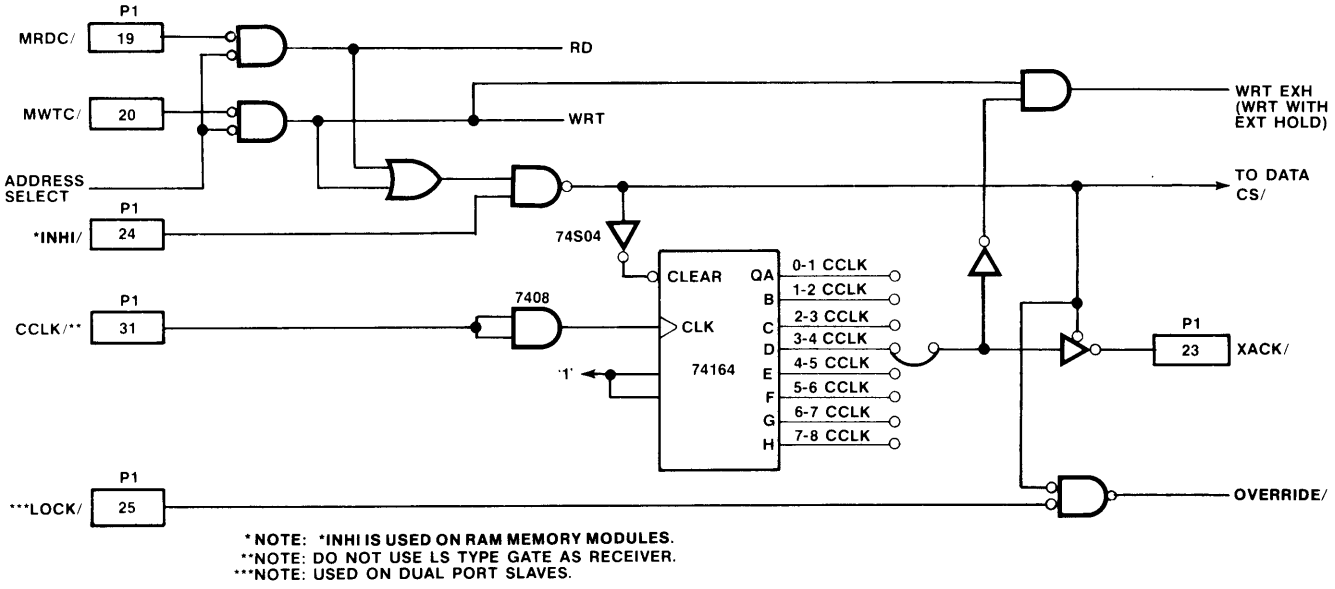


Figure 5-22. Slave Control Logic

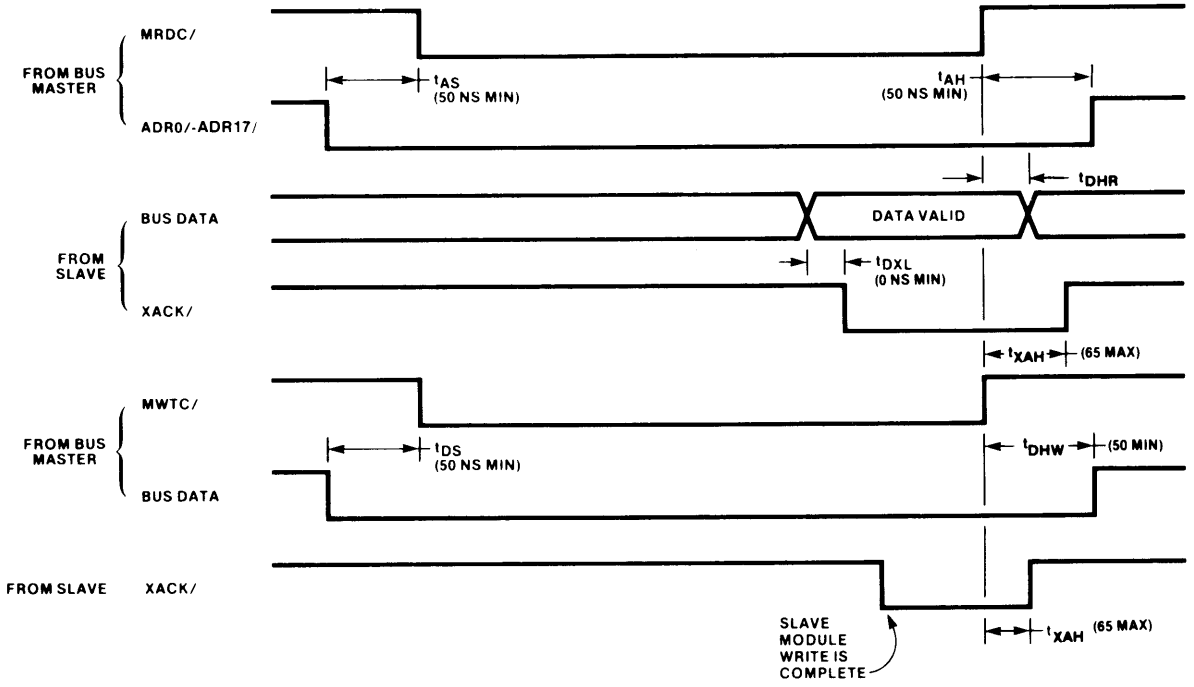


Figure 5-23. Slave Logic AC Timing

A linear select scheme in which no decoding is performed, is not recommended for the following reasons. First, the scheme offers no protection in case multiple devices are simultaneously selected. And second, the addressing within such a system is restricted by both the lack of flexibility in base address selection and by the extent of the address space occupied by such a scheme.

5.2.2.1 INPUT/OUTPUT ADDRESS DECODING. Figure 5-24 illustrates a means of implementing the two stage decoding scheme for I/O addresses. The fact that the MULTIBUS interface can support systems that generate 8, 12, or 16 bit I/O addresses must be taken into consideration when designing the input/output address decoding logic. In Figure 5-24, decoder circuits A1 and A2 are used to decode address bits ADR5/-ADRB/. These two circuits produce switch/jumper selectable outputs of the first stage of decoding. The ninth position of S2 (ground) is used to ignore bits ADR8/-ADRB/ on a system which only uses 8 bits for I/O addressing. The outputs of the first stage of decoding (S1 and S2) are used as enables for the second stage of decoding (A3). This circuit decodes bits ADR2/-ADR4/ of the address bus, and produces the chip select funds (CS0-CS7) for the I/O devices. ADR0 and ADR1 (the lower two address bits) are sent directly to the I/O devices where they can be used to activate a specific function of a multi-function device.

5.2.2.2 MEMORY ADDRESS DECODING. A memory address decoding scheme is shown in Figure 5-25. The design takes into consideration the ability of the MULTIBUS interface to support systems which can generate 20 or 24 bit memory addresses. Circuit A1 is used to decode bits ADR14/-ADR17/ (the upper four bits of a 24 bit address). The switch/-jumper selectable output of A1 specifies the 1M page (one of 16 possible in a 16 megabyte system) that this address is in. Decoder A1 is not needed in a 20 bit system, so S2 would be set to the ground position. A2 decodes bits ADR11/ - ADR13/ to select a switch/-jumper selectables (S1) 128K segment of memory. The outputs of these two circuits are

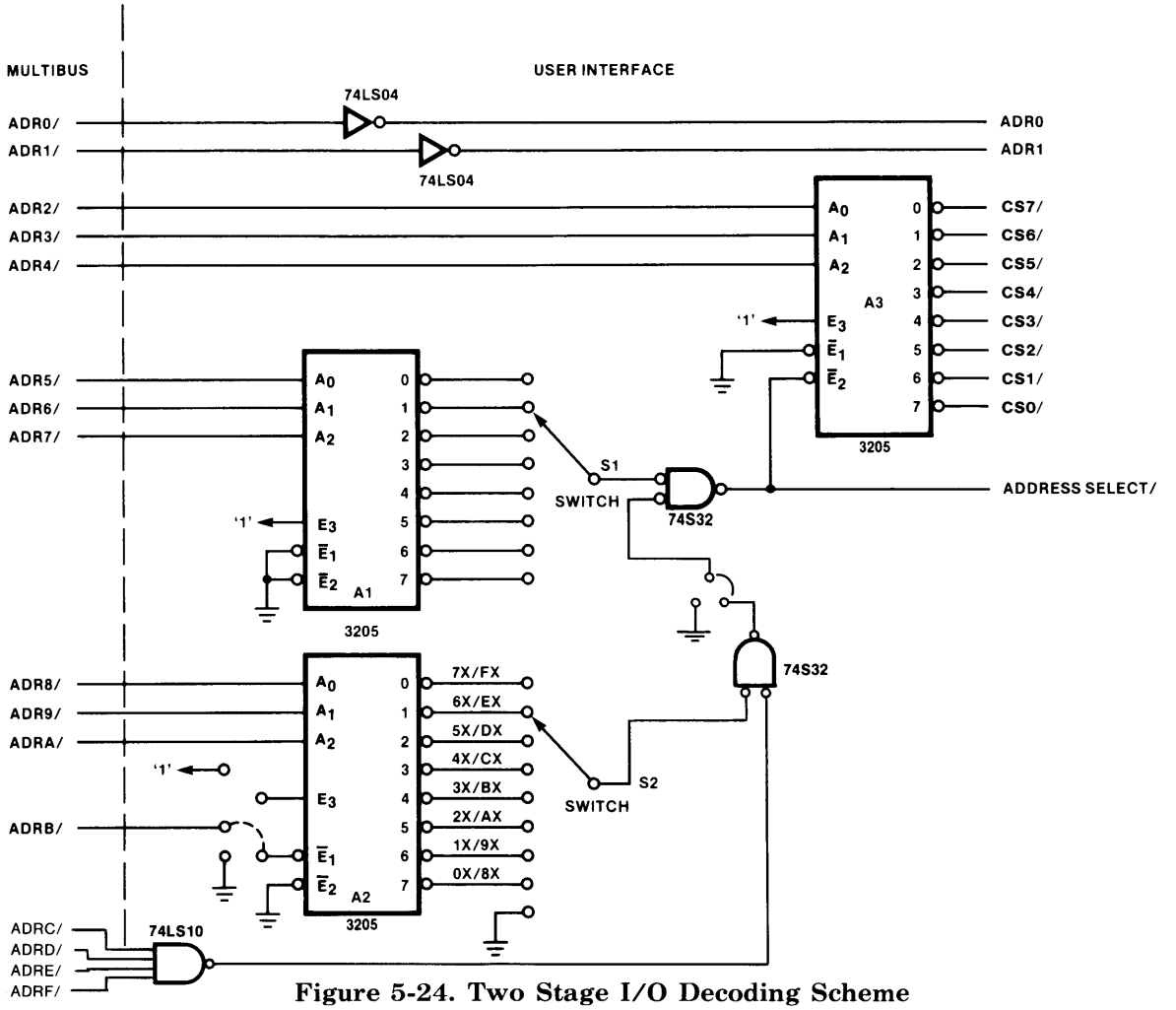


Figure 5-24. Two Stage I/O Decoding Scheme

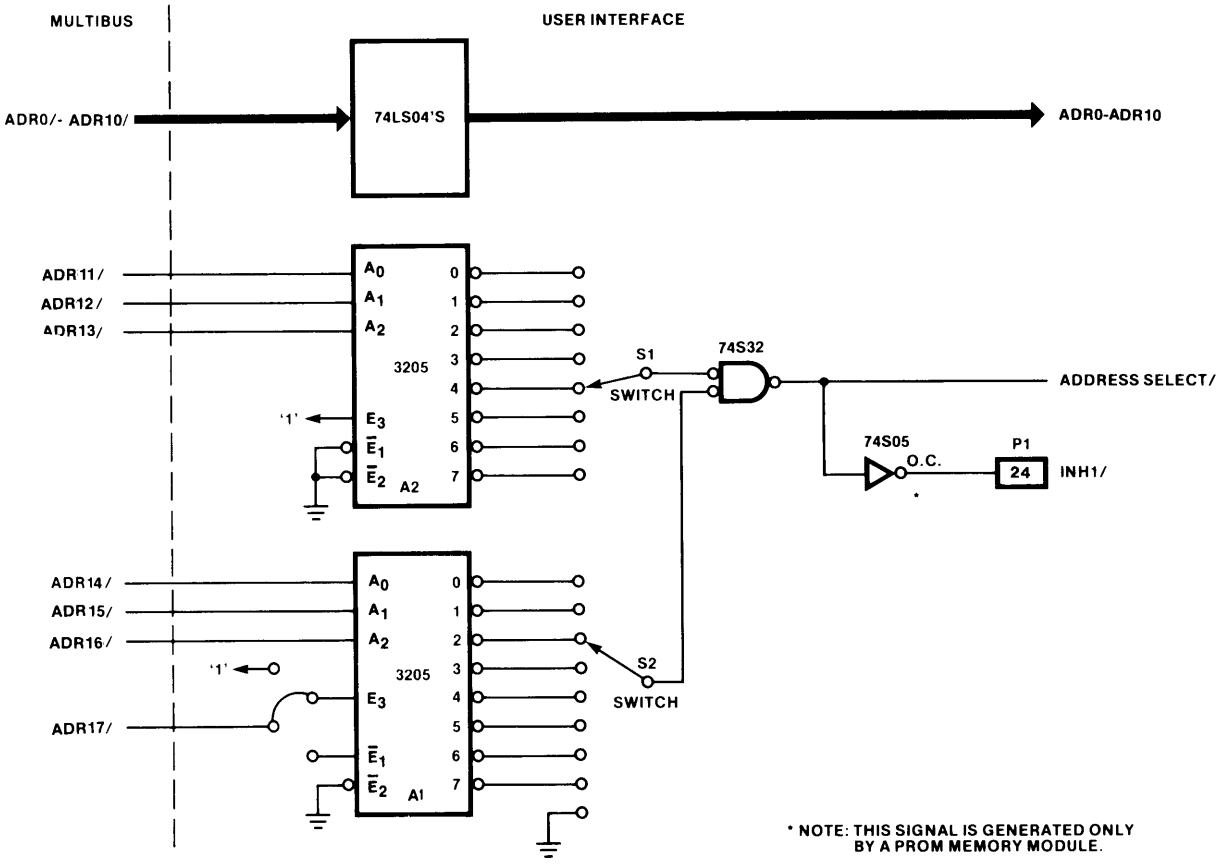


Figure 5-25. Memory Decoding Scheme

ANDed together to produce the Address Select function. Bits ADR0/-ADR10/ are sent directly to the memory circuits to select a specific location.

The inhibit signal (INH1/) is produced by PROM memory modules which overlap RAM memory space. This signal when active, turns off a RAM module which otherwise would respond to the address on the MULTIBUS. INH1/ should be generated as early as possible from the address information as shown in Figure 5-25. The INH1/ signal is generated by a high speed open collector device (74S05).

Important AC timing parameters for memory address decoding are shown in Figure 5-26.

5.2.2.3 EXTENDED MEMORY ADDRESSING COMPATIBILITY. Refer to section 6.5.4 for a discussion of the Extend Memory Addressing capabilities of the older MULTIBUS compatible products.

5.2.3 DATA BUS DRIVERS

The MULTIBUS requires three-state drivers on the bidirectional data lines. Uni-directional buffers may be used for user designed logic which only receives data from the MULTIBUS. Buffers are required to ensure that maximum allowable bus loading is not exceeded by the user logic.

In systems where the user designed logic must place data onto the MULTIBUS, three-state drivers are required. These drivers should be enabled only when a

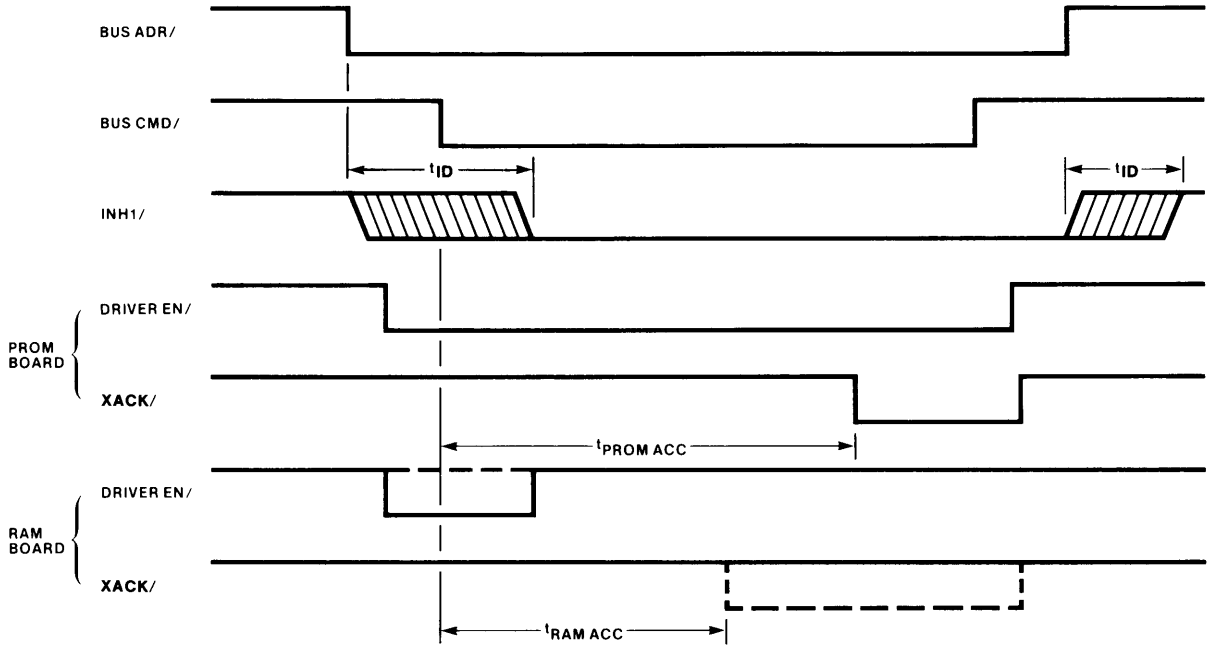


Figure 5-26. Inhibit AC Timing

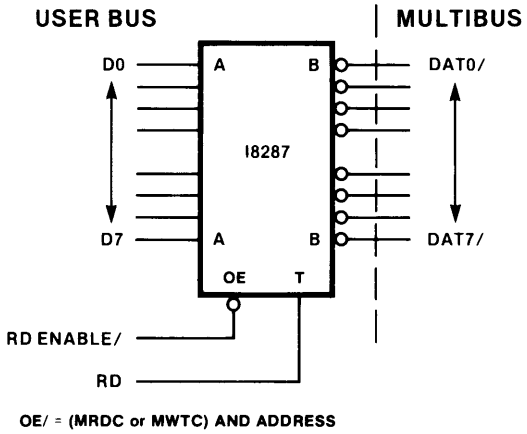


Figure 5-27. 8 Bit I/O Bidirectional Bus Drivers

memory read command (MRDC/) or an I/O read command (IORC/) is present and the module has been addressed.

When both the read and write functions are required, parallel bidirectional bus drivers (e.g., Intel 8286/8287) are used. A note of caution must be included for the designer who uses this type of device. A problem may arise if data hold time requirements must be satisfied for user logic following write operations. When bus commands are used to directly produce both the chip select for the bidirectional bus driver and a strobe to a latch in the user logic, removal of that signal may not provide the user's latch with adequate data hold time. Depending on the specifics of the user logic, this problem may be solved by gating the buffered write to the LSI devices with XACK/. This would turn off the on board write command, but not the data drivers, before the bus master terminates the command. This would provide sufficient hold times to the on board LSI device. An example of this is shown in Figure 5-22, where a write with extended data hold time (WRTEXH) is generated (WRTEXH is terminated when XACK/ goes active).

Figure 5-27 and 5-28 are examples of 8 bit and 8/16 bit data bus drivers. Detailed explanation of the 8/16 bit example is given in section 5.1.3 (Data Logic).

5.2.4 INTERRUPT LOGIC

Slave modules may support two types of MULTIBUS interrupts, non-bus vectored (NBV) interrupts and bus vectored (BV) interrupts. The interrupt lines must be driven by open collector devices with a minimum drive of 16 ma.

5.2.4.1 NON-BUS VECTORED INTERRUPTS.

A non-bus vectored (NBV) interrupt logic example is shown in Figure 5-29. This logic can assert, latch up, and read the status of the interrupt. The Interrupt

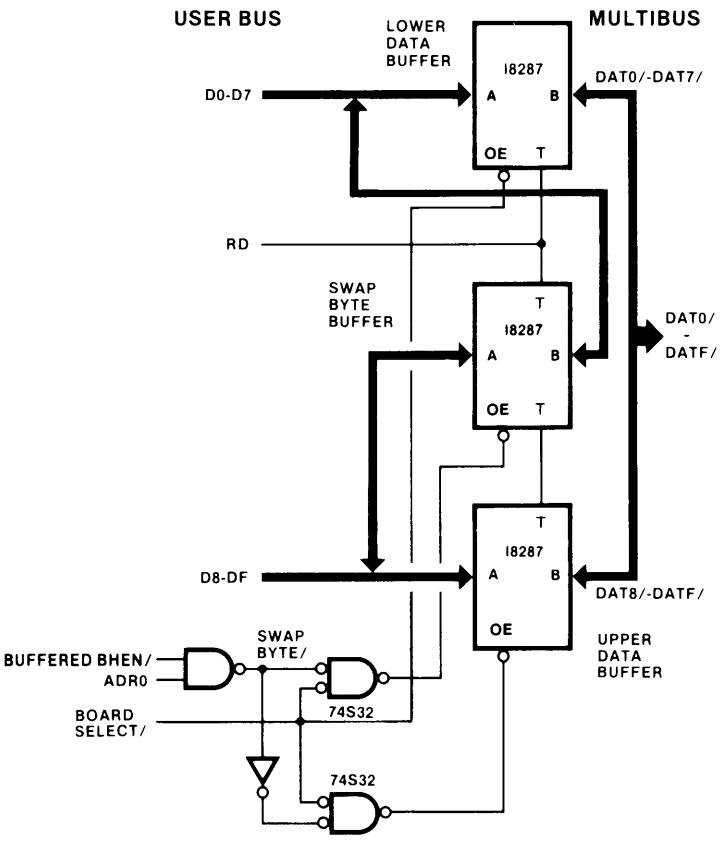


Figure 5-28. 16/8 Bit Data Drivers

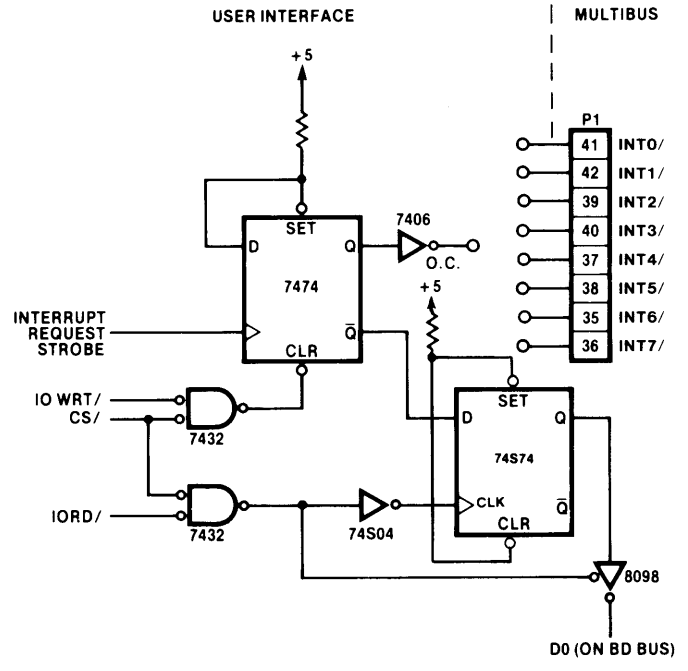


Figure 5-29. Slave NBV Interrupt Logic

Request Strobe feeds to the clock input of the 7474 flip-flop. When an interrupt occurs, it is latched up in the 7474. Once latched, the interrupt is buffered with a 7406 open collector device and fed to one of the eight MULTIBUS interrupt lines.

The bus master then processes the interrupt by generating it's own restart instruction and servicing the interrupt. The interrupt status is read (IORD/) when the slave is properly addressed (CS/) and the 74125 is enabled, allowing it to drive the data bus. The interrupt is cleared by writing (IOWRT/) to the same I/O address.

5.2.4.2 BUS VECTORED INTERRUPTS. The following two design examples show how a bus slave can handle Bus Vectored Interrupts.

A design which can accommodate NBV and BV interrupts (both 2 INTA and 3 INTA compatible) is given in Figure 5-30. The interrupt from the 8259A is buffered and routed to the MULTIBUS interrupt lines the same as in the NBV interrupt example. When the 8259A receives a user interrupt, it passes it on to the MULTIBUS. The bus master will respond to the interrupt by generating two INTA commands. The first INTA will freeze the internal state of all the 8259A's on the MULTIBUS, and request the master 8259A (the one on the bus master) to issue the interrupt address code on its internal bus. The MULTIBUS is also put into an override mode by the bus master to guarantee consecutive INTA commands. The second INTA command requests a restart address from the interrupting bus slave. Address lines ADR8—ADRA are driven by the bus master with the interrupt address code generated by the master 8259A. On the second INTA command, the slave 8259A looks at the address lines. If the address lines match the slave's address, it activates its EN/ pin which turns on that slaves data drivers. The slave 8259A will then drive the data lines (DAT0—DAT7) with the restart address, and activate the transfer acknowledge (XACK/) on the MULTIBUS causing the bus master to jump to the appropriate address and service the interrupt.

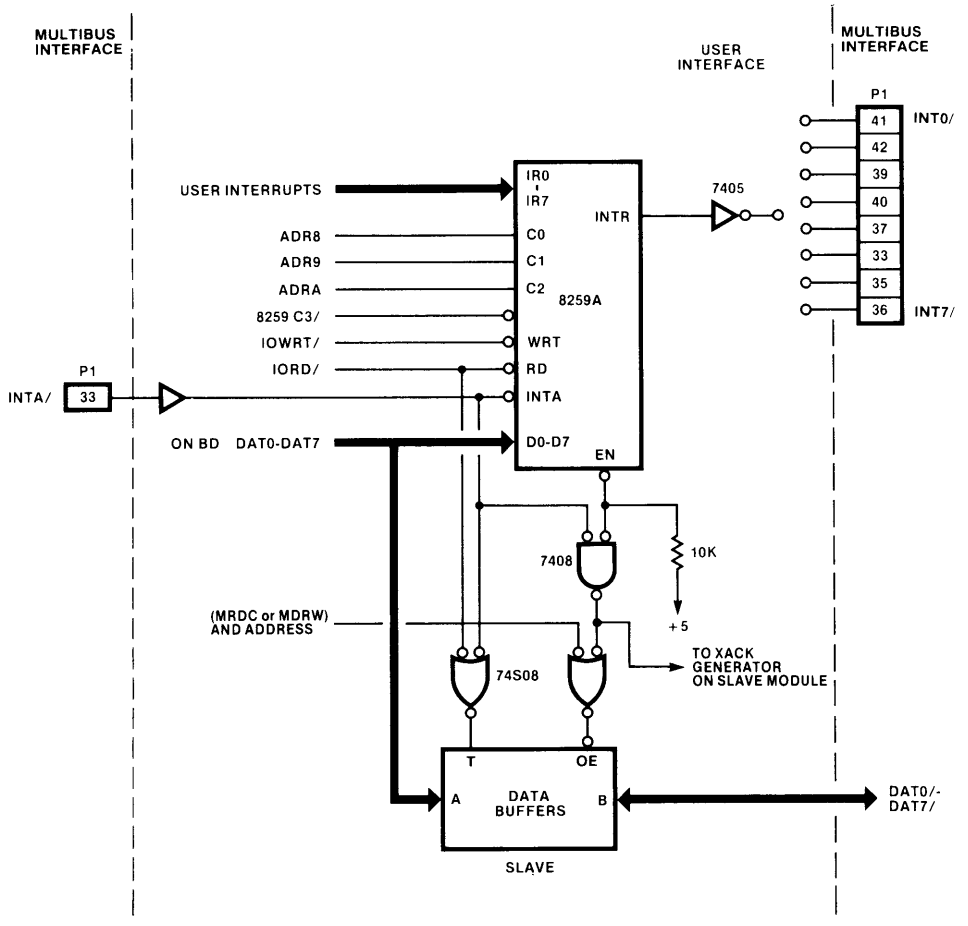


Figure 5-30. Slave BV Interrupt Logic

NOTE

The 8259A (not 8259) must be used when implementing BVIs with 8086 CPUs.

The second type of design used for the bus vectored interrupts (BVI) works with an 8080 or an 8085 microprocessor. The 8259 on the bus slave generates an interrupt to the bus master's 8259 via the IR0-IR7 interrupt lines. The master 8259 generates an interrupt to its processor, which in turn puts an INTA on the MULTIBUS interface. The first INTA commands all the 8259s on the MULTIBUS interface to freeze the internal state of their interrupts for priority resolution. The first INTA also causes the master 8259 to generate a call instruction to the processor, which then generates its own acknowledge. After the first INTA, the master 8259's C0-C2 lines (interrupt number) are valid and are sent out on the MULTIBUS address lines (ADR8-ADRA). The processor then generates two more INTAs. This causes the slave 8259 whose number was on the ADR8-ADRA lines to transfer two eight bit address bytes (on the data lines—DAT0-DAT7) to the bus master. The slave also generates an acknowledge (XACK/) to the bus master each time it sends and eight bit address byte. The bus master takes the 16 bits of address, and performs the necessary functions.

NOTE

The MULTIBUS interface can support only one type of Bus Vectored Interrupt on a given system.

5.3 BUS EXCHANGE IMPLEMENTATION EXAMPLES

The following two sections give examples of two bus exchange techniques (1) Parallel priority and (2) Serial priority.

5.3.1 PARALLEL PRIORITY EXAMPLE

This section describes the relationship of the bus exchange signals when using a parallel priority resolution technique. An example circuit which can accommodate up to 16 masters is shown in Figure 5-31. The circuit uses a 74148 Encoder and a 74S138 Decoder chip for each group of 8 masters. The 74148 monitors the BREQ/ lines for eight masters. When a BREQ/ goes active, the encoder takes this input and creates a 3 bit number to satisfy the BREQ/ line number. The output of the encoder feeds to the 74S138 Decoder which decodes the output and activates the appropriate BPRN/ (Bus Priority In) line for the master generating the request. The activation of the BPRN/ line allows the selected master to access the MULTIBUS interface. This parallel bus arbitration technique resolves bus priorities in external hardware.

The exchange process begins when master B generates a transfer request to access some resource, such as an I/O or memory module. This internal transfer request is synchronized with the falling edge of BCLK/ to generate a bus BREQ/ signal. The BPRN/ signal to master A goes inactive because of the BREQ/ from master B. When the BPRN/ signal to master A is inactive and master A has completed the current bus cycle, the busy (BUSY/) signal goes low on the falling edge of the next BCLK/. This allows the actual exchange to occur because control of the bus has been relinquished and another master is allowed to assume control. During this time the drivers of master A are disabled. Master B must take control of the bus with the next falling edge of BCLK/, completing the actual bus exchange. Master B takes control by asserting BUSY/ and enabling its drivers. Thus a full BCLK/ period, in addition to the synchronization of the internal transfer request, is required for the bus exchange between masters and must be included in bus latency calculations.

The relationship of the bus exchange signals is shown in Figure 5-32. In this example master A has been assigned a lower priority than master B. The bus exchange occurs because master B asserts a bus request during a time when master A has control of the bus.

As stated earlier, the bus resolution timing is synchronous with bus clock and must start on a falling edge and be completed by the next falling edge. The following timing must be met for proper bus exchanges to occur.

Parallel
Resolution time = BCLK = $t_{BRQ\ out}$ + $t_{bus\ delay}$
+ $t_{parallel\ resolution\ time}$
+ $t_{bus\ delay}$
+ $t_{BPRN\ set\ up}$ + BCLK skew

100NS	= 35	+ 1
	+ $t_{parallel\ resolution}$	+ 1
	+ 22	+ 2.0

Solving for

$t_{parallel\ resolution}$ ⩽ 100—62
⩽ 38ns

$t_{parallel\ resolution}$ for Figure 5-31
= t_{74148} + t_{74S138}
= 25ns + 12ns
= 37ns

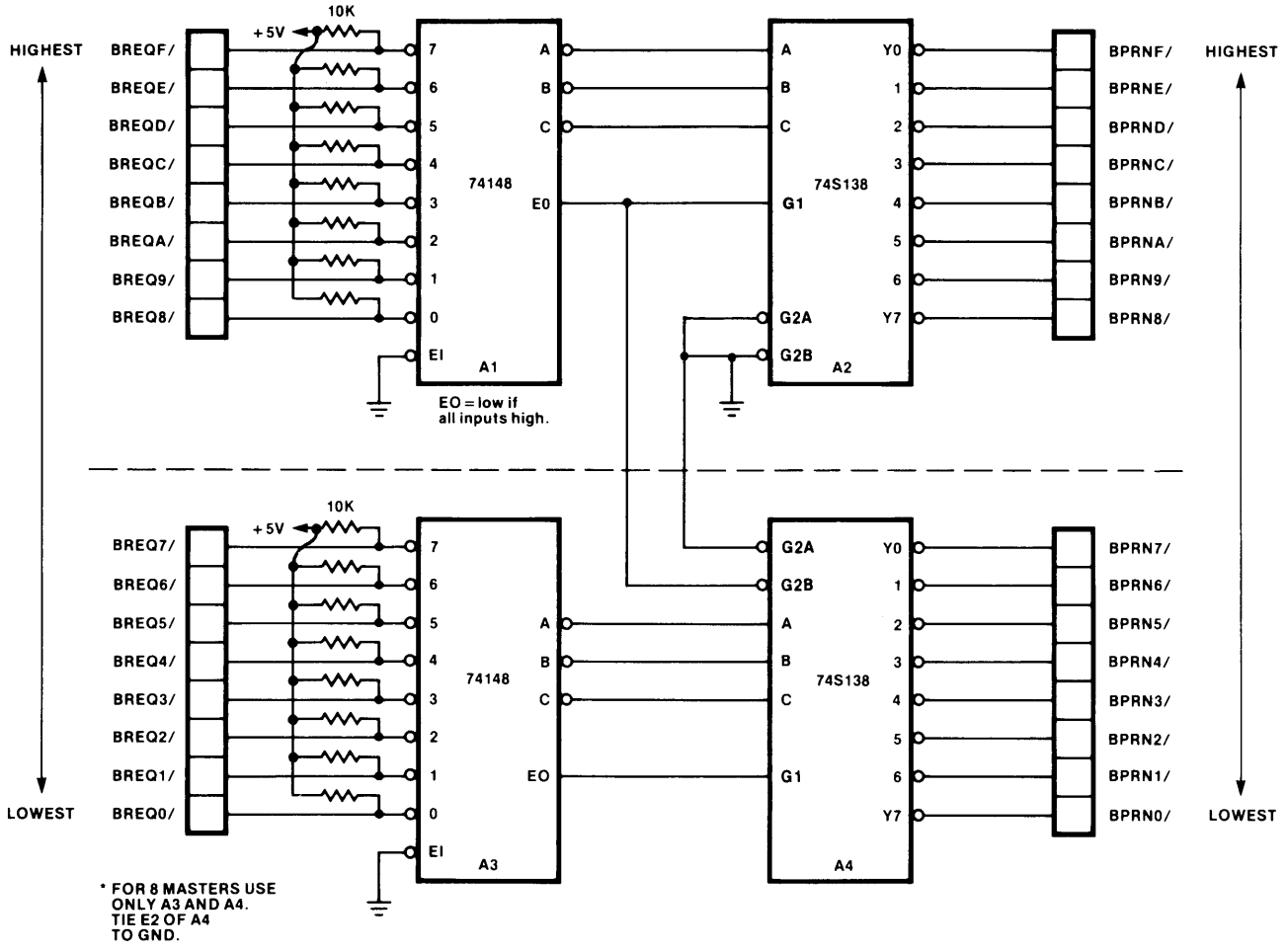


Figure 5-31. Parallel Priority Resolution Circuit For Up To 16 Masters

5.3.2 SERIAL PRIORITY EXAMPLE

This section explains the relationship of the bus exchange signal susing a serial priority resolution technique. A serial priority technique is a simple concept which passes priority on to the next lower priority master if this master does not need the MULTIBUS. Requests for system utilization are ordered by priority on the basis of bus location. The first master in the chain is the highest priority master with succeeding masters next in priority. Thus, each master on the bus notifies the next lower priority master when it needs to use the MULTIBUS for a data transfer, and monitors the bus request status of the higher priority master. The masters pass bus requests along from one to the next in daisy-chain fashion. In the example shown in Figure 5-33, the highest priority is given to master A, then master B, and the lowest is given to master C. The highest priority master (master A) will always receive access to the system bus when it requires it. There is no higher priority master to inhibit its bus requests, and its bus priority input line (BPRN/) is permanently enabled (grounded).

Masters operate asynchronously on the MULTIBUS. A master may be in the middle of a bus operation when a higher priority master requests the MULTIBUS. Obviously interruption of such an in-process cycle must not be allowed. The MULTIBUS mechanism for avoiding such erroneous operation is the BUSY/ line. Upon being notified that access to the MULTIBUS is possible (via BPRN/), the master examines BUSY/. If this control line is inactive (high), the master will assert it (drive it low) and complete its bus operation. If BUSY/ is already active, another master is currently using the MULTIBUS. In this case, the master will examine BUSY/ upon every falling edge of BCLK/ (typically once every 100ns) until it becomes inactive. When BUSY/ returns to its

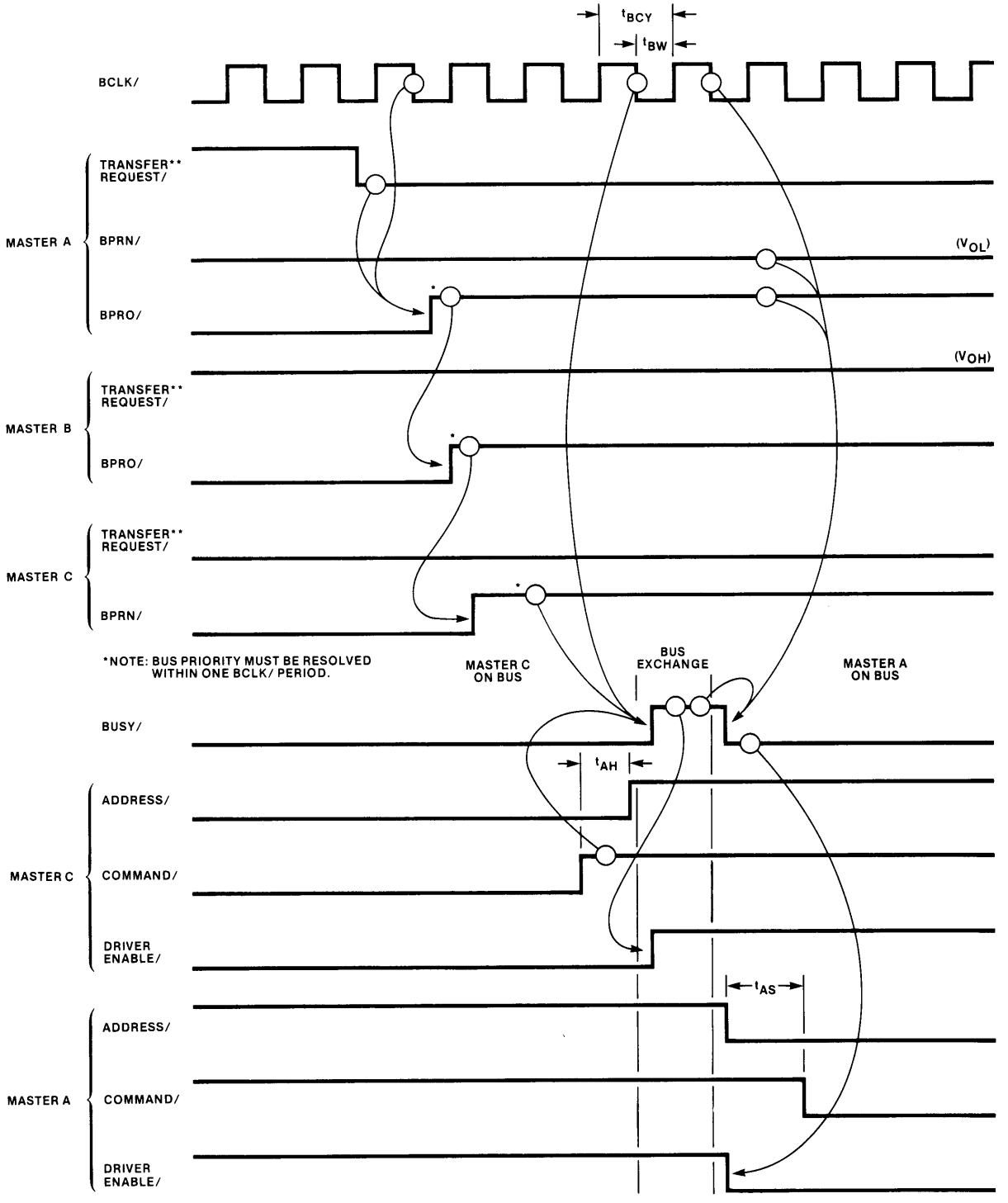


Figure 5-32. Bus Control Exchange Operation

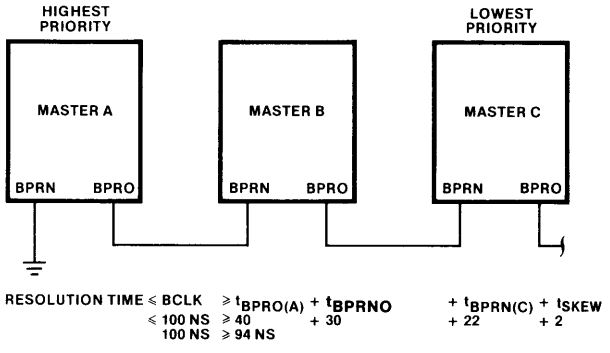


Figure 5-33. Serial Priority Circuit

inactive state, the master will then complete its operation. Because BPRN/ is sampled before BPRO/ is asserted, there is no possibility of erroneous bus arbitration. The BUSY/ line inhibits higher priority masters from destroying a bus transfer cycle which may be already in progress. The relationship of the bus exchange signals is shown in Figure 5-32 using a serial bus priority technique shown in Figure 5-33. The exchange process begins when master A requires the bus to access some resources such as an I/O or memory module. This internal transfer request is synchronized with the falling edge of BCLK/ to deactive its BPRO/ signal. This signal goes to the BPRN/ of master B and deactivates its BPRO/ which disables the BPRN/ of master C.

When the BPRN/ signal to master C is inactive and master C has completed its command, BUSY/ goes inactive on the next trailing (high to low) edge of BCLK/. This allows the actual exchange to occur because control of the bus has been relinquished and another master can now assume control. During this time the drivers of master C are disabled. Master A must take control of the bus with the next falling edge of BCLK/, completing the actual bus exchange. Master A takes control by asserting BUSY/ and enabling its drivers.

The maximum number of serial masters allowed on the MULTIBUS is calculated as follows:

$$\text{Max \#} = 2 + \left\lfloor \frac{t_{BCLK} - t_{BPRO(A)} - t_{BPRN} - t_{SKEW}}{t_{BPRNO}} \right\rfloor^{*}$$

*NOTE $\lfloor X \rfloor$ = The greatest integer less than or equal to X (the "floor" of X)

t_{BCLK} = bus clock period

t_{BPRO} = bus clock falling edge to BPRO/

t_{BPRNO} = propagation delay of BPRN/ in to BPRO/ out

t_{SKEW} = propagation of BCLK/ from source to end of bus (last master)

The maximum number can easily be extended if the user wishes to generate a BCLK/ with a longer cycle. All iSBC products provide a jumper option which allows the on-board BCLK/ to be disabled, so that the user can supply his own external clock.

5.4 POWER FAILURE BACKUP METHODS

There are two methods by which MULTIBUS compatible modules can optionally provide power failure backup voltages to the memory and supportive devices. The first method is simply a separation of power to devices which must be backed up. The backed up voltages go to the auxiliary connector (P2) and the system must provide the uninterruptable power source (UPS). The second method is similar to the first except that the UPS (a battery) is on the P.C. board. An advanced power down indication is given to the board which turns on the UPS.

Block diagrams for both methods are shown in Figure 5-34 (back up with system UPS) and Figure 5-36 (back up with on board UPS). The following options should be implemented on all modules which provide power failure back up.

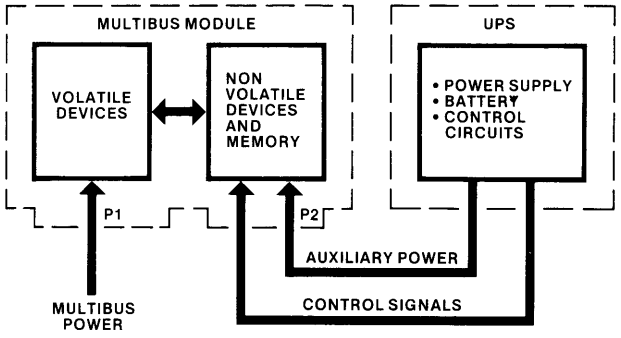


Figure 5-34. Power Failure Diagram Using A UPS

1. Provide the ability to connect MULTIBUS power to auxiliary power. This should be done when product is shipped.
2. Provide the ability to route the power fail interrupt (PFIN/) to the CPU if a master, or to the MULTIBUS interrupt lines if a slave.

3. Provide an input port to optionally read the power fail sense (PFSN/) line.
4. Provide an output port to optionally control the power fail sense reset (PFSR/) line.
5. Provide the ability to route a power up reset to the INIT/ line.

The power failure signal AC timing for both methods is shown in Figure 5-35 and 5-37 respectively.

5.6 AC AND DC SPECIFICATION RECOMMENDATION

This section is designed to standardize the writing of AC/DC specs for MULTIBUS modules. Tables 5-4, 5-5, and 5-6 list all standard mnemonics for master and slave modules. Figures 5-38 and 5-39 show the AC timing for MULTIBUS slaves and MULTIBUS masters.

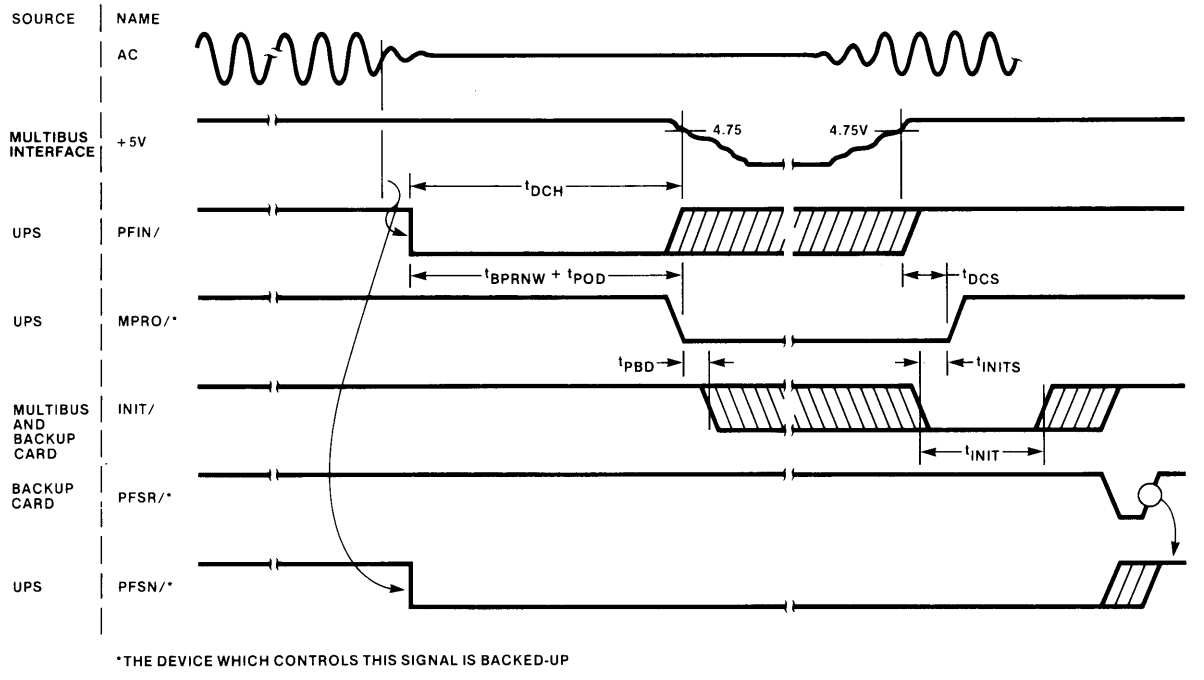


Figure 5-35. UPS Control Signals AC Timing

5.5 DESIGN RECOMMENDATION SUMMARY

The following sections provide a summary of the design recommendations.

5.5.1 SYSTEM POWER SUPPLIES (RECOMMENDATION ONLY)

All power supplies should conform to table 5-3.

5.5.2 MULTIBUS FORM FACTORS

All MULTIBUS compatible boards must conform to the outline drawing shown in Figure 4-4. Note that the top of the board is not fixed, and can be designed to meet your requirements. A series of top edge connectors have been developed to standardize common applications. Section 4.2.4 describes the top edge connector standards.

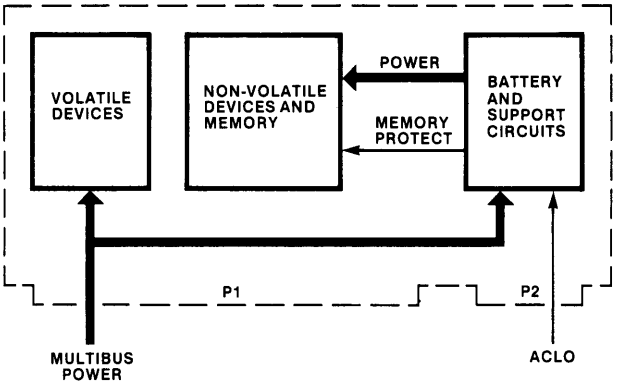
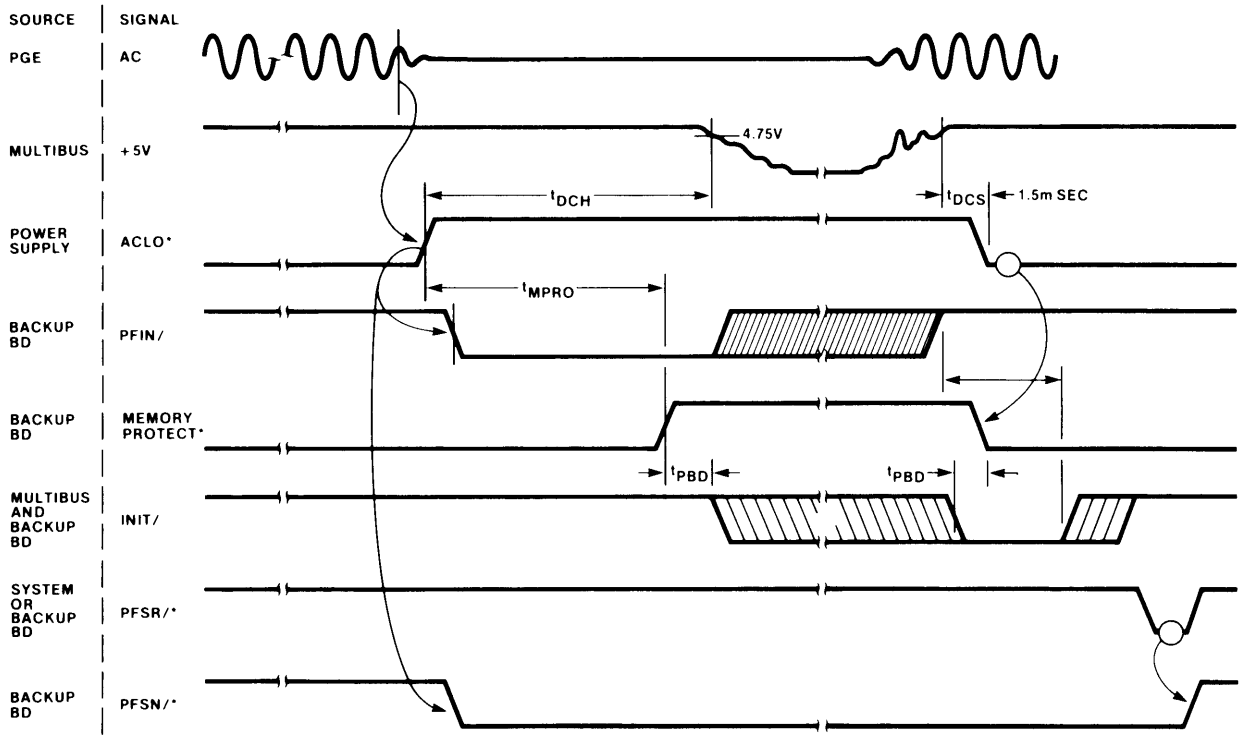


Figure 5-36. Power Fail Circuit Diagram Using On Board Backup Source



* THE DEVICE WHICH CONTROLS THIS SIGNAL IS BACKED-UP.

Figure 5-37. Power Fail AC Timing With On Board Backup Source

Table 5-3. Recommended Power Supply Specifications

	Standard				Optional					
					Analog Power		Battery Power Backup			
	Ground	+5	+12	-12	+15	-15	+5	+12	-12	-5
Mnemonic	GND	+5V	+12V	-12V	+15V	-15V	+5B	+12B	-12B	-5B
Bus Pins	P1+1,2, 11,12, 75,76, 85,86	P1+3,4 5,6,81, 82,83, 84	P1+7,8	P1+79, 80	P2+23,24	P2+25,26	P2+3,4, 5,6	P2+11, 12	P2+15, 16	P2-7, 8
Nominal Output	Ref.	+5.0V	+12.0V	-12.0V	+15.0V	-15.0V	+5.0V	+12.0V	-12.0V	-5.0V
Adjustable Range from Nominal	Ref.	±5%	±5%	±5%	±5%	±5%	±5%	±5%	±5%	±5%
Initial Setting from Nominal[1]	Ref.	±1%	±1%	±1%	±1%	±1%	±1%	±1%	±1%	±1%
Combined Line & Load Reg.[2]	Ref.	±2%	±2%	±2%	±0.3%	±0.3%	±2%	±2%	±2%	±2%
Periodic & Random Noise (Pk-Pk)[3]	Ref.	50mV	50mV	50mV	10mV	10mV	50mV	50mV	50mV	50mV
Transient Response[4]		500μs	500μs	500μs	100μs	100μs	500μs	500μs	500μs	500μs
Transient Deviation[5]		±10%	±10%	±10%	±10%	±10%	±10%	±10%	±10%	±10%
OVP from Nominal (minimum)	Ref.	±110%	±110%	±110%	±110%	±110%	±110%	±110%	±110%	±110%
OVP from Nominal (maximum)	Ref.	±135%	±135%	±135%	±120%	±120%	±135%	±135%	±135%	±135%
Voltage Temperature Coefficient[6]		±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%
Temperature Range	0-55°C (32-131°F)				0+55°C		0+55°C			
Humidity	90% MAX RELATIVE (NO CONDENSATION)									

NOTES:

1. Resolution of output adjustment must be within this tolerance.
2. As measured from the initial voltage for ±10% line variations and 0% to 100% load.
3. As measured over a bandwidth not to exceed 0 to 5 mHz.
4. As measured from the start of a ±50% load change to the time the output recovers to within ±0.1% of final voltage. Outputs shall be properly terminated with adequate capacitance filtering.
5. Measured as the peak deviation from the initial voltage.
6. Measured from the initial output voltage.

Table 5-4. Bus Module D.C. Mnemonic Definitions

Signal	Symbol	Description	Test Condition	Min	Max	Units
Output	V_{OL}	Output Low Voltage	I_{OL} = X mA		X	V
	V_{OH}	Output High Voltage	I_{OL} = X mA	X		V
	I_{LH}	Output Leakage High	V_O = X V		X	μA
	I_{LL}	Output Leakage Low	V_O = X V		X	μA
	C_L	Capacitive	Estimate Only Not Guaranteed		X	pF
Input	V_{IL}	Input Low Voltage				
	V_{IH}	Input High Voltage		X		V
	I_{IL}	Input Current At Low V	V_{IN} = X		X	mA
	I_{IN}	Input Current At High V	V_{IN} = X		X	mA
	C_L	Capacitive Load	Estimate Only Not Guaranteed		X	pF
Bidirectional	V_{OL}	Output Low Voltage	I_{OL} = X mA		X	V
	V_{OH}	Output High Voltage	I_{OH} = X mA	X		V
	V_{IL}	Input Low Voltage			X	V
	V_{IH}	Input High Voltage		X		V
	I_{IL}	Input Current At Low V	V_{IN} = XV		X	mA
	I_{LH}	Output Leakage At High V	V_O = XV		X	μA
	I_{IL}	Output Leakage At Low V	V_O = XV		X	μA
	C_L	Capacitive Load	Estimate Only Not Guaranteed		X	pF

All A.C. and D.C. specifications should be actual values on MULTIBUS specifications. An example is specifying actual address set-up (45 ns) and hold (30 ns) times of a slave module versus specifying 50 ns.

5.7 BUS TERMINATION CONSIDERATIONS

A summary of bus termination resistors is given in Table 5-7. These resistors must be connected to the bus for proper bus operation to occur. These resistors can be located anywhere along the bus except in the case of the B and C clock. The terminating resistors for B and C clock should be at the opposite end of the bus from the source of the clocks. Best results occur if all the bus termination resistors are placed at the end of the bus.

5.8 MISCELLANEOUS CONSIDERATIONS

This section contains miscellaneous MULTIBUS information.

5.8.1 NON-STANDARD VOLTAGES

Figure 5-40 shows a method of generating the non-standard -5 Volts.

5.8.2 BUS IC LOCATIONS

In general, all traces between the bus connectors (P1 and P2) should be minimized to reduce capitance and coupling.

5.8.3 TIME OUT GENERATION

Figure 5-41 illustrates a method of generating the Bus Timeout signal.

Table 5-5. Slave AC Timing Mnemonic Definitions

Parameter	Description	Specify
t_{AS}	ADDRESS SET-UP	Min
t_{DS}	WRITE DATA SET-UP	Min
t_{AH}	ADDRESS HOLD TIME	Max
t_{DHW}	DATA HOLD TIME FOR WRITE	Max
t_{DHR}	DATA HOLD TIME FOR READ	Max
t_{DXL}	READ DATA SET-UP TO XACK	Min
t_{CMD}	COMMAND WIDTH	Min
t_{CS}	COMMAND SEPARATION	Min
t_{XAH}	ACKNOWLEDGE HOLD TIME	Max
t_{INT}	INIT PULSE WIDTH	MIN
t_{ACC}	CMD TO DATA VALID (READ)	Max
t_{XACK}	CMD TO OPERATION COMPLETE	Max
t_{ID}	INHIBIT DELAY	Max
t_{CY}	CYCLE TIME OF BOARD	Max
t_{IS}	INHIBIT SET-UP TIME	Max
t_{IH}	INHIBIT HOLD TIME	Max

Table 5-6. Master AC Timing Mnemonic Definitions

Parameter	Descriptions	Specify
t_{AH}	ADDRESS HOLD TIME	Min
t_{AS}	ADDRESS SET-UP	Min
t_{BCY}	BUS CLOCK PERIOD	Max, Min
t_{BPNS}	BPRN SET-UP	Max
t_{BW}	BUS CLOCK WIDTH	Max, Min
t_{CBRD}	CBRQ DELAY	Max
t_{CBRS}	CBRQ SET-UP	Max
t_{CCY}	C CLOCK PERIOD	Max, Min
t_{CMD}	COMMAND WIDTH	Min
t_{CSEP}	COMMAND SEPARATION	Min
t_{CW}	C CLOCK WIDTH	Max, Min
t_{CY}	CPU CYCLE TIME	Max, Min
t_{DBO}	BPRO DELAY	Max
t_{DBQ}	BREQ DELAY	Max
t_{DBY}	BUSY DELAY TIME	Max
t_{LCKH}	LOCK/ HOLD TIME	Min
t_{LCKS}	LOCK/ SETUP TIME	Min
t_{LOCK}	LOCK/ WIDTH	Max
t_{DHR}	DATA HOLD TIME FOR READ	Min
t_{DHW}	DATA HOLD TIME FOR WRITE	Min
t_{DS}	WRITE DATA SET-UP	Min
t_{DSYS}	BUSY/SETUP TIME TO ↓ BLCK/	Min
t_{DXL}	READ DATA SET-UP TIME TO XACK	Min
t_{INIT}	INIT PULSE WIDTH	Min
t_{INTA}	INTA COMMAND WIDTH	Min
t_{NOD}	BPRN TO BPRO DELAY	Max
t_{XAH}	ACKNOWLEDGE HOLD TIME	Min
ACKW	XACK ↓ TO WRT CMD ↑	Min

Table 5-7. Bus Termination Resistor Values

PRIMARY (P1)				
Bus Signals	**Termination**			
	Location	**Type**	**R**	**Units**
DAT0/-DATF/ (16 lines)	Mother-board	Pullup	2.2	KΩ
ADR0/-ADRF/ ADR10/-ADR13/ BHEN/ (21 lines)	Mother-board	Pullup	2.2	KΩ
MRDC/,MWTC/	Mother-board	Pullup	1	KΩ
IORC/,IOWC	Mother-board	Pullup	1	KΩ
XACK/	Mother-board	Pullup	510	Ω
INH1/,INH2/	Mother-board	Pullup	1	KΩ
BCLK/	Mother-board	To +5V To GND	220 330	Ω Ω
BREQ/	Central Priority Module (not req)	Pullup	1	KΩ
BPRO/	(not req)			
BPRN/	(not req)			
BUSY/,CBRQ/	Mother-board	Pullup	1	KΩ
INIT/	Mother-board	Pullup	1	KΩ
CCLK/	Mother-board	To +5V To GND	220 330	Ω Ω
INTA/	Mother-board	Pullup	1	KΩ
INT0/-INT7/ (8 lines)	Mother-board	Pullup	1	KΩ
LOCK/	Mother-board	Pullup	1	KΩ
	OPTIONAL (P2)			
ADR14/-ADR17/	Mother-board	Pullup	2.2	KΩ
PFSF/	Driver	Pullup	1	KΩ
PFSN/	Driver	Pullup	1	KΩ
ACLO	Power Supply	Pullup	1	KΩ
PFIN/	Driver	Pullup	1	KΩ
MPRO/	Driver	Pullup	1	KΩ
Reset/	None			

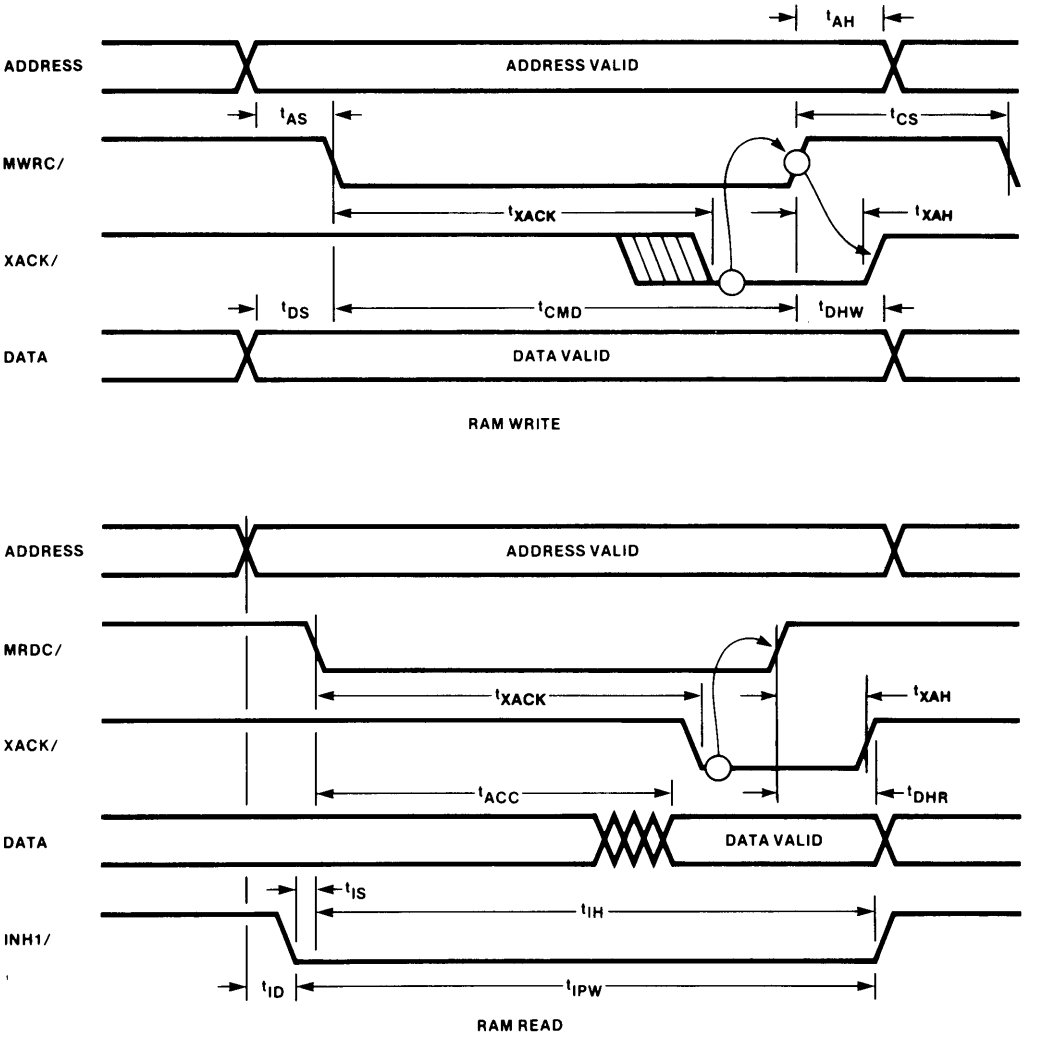


Figure 5-38a. Slave AC Timing

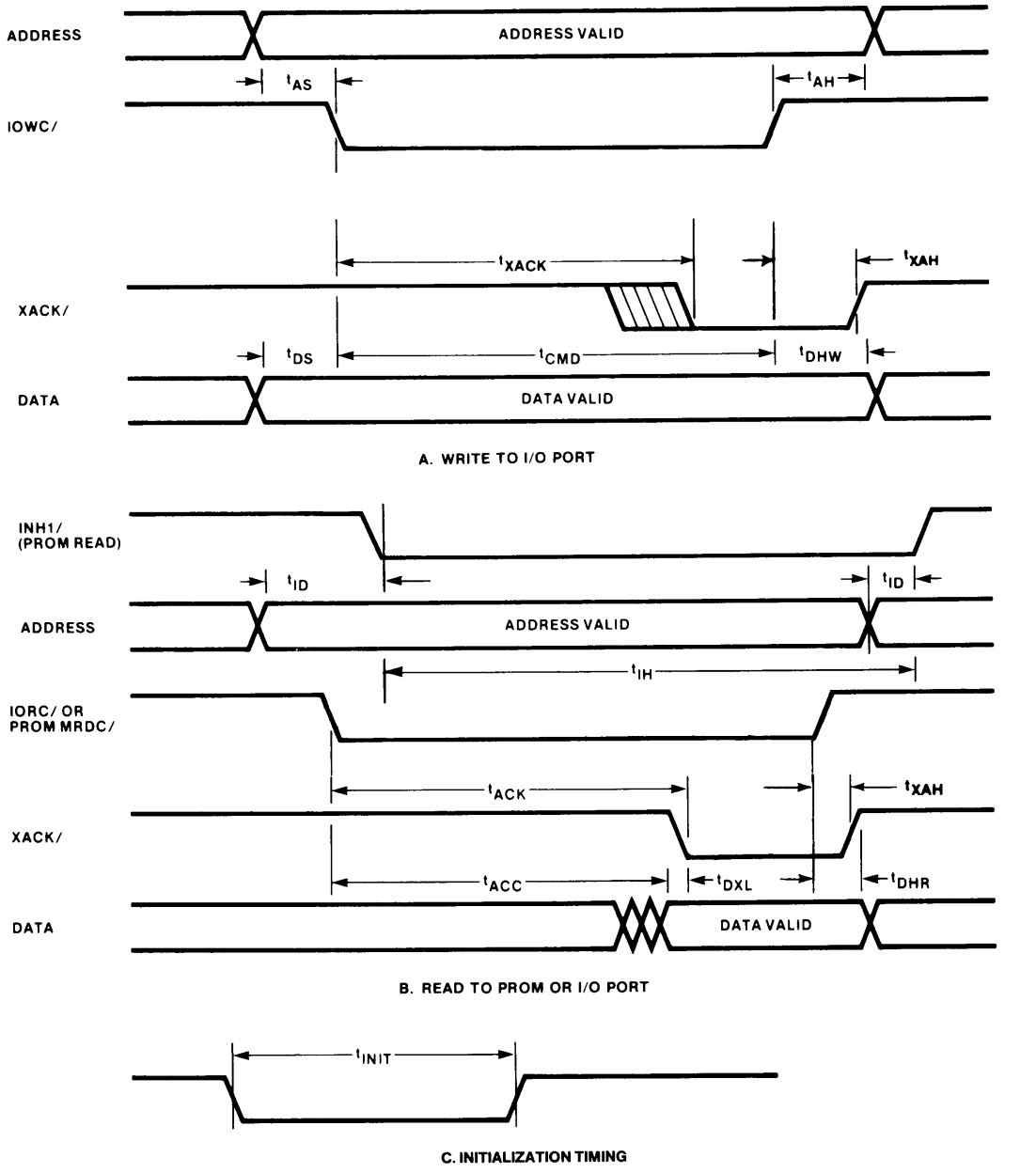


Figure 5-38b. Slave AC Timing

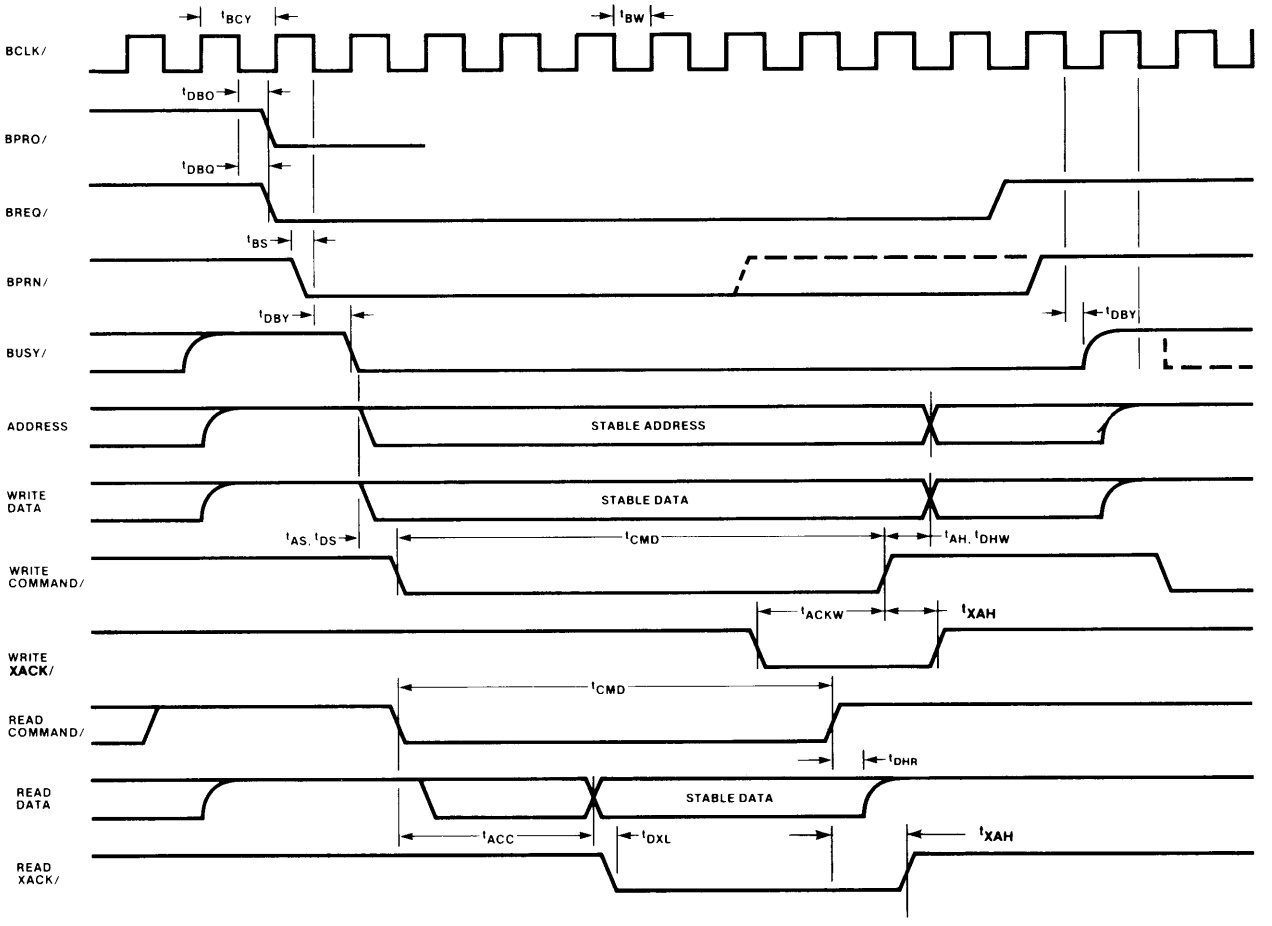


Figure 5-39. Master AC Timing

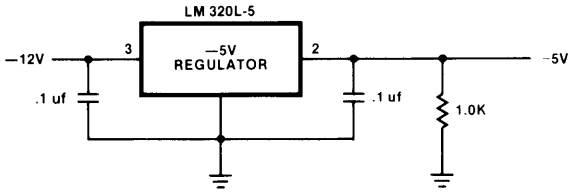


Figure 5-40. -5V Generation

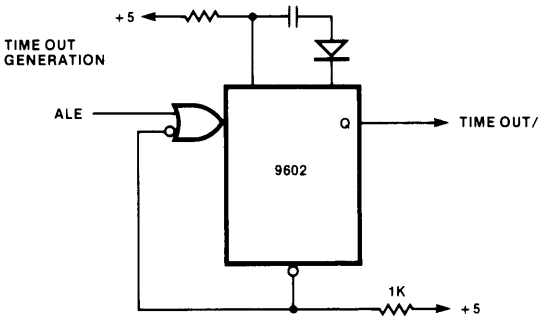


Figure 5-41. Bus Timeout Generation

SECTION 6
LEVELS OF COMPLIANCE

6.0 INTRODUCTION

This section presents the concept and notation of levels of compliance with the MULTIBUS as follows:

1. Variable Elements of capability composing the essence of MULTIBUS compliance.
2. General discussion of compliance relationship for masters and slaves.
3. Notation for describing levels fo compliance with the MULTIBUS.

The notation of levels of compliance is introduced to facilitate the use of MULTIBUS products of varying capability. It bounds the variability allowed within the MULTIBUS specification and provides a succinct and convenient notation for these variables.

6.1 VARIABLE ELEMENTS OF CAPABILITY

The MULTIBUS is very versatile allowing systems to be constructed with boards of varying capability. The MULTIBUS allows for variations in data path width, I/O address path width, and interrupt attributes. In addition it is recognized that some products have differing memory address path width.

6.1.1 DATA PATH

The MULTIBUS allows for both 8- and 16-bit data path products. The 16-bit data path products use the byte swapping technique described in section 2.2.2.4, thus allowing the 8- and 16-bit products to work together.

6.1.2 MEMORY ADDRESS PATH

The MULTIBUS designates a 24-bit address path. In many systems a 16- or 20-bit address path may be sufficient, though not fully MULTIBUS compatible.

6.1.3 I/O ADDRESS PATH

The MULTIBUS allows for both 8- and 16-bit I/O address paths. The 16-bit path products must also be configurable to act as 8-bit path products.

6.1.4 INTERRUPT ATTRIBUTES

The MULTIBUS (section 2.3) allows for considerable variety in interrupt attributes. A product may support no interrupts, Non Bus Vectored (NBV) interrupts, two-cycle bus vectored interrupts, and three-cycle bus vectored interrupts. There are two methods of interrupt sensing: the preferred level-triggered; and for historical compatibility only, edge-level-triggered.

> Level-Triggered. The active level of the request line indicates an active request. Requiring no edge to trigger an interrupt allows several sources to be attached to a single request line. Sources for level-triggered sense inputs should provide a programmatic means to clear the interrupt request.
>
> Edge-Level-Triggered. The transition from the inactive to the active level indicates an active request if and only if the active level is maintained at least until it has been recognized by the master. The requirement for a transition precludes multiple sources on a request line. But, Edge-Level triggering removes the requirement that the source have a programmatic means to clear the interrupt request.

NOTE

> Edge-Level-Triggering is described only to allow for historical compatibility. New designs shall use level-triggered interrupt sensing.

A master may support either or both of the above interrupt sensing methods. It is necessary to configure the system such that the source of the interrupt requests correspond to the interrupt sensing method of the master. Note that a source which is compatible with Level-Triggering is also compatible with Edge-Level triggering.

6.2 MASTERS AND SLAVES

When constructing MULTIBUS systems it is not necessary that all modules have identical capabilities. One may for instance have a master with an 8/16-bit data path and a slave with an 8-bit data path. The system is completely functional, though the application must restrict itself to 8-bit access to the slave.

The key concept when constructing a MULTIBUS system is that of required capability versus supplied capability. Each product will provide some set of capability. A transaction between two such products will be restricted to use that capability which is the intersection of the sets of capability of the two products. In some cases the intersection may be null implying fundamental incompatibility. It is the responsibility of the system designer to assure the viability of this intersection.

6.3 COMPLIANCE LEVEL NOTATION

A notation is introduced which allows a vendor to succinctly and accurately specify a product's level of compliance with the MULTIBUS. For boards which may act as either masters or slaves, the compliance levels must be specified for both cases. Increasing levels of comliance subsume lesser levels for data path width, memory address path width and I/O address path width. Interrupt attributes are listed separately as they are independent of one another. The lack of an element (i.e., no I/O address path) specification normally implies no capability for this element.

6.3.1 DATA PATH

D8 represents an 8 bit data path
D16 represents an 8/16 bit data path

6.3.2 MEMORY ADDRESS PATH

M16 represents a 16 bit memory address path
M20 represents a 20 bit memory address path
M24 represents a 24 bit memory address path

6.3.3 I/O ADDRESS PATH

I8 represents an 8 bit I/O address path
I16 represents an 8 or 16 bit I/O address path

6.3.4 INTERRUPT ATTRIBUTES

V0 represents Non Bus Vectoed interrupt requests
V2 represents two cycle bus vectored interrupt requests

V3 represents three cycle bus vectored interrupt requests

E represents Edge-level triggering only
L represents Level triggering only

The interrupt attributes notation can be concatenated to represent multiple capabilities.

6.3.5 AN EXAMPLE

A versatile combination I/O and memory slave board which supports an 8/16 bit data path, a 20-bit memory address, an 8- or 16-bit I/O address, NBV interrupt requests, two- and three-cycle bus vectored interrupt requests would be specified as follows:

MULTIBUS Compliance:
Slave D16 M20 I16 VO23 L

6.3.6 COMPLIANCE MARKING

The compliance level of a card shall be clearly marked on the printed circuit board as well as in the printed specifications.

APPENDIX A
MULTIBUS CONNECTIONS P1 AND P2 SIGNAL DEFINITIONS

MULTIBUS Connectors P1 and P2 Signal Definitions.

Table A-1 and A-2 contain definitions of the signals which appear on the Multibus connector (P1) and the Auxiliary connector (P2). Tables A-3 and A-4 contain connector pin assignments for P1 and P2.

Table A-1. MULTIBUS Connector (P1) Signal Definitions

SIGNAL	FUNCTIONAL DESCRIPTION
ADR0/-ADRF/ ADR10/-ADR13/	*Address.* These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0/ (when active) enables the even byte bank (DAT0/-DAT7/) on the Multibus; i.e., ADR0/ is active for all even addresses. ADR13/ is the most significant address bit for 20 bit addressing.
BCLK/	*Bus Clock.* Used to synchronize the bus contention logic on all bus masters.
BHEN/	*Byte High Enable.* When active low, enables the odd byte bank (DAT8/ - DATF/) onto the Multibus.
BPRN/	*Bus Priority In.* When low indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	*Bus Priority Out.* In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	*Bus Request.* In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	*Bus Busy.* Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	Common Bus Request. Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
CCLK/	*Constant Clock.* Provides a clock signal of constant frequency for use by other system modules.
DAT0/ - DATF/	*Data.* These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most-significant bit. For data byte operations, DAT0/ - DAT7/ is the even byte and DAT8/ - DATF/ is the odd byte.
INH1/	*Inhibit RAM.* For system applications, allows iSBC dual port RAM addresses to be overlayed by ROM/PROM or memory mapped I/O devices. Ths signal has no effect of local CPU access of its dual port RAM.
INH2/	*Inhibit ROM.* For system applications, allows ROM/PROM addresses to be overlayed by auxilliary ROM devices (e.g., a bootstrap program).
INIT/	*Initialize.* Reset the entire system to a known internal state.
INTA/	*Interrupt Acknowledge.* This signal is issued in response to an interrupt request.

Table A-1. MULTIBUS Connector (P1) Signal Definitions (Cont'd.)

SIGNAL	FUNCTIONAL DESCRIPTION
INT0/ - INT7/	*Interrrupt Request.* These eight lines transmit interrupt Requests to the appropriate interrupt handler. INT0 has the highest priority.
IORC/	*I/O Read Command.* Indicates that the address of an I/O port is on the Multibus address lines and that the output of that port is to be read (placed) onto the Multibus data lines.
IOWC/	*I/O Write Command.* Indicates that the address of an I/O port is on the Multibus address lines and that the contents on the Multibus data lines are to be accepted by the addressed port.
LOCK/	*Lock.* Indicates a locked access is being performed on the MULTIBUS.
MRDC/	*Memory Read Command.* Indicates that the address of a memory location is on the Multibus address lines and that the contents of that location are to be read (placed) on the Multibus data lines.
MWTC/	*Memory Write Command.* Indicates that the address of a memory location is on the Multibus address lines and that the contents on the Multibus data lines are to be written into that location.
XACK/	*Transfer Acknowledge.* Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the Multibus data lines.

Table A-2. Auxiliary Connector (P2) Signal Definitions

SIGNAL	FUNCTIONAL DESCRIPTION
ACLO	*AC Low.* Indicates a loss of AC voltage.
ADR14/- ADR17/	*Address.* These 4 lines are the 4 most significant address bits in 24 bit addressing.
ALE	*Address Latch Enable.* Generated by CPU to provide auxiliary address latch.
HALT/	*Halt.* Indicates that the master CPU is halted.
MPRO/	*Memory Protect.* This externally generated signal prevents access to the dual port RAM during battery backup operation.
PFIN/	*Power Fail Interrupt.* This signal from the power supply interrupts the processor when a power failure occurs.
PFSN/	*Power Fail Sense.* Provides a latch for power failure event.
PFSR/	*Power Fail Reset.* Used to reset power fail sense latch.
RESET/	*Reset.* This externally generated signal initiates a power-up sequence.
WAIT/	*Bus Master Wait State.* This signal indicated that the processor is in a wait state.

Table A-3. Pin Assignment of Bus Signals on Multibus Board Connector (P1)

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9		Reserved, bussed	10		Reserved, bussed
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 disable RAM
BUS CONTROLS AND ADDRESS	25	LOCK/	Lock	26	INH2/	Inhibit 2 disable PROM or ROM
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Intr Acknowledge	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	−12V	−12Vdc	80	−12V	−12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Table A-4. P2 Connector PIN Assignment of Bus Signals

PIN	(COMPONENT SIDE) MNEMONIC	DESCRIPTION	PIN	(CIRCUIT SIDE) MNEMONIC	DESCRIPTION
1	GND	Signal GND	2	GND	Signal GND
3	5VB	+5V Battery	4	GVB	+5V Battery
5		Reserved, not bussed	6	EEVPP	E²PROM Power
7	5VB	-5V Battery	8	-5VB	-5V Battery
9		Reserved, not bussed	10		Reserved, not bussed
11	12VB	+12V Battery	12	12VB	+12V Battery
13	PFSR/	Power Fail Sense Reset	14		Reserved, not bussed
15	-12VB	-12V Battery	16	-12VB	-12V Battery
17	PFSN/	Power Fail Sense	18	ACLO	AC Low
19	PFIN/	Power Fail Interrupt	20	MPRO/	Memory Protect
21	GND	Signal GND	22	GND	Signal GND
23	+15V	+15V	24	+15V	+15V
25	-15V	-15V	26	-15V	-15V
27	PAR1/	Parity 1	28	HALT/	Bus Master HALT
29	PAR2/	Parity 2	30	WAIT/	Bus Master WAIT STATE
31	PLC	Power Line Clock	32	ALE	Bus Master ALE
33	↕		34		Reserved, not bussed
35		Reserved, not bussed	36	BD RESET/	Board Reset
37			38	AUX RESET/	Reset switch
39			40		Reserved, not bussed
41	↕		42	↕	
43			44		
45			46		Reserved, bussed
47		Reserved, bussed	48		
49			50		
51			52		
53			54		
55	ADR16/	Address	56	ADR17/	Address
57	ADR14/	Bus	58	ADR15/	Bus
59		Reserved, bussed	60		Reserved, bussed

Notes:
1. PFIN, on slave modules, if possible, should have the option of connecting to INT0/ on P1.
2. All undefined pins are reserved for future use.

APPENDIX B
ELECTRICAL SPECIFICATION SUMMARY

Tables B-1 through B-3 summarize the electrical specifications of the MULTIBUS.

Table B-1. Bus Timing Specifications Summary

Parameter	Description	Minimum	Maximum	Units	Sections To Reference
t_{BCY}	Bus Clock Period	100	D.C.	ns	3.2.5
t_{BW}	Bus Clock Width	0.35 t_{BCY}	0.65 t_{BCY} (not restricted)		3.2.5
t_{SKEW}	BCLK/skew		3	ns	3.2.5
t_{PD}	Standard Bus Propagation Delay		3		3.1.2, 3.2.5
t_{AS}	Address Set-Up Time (at Slave Board)	50		ns	3.2.1, 3.2.2, 3.2.4
t_{AD}	Address Disable		100	ns	
t_{DS}	Write Data Set Up Time	50		ns	3.2.2
t_{AH}	Address Hold Time	50		ns	3.2.1, 3.2.2, 3.2.4
t_{DHW}	Write Data Hold Time	50		ns	3.2.2
t_{DXL}	Read Data Set Up Time To XACK	0		ns	3.2.1, 3.2.4
t_{DHR}	Read Data Hold Time	0	65	ns	3.2.1, 3.2.4
t_{XAH}	Acknowledge Hold Time	0	65	ns	3.2.1, 3.2.2, 3.2.4
t_{XACK}	Acknowledge Time	0	8	μs	3.2.1,3.2.2, 3.2.4
t_{CMD}	Command Pulse Width	100	t_{TOUT}	ns	3.2.1, 3.2.2
t_{ID}	Inhibit Delay	0	100 (Recommend < 100 ns)	ns	3.2.3
t_{XACKA}	Acknowledge Time of of an Inhibited Slave	t_{IAD} + 50ns	1500	ns	3.2.3
t_{XACKB}	Acknowledge Time of an Inhibiting Slave	1.5	8	μs	3.2.3
t_{IAD}	Acknowledge Disable from Inhibit (An internal parameter on an inhibited slave; used to determine t_{XACKA} Min.)	0	100 (arbitrary)	ns	2.3.2
t_{AIZ}	Address to Inhibits High delay		100	ns	3.2.3
t_{INTA}	INTA/ Width	250		ns	3.2.4
t_{CSEP}	Command Separation	100		ns	3.2.4, 3.2.6

Table B-1. Bus Timing Specifications Summary (Cont'd.)

Parameter	Description	Minimum	Maximum	Units	Sections To Reference
t_{BREQL}	↓BCLK/ to BREQ/ Low Delay	0	35	ns	3.2.5
t_{BREQH}	↓BCLK/ to BREQ/ High Delay	0	35	ns	3.2.5
t_{BPRNH}	BPRN to ↓BCLK/HOLD	5		ns	
t_{BPRNS}	BPRN/ to ↓BCLK/ Setup Time	22		ns	3.2.5
t_{BUSY}	BUSY/ delay from ↓BCLK/	0	70	ns	3.2.5
t_{BUSYS}	BUSY/ to ↓BCLK/ Setup Time	25		ns	3.2.5
t_{BPRO}	↓BCLK/ to BPRO/ (CLK to Priority Out)	0	40	ns	3.2.5
t_{BPRNO}	BPRN/ to BPRO/ (Priority In to Out)	0	30	ns	3.2.5
t_{CBRO}	↓BCLK/ to CBRQ/ (CLKto Common Bus Request)	0	60	ns	3.2.5
t_{CBRQS}	CBRQ/ to ↓BCLK/ Setup Time	35		ns	3.2.5
t_{XCD}	XACK↓ to Command↑ Delay	20		ns	3.2.1 3.2.2
t_{BSYO}	CBRQ/↓ and BUSY/↓ to BUSY/↑	—	12	μs	3.2.5
t_{LCKH}	LOCK/ hold time from Command/↓	100		ns	3.2.6
t_{LCKS}	LOCK/ to command setup time	100		ns	3.2.6
t_{LOCK}	LOCK/ Width		12	μs	3.2.6
t_{CCY}	C-clock Period	100	110	ns	3.2.6
t_{CW}	C-clock Width	0.35 t_{CCY}	0.65 t_{CCY}	ns	3.2.6
t_{INIT}	INIT/Width	5		ms	3.2.6 3.2.7
t_{INITS}	INIT/ to MPRO/ Setup Time	100		ns	3.2.7
t_{PBD}	Power Backup Logic Delay	0	200	ns	3.2.7
t_{PFINW}	PFIN/ Width	2.5		ms	3.2.7
t_{MPRO}	MPRO/ Delay	2.0	2.5	ms	3.2.7
t_{ACLOW}	ACLO/ Width	3.0		ms	3.2.7
t_{PFSRW}	PFSR/ Width	100		ns	3.2.7
t_{TOUT}	Timeout Delay	1	∞ (DC)	ms	—
t_{DCH}	D.C. Power Supply Hold from ALCO/	3.0		ms	3.2.7
t_{DCS}	D.C. Power Supply Setup to ACLO/	1		ms	3.2.7

Table B-2. Bus Power Supply Specifications

	Standard				Optional					
					Analog Power		Battery Power Backup			
	Ground	+5	+12	-12	+15	-15	+5	+12	-12	-5
Mnemonic	GND	+5V	+12V	-12V	+15V	-15V	+5B	+12B	-12B	-5B
Bus Pins	P1+1,2, 11,12, 75,76, 85,86	P1+3,4 5,6,81, 82,83, 84	P1+7,8	P1+79, 80	P2+23,24	P2+25,26	P2+3,4, 5,6	P2+11, 12	P2+15, 16	P2-7, 8
Nominal Output	Ref.	+5.0V	+12.0V	-12.0V	+15.0V	-15.0V	+5.0V	+12.0V	-12.0V	-5.0V
Adjustable Range from Nominal	Ref.	±5%	±5%	±5%	±5%	±5%	±5%	±5%	±5%	±5%
Initial Setting from Nominal[1]	Ref.	±1%	±1%	±1%	±1%	±1%	±1%	±1%	±1%	±1%
Combined Line & Load Reg.[2]	Ref.	±2%	±2%	±2%	±0.3%	±0.3%	±2%	±2%	±2%	±2%
Periodic & Random Noise (Pk-Pk)[3]	Ref.	50mV	50mV	50mV	10mV	10mV	50mV	50mV	50mV	50mV
Transient Response[4]		500μs	500μs	500μs	100μs	100μs	500μs	500μs	500μs	500μs
Transient Deviation[5]		±10%	±10%	±10%	±10%	±10%	±10%	±10%	±10%	±10%
OVP from Nominal (minimum)	Ref.	±110%	±110%	±110%	±110%	±110%	±110%	±110%	±110%	±110%
OVP from Nominal (maximum)	Ref.	±135%	±135%	±135%	±120%	±120%	±135%	±135%	±135%	±135%
Voltage Temperature Coefficient[6]		±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%	±0.03%
Temperature Range	0-55°C (32-131°F)				0+55°C		0+55°C			
Humidity	90% MAX RELATIVE (NO CONDENSATION)									

NOTES:

1. Resolution of output adjustment must be within this tolerance.
2. As measured from the initial voltage for ±10% line variations and 0% to 100% load.
3. As measured over a bandwidth not to exceed 0 to 5 mHz
4. As measured from the start of a ±50% load change to the time the output recovers to within ±0.1% of final voltage. Outputs shall be properly terminated with adequate capacitance filtering.
5. Measured as the peak deviation from the initial voltage.
6. Measured from the initial output voltage.

Table B-3. Bus Drivers, Receivers, and Terminations

Driver 1,3						Receiver 2,3				Termination			
Bus Signals	Location	Type	I_{OL} Min_{ma}	I_{OH} $Min_{\mu a}$	C_O Min_{pf}	Location	I_{IL} Max_{ma}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	Location	Type	R	Units
DAT0/→DATF/ (16 lines)	Masters and Slaves	TRI	16	−2000	300	Masters and Slaves	−0.8	125	18	Mother-board	Pull up	2.2	KΩ
ADR0/-ADR13/, BHEN/ (25 lines)	Masters	TRI	16	−2000	300	Slaves	−0.8	125	18	Mother-board	Pull up	2.2	KΩ
MRDC/,MWTC/	Masters	TRI	32	−2000	300	Slaves (Memory; memory-mapped I/O)	−2	125	18	Mother-board	Pull up	1	KΩ
IORC/,IOWC/	Masters	TRI	32	−2000	300	Slaves (I/O)	−2	125	18	Mother-board	Pull up	1	KΩ
XACK/	Slaves	TRI	32	−2000	300	Masters	−2	125	18	Mother-board	Pull up	510	Ω
INH1/,INH2/	Inhibiting Slaves	O.C.	16	—	300	Inhibited Slaves (RAM, PROM, ROM, Memory Mapped I/O)	−2	50	18	Mother-board	Pull up	1	KΩ
BCLK/	1 place (Master)	TTL	48	−3000	300	Master	−2	125	18	Mother-board	To +5V To GND	220 330	Ω Ω
BREQ/	Each Master	TTL	10	−200	60	Central Priority Module	−2	50	18	Central Priority Module (not req)	Pull up	1	KΩ
BPRO/	Each Master	TTL	3.2	−200	60	Next Master in Serial Priority Chain at its BPRN/	−3.2	100	18	(not req)			
BPRN/	Parallel: Central Priority Module Serial: Prev Masters BPRO/	TTL	3.2	−200	60	Master	−3.2	100		(not req)			
LOCK/	Master	TRI	32	−2000	300	All	−2	125	18	Mother-board	Pull up	1	KΩ
BUSY/,CBRQ/	All Masters	O.C.	20	—	300	All Masters	−2	50	18	Mother-board	Pull up	1	KΩ
INIT/	Master	O.C.	32	—	300	All	−2	50	18	Mother-board	Pull up	1	KΩ
CCLK/	1 place	TTL	48	−3000	300	Any	−2	125	18	Mother-board	To +5V To GND	220 330	Ω Ω
INTA/	Masters	TRI	32	−2000	300	Slaves (Interrupting I/O)	−2	125	18	Mother-board	Pull up	1	KΩ
INT0/ → INT7/ (8 lines)	Slaves	O.C.	16	—	300	Masters	−1.6	40	18	Mother-board	Pull up	1	KΩ
PFSR/	User's Front Panel	TTL	16	−400	300	Slaves, Masters	−1.6	40	18	Driver	Pull up	1	KΩ
PFSN/	Power Back-Up Unit	TTL	16	−400	300	Masters	−1.6	40	16	Driver	Pull up	1	KΩ
ACLO	Power Supply	O.C.	16	−400	300	Slaves, Masters	−1.6	40	18	Power Supply	Pull up	1	KΩ
PFIN/	Power Back-Up Unit	O.C.	16	−400	300	Masters	−1.6	40	18	Driver	Pull up	1	KΩ
MPRO/	Power Back-Up Unit	TTL	16	−400	300	Slaves Masters	−1.6	40	18	Driver	Pull up	1	KΩ

Table B-3. Bus Drivers, Receivers, and Terminators (Cont'd.)

Driver 1,3						Receiver 2,3				Termination			
Bus Signals	Location	Type	I_{OL} Min_{ma}	I_{OH} $Min_{\mu a}$	C_O Min_{pf}	Location	I_{IL} Max_{ma}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	Location	Type	R	Units
Aux Reset/	User's Front Panel	Switch to GND	—	—	—	Masters	-2	50	18	Note: 5			

Notes:

1. Driver Requirements

   I_{OH} = High Output Current Drive
   I_{OL} = Low Output Current Drive
   C_O = Capacitance Drive Capability
   TRI = 3-State Drive
   O.C. = Open Collector Driver
   TTL = Totem-pole Driver

2. Receiver Requirements

   I_{IH} = High Input Current Load
   I_{IL} = Low Input Current Load
   C_I = Capacitive Load

3. For Low and High Voltages specifications (see Section 3.1.1).

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