

Figure 21. Temperature Sensor Flow Diagram

DEG. C	THERMISTOR OHMS	(.7) (1 $\mu$ ) (R <sub>T</sub> ) APPROX. TIME (ms)	START WITH 3FFE <sub>H</sub> APPROX. COUNT LEFT (HEX)
20	12,490	.874	3585
21	11,940	.836	35FA
22	11,420	.799	366A
23	10,920	.764	36D5
24	10,450	.732	373A
25	10,000	.7	3772
26	9,573	.670	37D0
27	9,167	.642	384D
28	8,777	.614	38A1
29	8,407	.588	38F1
30	8,057	.564	393C
31	7,723	.541	3984
32	7,403	.518	39C8
33	7,097	.497	3A0A
34	6,807	.476	3A48
35	6,530	.457	3A84
36	6,267	.439	3ABC
37	6,017	.421	3AF2
38	5,747	.402	3B2C
39	5,547	.388	3B57
40	5,327	.373	3B86
41	5,117	.358	3BB3


8085A Cycle Time = 326 ns

Oneshot Approx. Time =

L<sub>N2</sub> (CEXT) (REXT)

≈ (.7) (1 $\mu$ ) R<sub>THERMISTOR</sub>

Table 8. Thermistor Resistance Mapping



**UNI-CURVE  
THERMISTOR**

INTERCHANGEABLE  
CURVE MATCHED

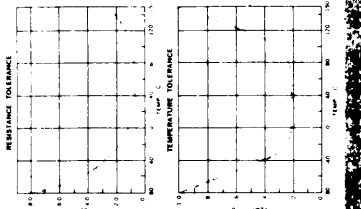
UNI-CURVE  
PART NUMBER  
UNI-CURVE

**UNI-CURVE INTERCHANGEABLE THERMISTOR**

UNI-CURVE INTERCHANGEABLE THERMISTOR  
PART NUMBER: 8085A  
RESISTANCE: 10,000 OHMS  
TOLERANCE: ±1%

RESISTANCE TOLERANCE

TEMPERATURE TOLERANCE



For an example with N = 256, CC = .32  $\mu$ sec at 3.125 MHz;  
 Byte time = 6.7  $\mu$ sec. A match search routine with minimum  
 memory usage is given below:

Search	Cmp M	compare byte
	RZ	return if match
	INX H	else increment pointer
	DCR C	has the entire
	JNZ search	block been searched?
	STC	If so set no match flag
	RET	and return.

In this application, a user may want to have several tempera-  
 ture ranges which can be swapped in and out with a block  
 move subroutine. Similar code can be developed for this as  
 shown below for a 4 byte move group:

BLKMOV	LXI H, 000H	clear HL
	DAD SP	move SP to HL
	SHLD SAVESP	save sP
	MOV H, B	move Block move
	MOV L, C	Source address
	SPHL	To SP
	XCHG	Move Block move
		address to HL
Loop	POP B	fetch four bytes from
	POP D	source store 1st byte
	MOV M, C	at destination
	INX H	
	MOV M, B	2nd
	INX H	
	MOV M, E	3rd
	INX H	
	MOV M, D	4th
	INX H	
	DCR A	check for end of
	JNZ Loop	Block move
	LHLD SAVESP	return old
	SPHL	SP
	RET	return

Once the count less than match is found in the application the  
 HL register has 10 added to it which points it at the corre-  
 sponding temperature (lines 79-82). This temperature is then  
 displayed in the address field of the SDK 85 display using  
 user available monitor routines. If the temperature is out of  
 range the code detects it (lines 69-74) and outputs 1's on Port  
 A or Port B if the temperature was too low or too high respec-  
 tively (lines 101-105 "too low" and lines 108-112 "too high").

## APPLICATION EXAMPLE 2

### CRT INTERFACE

Most microprocessor systems require some sort of serial communications. This may be selected for reasons of economy (to reduce the number of interconnections required in a distributed system), or it may be necessary in order to communicate with such common peripherals as CRT's or teletypewriters.

These peripherals all use a standard convention for transmitting serial ASCII code. Each data byte is transmitted as a series of 10 or 11 bits. The uniform time per bit corresponds to the data transmission rate. For example, if the transmission rate is to be 2400 baud (2400 bits per second), each bit time must be  $1/2400 \text{ bps} = 416.7 \mu\text{sec/bit}$ . The standard 10-bit sequence consists of a logically zero "Start" bit, 8 data bits (least significant bit first), and one or more stop bits (logic 1). An 11-bit sequence with two stop bits is used for 110 baud TTY's. The logic one level continues until the start bit of the next byte to ensure that each 10-bit sequence is initiated with a one-to-zero transition. The 8 bits transferred might be raw binary data or alphanumeric characters using the standard ASCII code. In this case, the most significant bit -- the last data bit transmitted -- will depend on the parity convention being used. This sequence is illustrated for the ASCII "space" character in Figure 22.

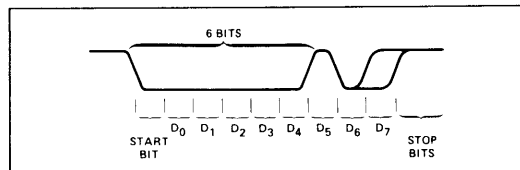


Figure 22. ASCII Space Character

The algorithm for receiving serial code involves sampling the incoming data at the middle of each bit time. The eight sampled values are shifted into a serial byte corresponding to the data originally transmitted. The one-to-zero transition at the beginning of each byte makes it possible to synchronize the sampling points relative to the start of each data sequence.

### Hardware Interface

In general, any serial communications system will require both hardware and software interfaces. Since the SOD line can drive only one TTL load, additional current and voltage buffering is required to be compatible with the RS-232C interface standard used by most peripherals. A schematic for achieving this buffering is shown in Figure 23. The MC1488 and MC1489 circuits interface positive logic TTL signals with the RS-232 high voltage inverted logic levels.

### Software Package

The software needed to drive the CRT interface is divided into three parts. All three use software timing and delay loops, with fixed and variable parameters. In conjunction, they are able to identify incoming signals at any rate from below 110 to over 9600 baud and respond at the same rate.

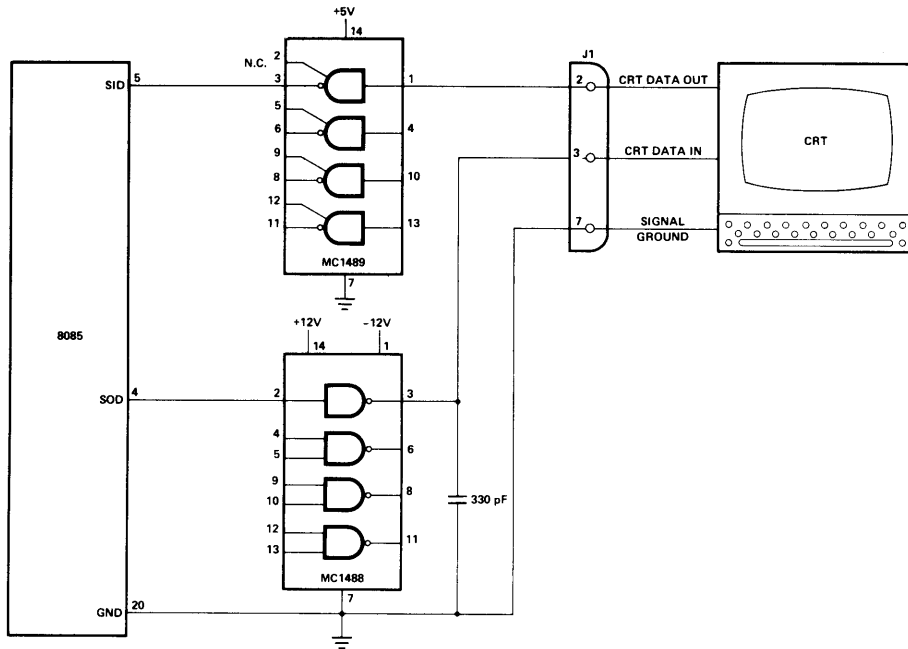


Figure 23. RS-232C Interface Schematic

Upon power-up or reset, or when the console device baud rate is changed, the baud rate identification subroutine (BRID) is called. This routine waits until an ASCII space character (20H) is received from the console. (Any other character will result in a case of mistaken identification.) When a space character is received, two time parameters are computed which correspond to the bit time and one-half the bit time of the baud rate being used. These are stored as variables BITTIME and HALFBIT. To output a character to the console, the character code is placed in register C, and the subroutine COUT is called. This routine uses BITTIME as a parameter for the software delay loop which determines the baud rate. To accept a character from the keyboard, CIN is called. CIN returns after the next key is typed, with the corresponding character code in register C. CIN uses both parameters BITTIME and HALFBIT.

Since COUT and CIN use time parameters computed by BRID, they will function at a rate the same as that of the initial space character input. Because of the nature of the software, the rate does not depend on the CPU clock frequency. This

results in additional flexibility in the following respects:

1. The software does not need to be modified if the 8085 crystal frequency is changed or Wait states are added.
2. Since the time base is no longer critical, the quartz crystal could be replaced by a less expensive RC network, provided the frequency does not drift by more than a few percent during a session. Additional drift can be accommodated by periodically recalling the BRID routine.
3. Communication is possible at non-standard baud rates which relaxes the constraints on system peripherals.

It should be noted, though, that slowing down the CPU clock will decrease its throughput proportionately. In addition, it will degrade the maximum resolution of the delay loops, with the result that the highest baud rates may no longer be achievable.

A more detailed analysis of the CRT interface routines will be presented in the order of increasing complexity: COUT, CIN, and BRID. Since SID and

SOD are ideal for many applications which involve critical I/O timing, the timing techniques used here may be of interest to software designers. Accordingly, the mathematical derivation of the timing parameters is included in this analysis, as well as a justification for the BRID algorithm. The algebra involved might be a bit too tedious for designers unconcerned with generating software delays. If so, they (and other bored readers) have the freedom of choice to skip over the sections they find objectionable.

### OUTPUT ROUTINE

It would seem natural to write data in the standard format in three stages: output a zero start bit, then the 8 data bits (using a loop sequence), then the stop bits. Each stage would incorporate its own appropriate delay and output sections, leading to unnecessary duplication. Instead, the code below executes the same main loop 11 times. Its bit manipulation routine inherently results in the correct data sequence being formed. It accomplishes this by using the carry and C register as a 9-bit pseudo-circular shift register. Initially CY=0. The algorithm outputs CY, waits one bit time, sets CY=1, and then rotates the pseudo-register right one bit. This repeats for 11 cycles. On the tenth and all subsequent loops, the output bit will be a logical one, since that bit had been set nine loops earlier while in the CY (see Figure 24).

When COUT is called the registers to be used must be preserved and interrupts disabled so the timing loop will not be disrupted. Clear the CY in preparation for outputting the start bit, and set the loop counter for 11 bits (if 110 baud will never be used, the counter could be set to 10):

```

COUT:  PUSH  B
        PUSH  H
        DI
        MRR  A
        MVI  B,11
    
```

Output of the contents of the CY:

```

001:  MVI  A,0AH    (7)
        RRR      (4)
        SIM      (4)
    
```

The numbers in brackets indicate how many machine cycles are required for each instruction. They will be referred to in the timing analysis section.

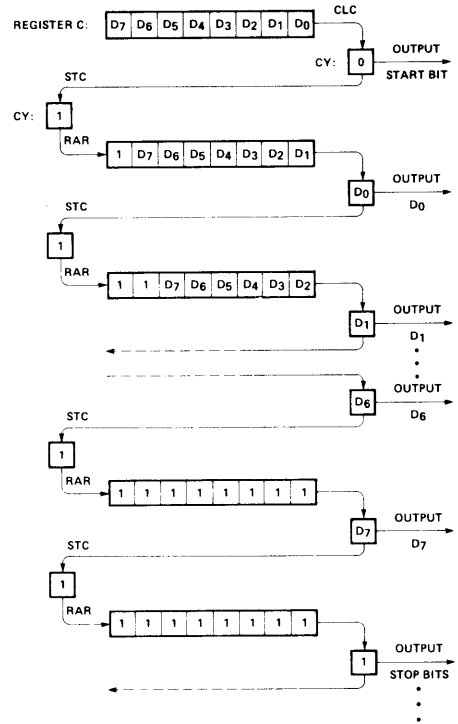


Figure 24. Data Serialization Algorithm

Get stuck in a loop for the appropriate time (don't worry for now how "BITTIME" is determined):

```

        LHL0  BITTIME    (16)
002:  DCR  L                (4)
        JNZ  002          (4)
        DCR  H                (4)
        JNZ  002          (4)
    
```

Rotate the contents of register C right into the CY, while moving a one into the left end. Continue until all bits have been transmitted:

```

        STC                (4)
        MOV  A,C            (4)
        RRR                (4)
        MOV  C,A            (4)
        DCR  B                (4)
        JNZ  001          (10)
    
```

Restore processor status and return:

```

POP    H
POP    R
EI
RET

```

### INPUT ROUTINE

The console input routine uses the opposite procedure; instead of moving a bit from register C to the CY, then to A7, then to SOD, CIN loads a bit from SID into A7, then moves it to CY, then into register C.

First, set up the CPU as before:

```

CIN    PUSH    H
        DI
        MVI    B, 8

```

When a start bit transition arrives, the first sampling should not be taken until the middle of the first data bit, one and one-half bit times after the transition. Await the start bit transition, then set up the delay parameter for one-half bit time:

```

C11:   RIM                (4)
        ORA    A          (4)
        JM     C11        (7)
        LHL   HALFBIT    (16)

```

Loop for one-half bit time before starting to sample data:

```

C12:   DCP    L          (0)
        JNZ   C12        (0)
        DCP    H          (0)
        JNZ   C12        (0)

```

Wait until the middle of the next bit before sampling SID, then move the data bit into CY:

```

C13:   LHL   BITTIME     (16)
C14:   DCP    L          (0)
        JNZ   C14        (0)
        DCP    H          (0)
        JNZ   C14        (0)
        RIM                (4)
        RAL                (4)

```

Decrement the bit counter. If this is the ninth cycle, the 8 data bits are in register C, so quit (the first stop bit will already have been received, and be in CY):

```

DCP    B          (4)
JZ     C15        (7)

```

Otherwise, continue. Rotate the data bit right into register C, and repeat the cycle:

```

MOV    A, C      (4)
RAR                (4)
MOV    C, A      (4)
NOP                (4)
JMP    C12       (18)

```

(A NOP is needed to make the COUT and CIN loops exactly equal in number of machine cycles, so that each can use the same delay parameter.) Restore status and return.

```

C15:   POP    H
        EI
        RET

```

### TIMING ANALYSIS

COUT and CIN now need to be provided with parameters for BITTIME and HALFBIT. It can be seen from the above code that each routine uses  $61 + D$  machine cycles per input or output bit, where  $D$  is the number of cycles spent in either four line delay segment. If  $\langle H \rangle$  and  $\langle L \rangle$  are the contents of the H and L registers going into this section of code, then:

$$D = 22 + (\langle L \rangle - 1) \times 14 + (\langle H \rangle - 1) \times [(255 \times 14) + 25] \quad (1)$$

$$\text{If } \langle H' \rangle \equiv \langle H \rangle - 1, \langle L' \rangle \equiv \langle L \rangle - 1, \text{ and } \langle HL' \rangle \equiv 256 \langle H' \rangle + \langle L' \rangle \quad (2)$$

$$\text{then } D = 22 + 14 \langle L' \rangle + 3595 \langle H' \rangle \quad (3)$$

This can be approximated by:

$$D = 22 + 14 \langle HL' \rangle \quad (4)$$

This approximation is exact for  $\langle H' \rangle = 0$ ; otherwise, it is accurate to within 0.3%. Thus each loop of COUT or CIN uses a total of:

$$C = 61 + D = 83 + 14 \langle HL' \rangle \text{ machine cycles} \quad (5)$$

Each machine cycle uses two crystal cycles in the 8085, so the resulting data rate is:

$$B = \frac{\text{cycle frequency}}{C} = \frac{(\text{crystal frequency}) \div 2}{83 + 14 \langle HL' \rangle} \quad (6)$$

For a typical calculation, see the example below.

**EXAMPLE**

To produce 2400 baud with the standard 6.144 MHz crystal:

$$2400 = \frac{(6.144 \times 10^6) \div 2}{83 + 14 \langle HL \rangle'}$$

$$14 \langle HL \rangle' = \left( \frac{6.144 \times 10^6 \div 2}{2400} \right) - 83$$

$$\langle HL \rangle' = \left[ \left( \frac{6.144 \times 10^6 \div 2}{2400} \right) - 83 \right] \div 14 = 85.5 \cong 86$$

$$\langle HL \rangle' = 8610 = 0056H$$

$$\langle HL \rangle = 0157H = \text{BITTIME}$$

To determine the true data rate this parameter will produce, substitute into equation (6):

$$\begin{aligned} \text{Date Rate} &= \frac{6.144 \times 10^6 \div 2}{83 + 14(86)} \\ &= 2387 \text{ baud, which is } 0.54\% \text{ slow.} \end{aligned}$$

For 9600 baud, the same calculations will yield  $\langle HL \rangle' = 17$ , which is actually 0.3% slow; a sizzling 19200 baud or 38400 baud could each be generated to within 5% if  $\langle HL \rangle' = 6$  or 0! Table 9 presents the parameters for several standard baud rates.

Notice that the resolution of the delay algorithm — the difference between bit times resulting from parameters which differ by one — is 14 machine cycles. As a result, the true bit delay produced can always manage to be within  $\pm 2.3 \mu\text{sec}$  of the delay

desired. This guarantees that at rates up to 9600 baud, where each bit time is at least 104  $\mu\text{sec}$  wide, some value of BITTIME can be found which will be accurate to within 2.2%.

**BAUD RATE IDENTIFICATION ROUTINE**

The function of BRID is to compute the appropriate parameters BITTIME and HALFBIT. It accomplishes this by observing the data pattern received when the space bar is pressed on the console device. Since a space character has the ASCII code 20H = 0010000B, the pattern represented back in Figure 4 is transmitted. Notice that the initial zero level is 6 bits wide. Suppose it could be determined that this corresponds to M machine cycles. Then one bit would correspond to  $(M \div 6)$  machine cycles. The reason for dividing down a space several bits long is so that any distortion caused by the signal rise and fall times, or any lack of precision in detecting the two transitions, will be reduced by a factor of six. Since the bit period of COUT and CIN is  $83 + 14 \langle HL \rangle'$ , BRID must generate a value  $\langle HL \rangle'$  such that:

$$M \div 6 = 83 + 14 \langle HL \rangle' \tag{7}$$

$$\langle HL \rangle' = \frac{(M \div 6) - 83}{14} \tag{8}$$

$$\langle HL \rangle' = \frac{M}{84} - 6 \text{ (approximately)} \tag{9}$$

This value can be determined by setting register pair HL to -6, then incrementing it once every 84 machine cycles during the period that the incom-

**Table 9**

**DELAY PARAMETERS FOR STANDARD BAND RATES USING 6.144 MHz CRYSTAL**

TARGET BAUD RATE	$\langle HL \rangle'_{10}$ (See Text)	$\langle HL \rangle'_{16}$ (See Text)	$\langle HL \rangle'$ or BITTIME (See Text)	HALFBIT	ACTUAL BAUD RATE PRODUCED	% ERROR
110	1989	07C5	08C6	04E3	109.99	-0.006
150	1457	05B1	06B2	03D9	149.99	-0.005
300	726	02D6	03D7	026C	299.80	-0.068
600	360	0168	0269	01A5	599.65	-0.059
1200	177	00B1	01B2	0159	1199.5	-0.039
2400	86	0056	0157	012C	2386.9	-0.547
4800	40	0028	0129	0115	4777.6	-0.469
9600	17	0011	0112	0109	9570.1	-0.312
19200	6	0006	0107	0104	18395.2	-4.37

ing signal is zero. BITTIME is then obtained by individually incrementing registers H and L. To obtain HALFBIT, divide the value of <HL>' determined above by two before incrementing each register.

In order to implement this algorithm, set HL to -6, verify that the incoming signal is a logic one, then wait for the start bit transition.

```
BR10: MVI  A,000H
      SIM
      LMI  H,-5H
BR11: RIM
      ORA  A
      JP   BR11
BR12: RIM
      ORA  A
      JM  BR12
```

Increment register pair HL, then delay so that each cycle will require 84 machine cycles:

```
BR13: INX  H           (6)
      MVI  E,04H      (7)
BR14: DCR  E           (52)
      JNZ  BR14       (10)
```

Check if SID is still low. If so, repeat:

```
RIM           (4)
ORA  A       (4)
JP   BR13    (10)
```

Otherwise continue. Store HL temporarily for the HALFBIT calculation. Obtain and store BITTIME:

```
PUSH  H
INR   H
INR   L
SHLD  BITTIME
```

Restore HL, calculate HALFBIT, and return:

```
POP   H
ORA  A
MOV  A,H
RAR
MOV  H,A
MOV  A,L
RAR
MOV  L,A
INR  H
INR  L
SHLD HALFBIT
RET
```

The assembled listings for these subroutines, along with a simple test program, is presented in the CRT and Cassette Code.

## APPLICATION EXAMPLE 3

### CASSETTE RECORDER INTERFACE

There are many situations where data has to be transmitted through a non-ideal medium. To give three typical examples, a system with electrically isolated elements might require that signals be AC coupled, communications through an audio network (such as telephone or radio) are greatly bandwidth limited, and some applications (such as a distributed network in an industrial environment) must tolerate random electrical noise. Attempting to record data on a cheap cassette recorder (the one used for this note cost \$17.00) will reveal all of these shortcomings, plus one: The tape speed fluctuates significantly and varies as the batteries run down, hence the data rate is inconsistent.

The recording scheme used here makes very few demands on the transmission medium. It makes no attempt to transmit DC voltage levels. Instead, data is transmitted by a series of variable length tone bursts. The dominant frequency of the tone used can be selected to be within the passband of the particular medium. Data is transmitted with each bit composed of a tone burst followed by a pause. The first third of a bit period is always a tone burst, the middle third is either a tone burst continuous with the first or a pause corresponding to, respectively, a one or zero, and the final third is always a pause, as shown in Figure 25. Thus, data is distinguished by the burst/pause ratio.

#### Hardware Design

These tone bursts are obtained from the 8085 SOD line, using analog signal conditioning to eliminate the DC component of the waveform. (This low frequency component is due to the single-ended nature of the SOD line: its deviations from ground are all positive, which unbalances the capacitive input stage of the recorder.) A suggested interface

circuit is shown in Figure 26, using one LM324 quad op amp and a few standard value discrete components which should be available in even a digital design laboratory. On playback, analog circuitry is again used to detect the presence of a tone burst. In Figure 26, A2 buffers the incoming signal, and A3 inverts it. The peaks of these two signals are transmitted through D1 or D2 and are filtered by an RC network. Comparator A4 then squares up the output and produces the logic signal read by the SID pin. Since the op amps are powered by the single 5-volt supply, a 2.0-volt reference level is obtained from a resistive voltage divider. The waveforms present at several points in the circuit are shown in Figure 27.

#### Software

The algorithm for reading a data bit off the tape is simple and straightforward: If the tone burst is longer than the pause, the bit is a one. Otherwise, it is a zero. Since only the time ratio is considered, any variation in tape speed will not affect the data determination.

#### VOLUME CONTROL

A question that arises with any audio cassette interface is how to set the volume control. (Recording level is usually determined internally.) When the playback level is correct, the logic signal output from A4 will have either a one-third or two-thirds duty cycle. This can be readily observed with an oscilloscope. In the field, an old-fashioned mechanical-type voltmeter could be connected to the A4 output, and the volume adjusted until the meter needle hovered somewhere between 1/3 and 2/3 the high level output voltage. With random data, the reading would be about 2 volts. There will be a fairly wide range of acceptable volume settings. (Since the quivering meter needle is being used here for inertial signal averaging, a digital voltmeter would not be very helpful in this application.)

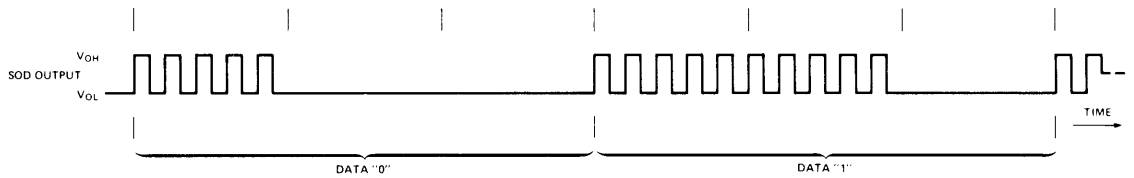


Figure 25. Tape Interface Data Recording Scheme

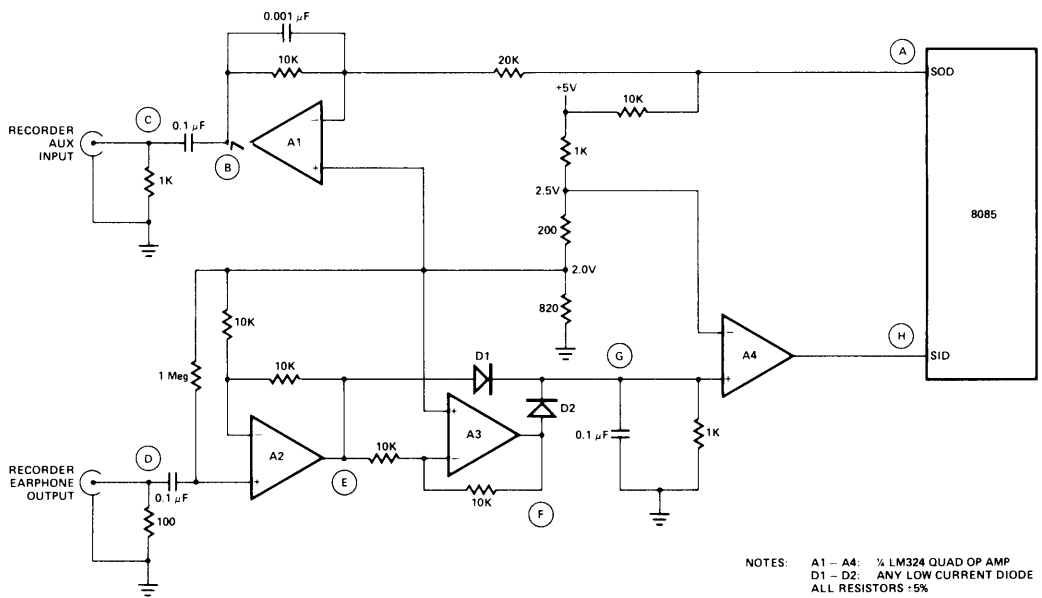
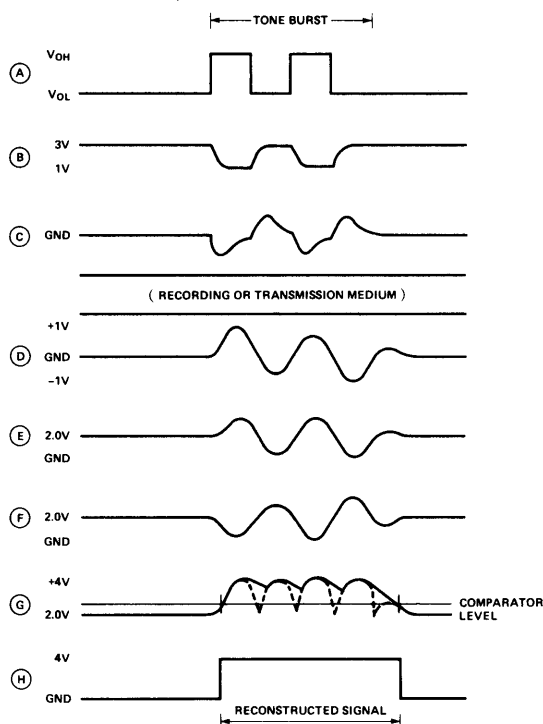


Figure 26. One Chip Magnetic Tape Interface Schematic



**Figure 27. Analog Signal Waveforms**

After the CRT software analysis, the tape routines are almost trivial. TAPEO is a subroutine for outputting the contents of register C to a cassette recorder. TAPEIN reads 8 bits into register C.

### OUTPUT ROUTINE

TAPEO calls a subroutine named BURST three times for each bit. If A<sub>6</sub> (the SOD enable bit) is set when BURST is called, a square-wave tone burst will be transmitted. If A<sub>6</sub> is not set, BURST simply delays for exactly the same amount of time before returning. The three calls are used to, respectively, output the initial burst, output the data burst/space, and create the space at the end of each bit. Nine bits will be output: the eight data bits (LSB first) followed by a zero bit. The start of the initial burst of the trailing zero is needed to mark the end of the final space of the preceding data bit.

Start each bit by outputting a tone burst:

```

TAPEO: MVI   B,9
        MVI   A,000H
        CALL  BURST

```

Rotate register C through CY:

```

MOV   A,C
RAR
MOV   C,A

```

Move CY to the SOD enable bit position, A<sub>6</sub>. Simultaneously set A<sub>7</sub> to one, and clear all other bits. Output a tone burst or space, depending on the previous contents of CY:

```

MVI   A,01H
RAR
RAR
CALL  BURST

```

Clear the accumulator, and output a space:

```

XRA   A
CALL  BURST

```

Keep cycling until the full 9-bit sequence is finished:

```

DCR   B
JNZ   T01
RET

```

The BURST subroutine executes the SIM instruction CYCNO times, at intervals of 29 + 14 <HALFCYC> machine cycles. In between each SIM, bit A<sub>7</sub> is complemented. CYCNO should be an even number. If A<sub>6</sub> is set upon calling BURST a square-wave will be created. Otherwise, the same code sequence is followed but SOD does not change – thus a space results.

```

BURST: MVI   D,CYCNO    <7>
        SIM
        MVI   E,HALFCYC <7>
        DCR   E         <4>
        JNZ   BU2       <7/10>
        XRI   00H       <7>
        DCR   D         <4>
        JNZ   BU1       <7/10>
        RET              <10>

```

### INPUT ROUTINE

TAPEIN uses a subroutine called BITIN to move the data at the SID pin into the CY. The maximum rate at which SID is read is limited by a delay loop in BITIN.

Initialize the bit counter and the register D, which will keep track of the tone burst time. If a tone

burst is being received when TAPEIN is called, wait until the burst is over:

```

TAPEIN: MVI   B, 8
        MVI   D, 00H
T11:    CALL  BITIN
        JC    T11
        CALL  BITIN
        JC    T11
    
```

(Throughout this subroutine, a level transition is recognized only after it has been read once initially and then verified on the next reading. This provides some degree of software noise immunity.) Now await the start of the next burst:

```

T12:    CALL  BITIN
        JNC  T12
        CALL  BITIN
        JNC  T12
    
```

The next burst has now arrived. Keep reading the SID pin, decrementing register D (thus making it more negative), each cycle until the pause is detected:

```

T13:    DCR   D
        CALL  BITIN
        JC   T12
        CALL  BITIN
        JC   T12
    
```

Now continue reading the SID pin, incrementing the D register (back towards zero), each cycle until the next burst is received:

```

T14:    INR   D
        CALL  BITIN
        JNC  T14
        CALL  BITIN
        JNC  T14
    
```

Now, if the burst lasted longer than the space, D was not incremented all the way back to zero; it is still negative. If the space was longer, D was incremented up through zero; it is now positive. In other words, the sign bit of D will now correspond to the data bit that would lead to each of these results. Move the sign bit into the CY, then rotate it into register C:

```

MOV    A, D
RAL
MOV    A, C
RAR
MOV    C, A
MVI   D, 00H
    
```

Continue until the last bit has been received:

```

DCR   B
JNZ   T13
RET
    
```

(Notice that the first half of this subroutine is incorporated in the second half. In fact, the assembled listing included in the Appendix makes use of this fact to eliminate 24 bytes of duplicated code.)

BITIN waits a short time in order to regulate the sampling rate, then reads SID and moves the data bit into the CY:

```

BITIN: MVI   E, CKRATE <?>
B11:   DCR   E <4>
        JNZ  B11 <7/10>
        PIM <4>
        RAL <4>
        RET <10>
    
```

The tone burst frequency and duration, and the TAPEIN sampling rate are determined by HALF CYC, CYCNO, and CKRATE. Tables 10 and 11 give typical values.

Table 10  
EXAMPLE COMBINATIONS OF HALF CYC AND CYCNO.  
ALL VALUES IN DECIMAL

APPROXIMATE TONE FREQUENCY	CORRESPONDING HALF CYC VALUE	RESULTING DATA RATE			
		8	20	100	CYCNO CYC/BURST
500 Hz	217	42	17	3.3	bps
1 kHz	108	83	33	6.6	bps
2 kHz	53	166	66	13	bps
5 kHz	20	414	166	33	bps
10 kHz	9	826	330	66	bps

Table 11  
MAXIMUM SAMPLING RATES  
FOR VARIOUS VALUES OF  
CKRATE

CKRATE VALUE	SAMPLING RATE (INCLUDING CALL & RET)
1	17.6 $\mu$ sec
20	104 $\mu$ sec
80	378 $\mu$ sec
250	1.14 msec

The CRT and Cassette Code also includes a simple block record routine utilizing TAPEO. Before calling BLKRCD, HL must be set to the start of the desired block, and the recorder turned on manually. Successive bytes will be recorded until the end of that page, i.e., until L is incremented to zero. The playback routine requires presetting HL to the target address and turning on the recorder before PLAYBK is called. These routines incorporate a long tone burst before each data block to allow a recorder with Automatic Gain Control to stabilize before the data starts.

### ADDITIONAL COMMENTS

The two design examples given so far were built up using an SDK-85 System Design Kit. Both hardware interfaces were wire-wrapped on the ample breadboarding area provided on the board. The connections between SID and SOD and the on-board TTY interface were broken, so as not to affect the 8085 I/O electrical characteristics.

The CRT interface was tested with a Beehive Mini-Bee II Terminal in the full duplex mode at each of its 14 possible transmission rates, from 110 to 9600 baud. It was also checked out at 19200 baud using a Beehive B-100 terminal. In addition, the software was exercised using an SBC 80/20 system as a variable baud rate character generator and receiver.

An additional advantage to having software selectable communications rates is that it would be possible to communicate with several system peripherals, each at its own preferred rate, without having to duplicate hardware. For example, the addition of a single 7408 AND gate and an output port (such as on the 8155) would make it possible to use the same two RS-232 circuits to interface with up to seven I/O devices (see Figure 28). Three of the MC1488 drivers have Enable inputs which can be controlled by the output port. One AND gate can be used to buffer the SOD line and drive the MC1488 Data inputs. The rest of the 7408 can be configured as a four input AND gate. This would act as an inverted logic OR gate to reduce the four MC1489 receiver outputs to a single line, which could be read by the SID. This assumes that only one input device (CRT, PTR) at a time will be used (which is usually the case in a non-time shared, interactive application), and that the unused devices are transmitting a logic one level (which should also be the case).

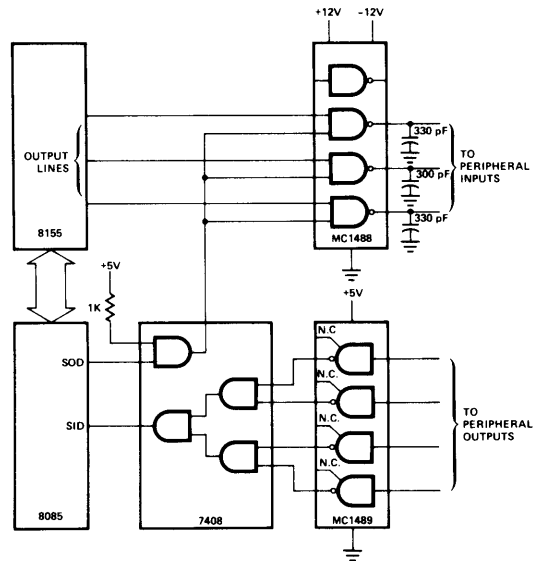


Figure 28. Interfacing 8085 to Multiple Peripherals

The software needed to support additional peripherals would be simple and straightforward. A routine intended to dump a section of memory to a paper tape punch, for example, would first have to store BITTIME and HALFBIT somewhere (perhaps on stack), load the variables with new parameters corresponding to the paper tape punch rate, and then write a bit pattern to the output port which would disable the console driver and enable the punch (and perhaps a typewriter). After the dump was over, the original time parameters and driver status would be restored.

As explained before, the BRID routine computed rate parameters based on the fact that an ASCII "space" character resulted in a zero level 6 bits long. Conceivably, some obscure peripherals might produce a transient between successive zero bits. (This might be the case, for example, if the signal was produced by mechanical rather than electronic means.) If so, the BRID algorithm used here probably would not work reliably. Once the two time parameters were identified, though, COUT and CIN could still be used. An alternate algorithm for baud rate identification would require a table in ROM (note the fifth and final R/S-I/O-M/D permutation). This table would contain a list of delay parameters corresponding to the standard transmis-

---

sion rates, as computed for the selected crystal frequency. Initialization would require the operator to hit a specific key several times (usually the "U" key, which generates a pattern of alternating ones and zeros). The identification routine would attempt to "read" this pattern at each baud rate, in turn, until finding the rate at which the read was successful.

The cassette recorder used to develop the tape interface was a Lloyd's push-button model which cost \$17 in 1972. Empirical testing has indicated that for this application, the quality of the cassette recorder is less critical than the quality of the tape itself. In other words, some 33¢ cassettes were not very reliable, even when used with more expensive recorders.

When using a cassette at the beginning of a side, allow the tape to run for about 10 seconds until the leader has passed before starting to write data. Otherwise, data will be lost to the leader.

Depending on the recorder quality, the tone burst frequency and duration can be optimized for higher data rates by modifying HALFCYC and CYCNO. If so, CKRATE should also be reduced, so that between about 10 and 80 data samplings are made during a single (one-third width) tone burst. At greatly increased frequencies, some of the

components in the analog interface might also be modified.

The two simple routines for recording and playing back blocks of data were intended to illustrate one way of using TAPEIN and TAPEO, and therefore do not contain any provisions for error detection or correction. Depending on the nature of a particular application, these routines could be augmented with parity bit or checksum comparison, or an error correcting code technique.

Funny things happen when recording and playing back a page of RAM which includes the subroutine stack. Eventually, PLAYBK will start writing over the data at the top of the stack, destroying the subroutine traceback sequence. The next RET instruction will then cause a jump to a place where you'd rather not be.

The printout reproduced in the CRT Code includes the assembled listings for the CRT and magnetic tape interfaces discussed in this application note. The object code produced was programmed into an 8755 EPROM, which was installed in the expansion PROM socket of the SDK-85 board. Some very minor differences exist between this listing and the code segments presented earlier, which were written for maximum clarity.

# Temperature Sensor Code

ASM88 F1 TEST SRC MOD85

IS15-I1 8888/8885 MACRO ASSEMBLER, V2 0      MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1 ;	
		2 ;	
026C		3 HXDSP EQU 026CH	;EXPAND HEX TO DISPLAY, SDK MONITOR ROUTINE
02B7		4 OUTPUT EQU 02B7H	;OUTPUT TO DISPLAY, SDK MONITOR ROUTINE
05F1		5 DELAY EQU 05F1H	;DELAY DISPLAY, SDK MONITOR ROUTINE
		6 ;	
2000		7 ORG 2000H	
		8 ;	
		9 ;	
		10 ;	
		11 ;	
2000 31C820		12 LXI SP,20C8H	;INITIALIZE STACKPOINTER
2003 F3		13 DI	;DISABLE INTERRUPTS
		14 ;	
		15 ;	INITIALIZE COUNTER IN 8155 FOR COUNTDOWN MODE. LOAD COUNTER
		16 ;	WITH HIGHEST VALUE (3FFF).
		17 ;	
2004 3EBF		18 MVI A,0BFH	
2006 D325		19 OUT 25H	;ADDRESS FOR TOP HALF OF COUNTER
2008 3EFF		20 MVI A,0FFH	
200A D324		21 OUT 24H	; " " LOWER HALF OF COUNTER
200C 3EC0		22 MVI A,0C0H	
200E D320		23 OUT 20H	;COUNT DOWN MODE START
		24 ;	
		25 ;	PULSE THE ONE SHOT WITH A POSITIVE GOING PULSE ON THE S00
		26 ;	OUTPUT PIN OF THE 8885
		27 ;	
2010 3EC8		28 MVI A,0C8H	
2012 30		29 SIM	;OUTPUT A HIGH ON S00 LINE
2013 3E48		30 MVI A,48H	
2015 30		31 SIM	;OUTPUT A LOW ON S00 LINE
2016 FB		32 EI	;ENABLE INTERRUPTS(AFTER PULSE)
		33 ;	
		34 ;	IDLE UNTIL ONESHOT INTERRUPTS THE RST 6 5 PIN ON THE 8885
		35 ;	
2017 00		36 NPO	
2018 C31720		37 JMP NPO	;IDLE UNTIL INTERRUPT
		38 ;	
		39 ;	AFTER INTERRUPT, STOP COUNTER AND READ IN FINAL COUNT FROM
		40 ;	8155. STORE IN REGISTER PAIR BC.
		41 ;	
201B 3E40		42 CNTU MVI A,40H	
201D D320		43 OUT 20H	;STOP COUNTER
201F DB24		44 IN 24H	
2021 4F		45 MOV C,A	;STORE LOWER ORDER BYTE IN C
2022 DB25		46 IN 25H	
2024 47		47 MOV B,A	;STORE HIGHER ORDER BYTE IN B
2025 263F		48 MVI H,3FH	;LOAD HL WITH FULL START COUNT
2027 2EFF		49 MVI L,0FFH	
		50 ;	
		51 ;	ADJUST THE COUNT VALUE IN REGISTER BC TO REPRESENT ACTUAL
		52 ;	COUNT (SEE TEXT FOR EXPLANATION)

## Temperature Sensor Code (Cont'd)

1515-11 8888/8885 MACRO ASSEMBLER, V2.0

MODULE PAGE 2

LOC	OBJ	SEQ	SOURCE STATEMENT
		53 ;	
2029	CD6820	54	CALL ADJUST ; CONVERTS 8155 COUNT TO ACTUAL COUNT
		55 ;	
		56 ;	SETUP INITIALIZATION FOR SEARCH ROUTINE. ROUTINE LOOKS FOR TEMPERATURE
		57 ;	RANGE OF COUNT (SEE TEXT). SEARCH ONLY FOR UPPER HALF TO SIMPLIFY CODE.
		58 ;	
202C	2E80	59	MVI L, 00H ; SET HL TO BEGINNING OF SEARCH
202E	2620	60	MVI H, 20H ; STRING IN MEMORY.
2030	B0	61	ORA B ; CLEAR CARRY FOR ROUTINE
2031	78	62	MOV A, B ; PLACE B INTO ACCUMULATOR
2032	0E01	63	MVI C, 1H ; SET TIMES THROUGH SEARCH
2034	CD9220	64	CALL SEARCH ; LOOKS FOR TEMP RANGE COUNT IS IN
		65 ;	
		66 ;	CHECK IF SEARCH WAS SUCCESSFUL. IF NOT THEN OUTSIDE ACCEPTABLE
		67 ;	RANGE.
		68 ;	
2037	3E80	69	MVI A, 00H ; DID L FIND LESS THAN AT
2039	AD	70	XRA L ; AT BEGINNING OF STRING?
203A	CAFF20	71	JZ TLOW ; TEMP BELOW ALLOWED LIMITS. SET PORT A
203D	3E00	72	MVI A, 00H ; DID C GET DECREMENTED?
203F	B9	73	CMF C ; IF SO, SEARCH DID NOT FIND
2040	CAB820	74	JZ THIGH ; TEMP ABOVE LIMITS, SET PORT B
		75 ;	
		76 ;	SOFTWARE MAP THE MATCH TO A TEMPERATURE IN DEGREES C BY ADDING
		77 ;	10 TO SEARCH ADDRESS. PLACE TEMPERATURE IN REGISTER E.
		78 ;	
2043	3E0A	79	MVI A, 00H ; SHIFT HL BY 10 (SOFTWARE MAP)
2045	85	80	ADD L
2046	6F	81	MOV L, A
2047	5E	82	MOV E, M ; READ IN TEMPERATURE
		83 ;	
		84 ;	SET UP INITIALIZATION FOR DISPLAYING TEMPERATURE USING SDK
		85 ;	MONITOR ROUTINES. FIRST EXPAND DE REGISTER AND THEN DISPLAY
		86 ;	FOR DELAY PERIOD.
		87 ;	
2048	0600	88	MVI B, 00H ; CLEAR DOT AT ADDRESS FIELD
204A	CD6C02	89	CALL HDSP ; CALL EXPAND
204D	3E00	90	MVI A, 00H
204F	CD8702	91	CALL OUTPUT ; OUTPUT TO SDK DISPLAY
2052	11FF00	92	LXI D, 0FFH ; SET DELAY PERIOD
2055	CDF105	93	CALL DELAY ; DISPLAY FOR DELAY PERIOD
2058	CF	94	RST 1 ; SOFTWARE RESTART
		95 ;	
		96 ;	SUBROUTINES
		97 ;	
20AF		98 ORG 20AFH	
		99 ;	
		100 ;	
20AF	3E03	101 TLOW	MVI A, 03H
20B1	D320	102	OUT 20H
20B3	3EFF	103	MVI A, 0FFH ; SET PORT A AS 1'S
20B5	D321	104	OUT 21H
20B7	CF	105	RST 1
		106 ;	
		107 ;	

## Temperature Sensor Code (Cont'd)

1515-11 8888/8885 MACRO ASSEMBLER, V2.0      MODULE    PAGE    3

LOC	OBJ	SEQ	SOURCE	STATEMENT
2088	3E03	108	THIGH	MVI    A,03H
208A	D320	109		OUT    20H
208C	3EFF	110		MVI    A,0FFH      ;SET PORT B AS I'S
208E	D322	111		OUT    22H
20C0	CF	112		RST    1
		113		;
		114		;
2092		115	ORG	2092H
		116		;
		117		;
2092	BE	118	SEARCH	CMP    M
2093	D8	119		RC
2094	23	120		INX    H      ;ELSE INCREMENT POINTER
2095	BE	121		CMP    M      ;COMPARE 2ND BYTE
2096	D8	122		RC
2097	23	123		INX    H
2098	BE	124		CMP    M      ;COMPARE 3RD BYTE
2099	D8	125		RC
209A	23	126		INX    H
209B	BE	127		CMP    M      ;COMPARE 4TH BYTE
209C	D8	128		RC
209D	23	129		INX    H
209E	BE	130		CMP    M      ;COMPARE 5TH BYTE
209F	D8	131		RC
20A0	23	132		INX    H
20A1	BE	133		CMP    M      ;COMPARE 6TH BYTE
20A2	D8	134		RC
20A3	23	135		INX    H
20A4	BE	136		CMP    M      ;COMPARE 7TH BYTE
20A5	D8	137		RC
20A6	23	138		INX    H
20A7	BE	139		CMP    M      ;COMPARE 8TH BYTE
20A8	D8	140		RC
20A9	23	141		INX    H
20AA	00	142		DCR    C      ;HAS ENTIRE BLOCK BEEN
20AB	C29220	143		JNZ    SEARCH    ;SEARCHED? IF SO SET NO
20AE	C9	144		RET              ;LESS THAN AND RETURN
		145		;
		146		RESTART 6 5 JUMP ADDRESS
		147		;
20CE		148	ORG	20CEH
		149		;
		150		;
20CE	C31B20	151		JMP    CNTU
		152		;
		153		;
		154		;
		155		;
		156		;
		157		;
		158		SEARCH COMPARE DATA STRING (SEE TEXT)
		159		;
		160		;
20E0		161	ORG	20E0H
		162		;

# Temperature Sensor Code (Cont'd)

IS15-11 8088/8085 MACRO ASSEMBLER, V2.0      MODULE    PAGE    4

```

LOC  OBJ      SEQ      SOURCE STATEMENT

163 ;
2000 35      164      DB      35H,36H,37H,38H,39H,3AH,3BH,3CH
2001 36
2002 37
2003 38
2004 39
2005 3A
2006 3B
2007 3C

165 ;
166 ;    SOFTWARE MAP TO TEMPERATURE
167 ;
2008      168  ORG      2000H
169 ;
170 ;
2008 21      171      DB      21H,23H,25H,26H,31H,35H,39H
200C 23
200D 25
200E 28
200F 31
2090 35
2091 39

172 ;
173 ;
2060      174  ORG      2060H
175 ;
176 ;
177 ;    SUBROUTINE ADJUST FOR COUNT IN 8155
178 ;
2060 78      179  ADJUST  MOV    A,B            ;LOAD ACCUMULATOR WITH UPPER HALF
2061 E63F    180    ANI    3FH           ;RESET UPPER TWO BITS,CLEAR CARRY
2063 1F      181    RAR           ;ROTATE RIGHT THROUGH CARRY
2064 47      182    MOV    B,A           ;STORE SHIFTED VALUE BACK IN B
2065 79      183    MOV    A,C           ;LOAD ACCUMULATOR WITH LOWER HALF
2066 1F      184    RAR           ;ROTATE WITH CARRY RIGHT
2067 4F      185    MOV    C,A           ;STORE SHIFTED VALUE IN C
2068 D8      186    RNC           ;1ST HALF OR SECOND? IF SECOND RETURN
2069 3F      187    CMC           ;CLEAR CARRY
206A 7C      188    MOV    A,H           ;OBTAIN ONE HALF OF FULL COUNT
206B 1F      189    RAR           ;IF HL IS ODD THIS CONTAINS
206C 67      190    MOV    H,A           ;ONE HALF(FULL COUNT-1), WHICH
206D 7D      191    MOV    A,L           ;IS CORRECT
206E 1F      192    RAR          
206F 6F      193    MOV    L,A          
2070 09      194    DAD    B           ;DOUBLE PRECISION ADD
2071 44      195    MOV    B,H           ;RESTORE BC REGISTERS WITH COUNT
2072 4D      196    MOV    C,L          
2073 C9      197    RET
198 ;
199 ;
200            200            END

```

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS

IS15-11 8088/8085 MACRO ASSEMBLER, V2.0      MODULE    PAGE    5

ADJUST A 2060    CNTU    A 201B    DELAY    A 05F1    HXD/SP    A 026C    NFO    A 2017    OUTPUT    A 0267    SEARCH    A 2092  
 THIGH    A 2068    TLOW    A 206F

ASSEMBLY COMPLETE. NO ERRORS

---

## CRT and Cassette Code

ISIS-II 8080/8085 ASSEMBLER, V1.0

MODULE

PAGE 1

LOC DBT

SEQ

SOURCE STATEMENT

0 \$ MOD85 TITLE('8085 SERIAL I/O NOTE APPENDIX')

## CRT and Cassette Code (Cont'd)

IS15-II 8080/8085 ASSEMBLER: V1 0                      MODULE                      PAGE    2  
8085 SERIAL I/O NOTE APPENDIX

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	
		2	THE FOLLOWING PROGRAMS AND SUBROUTINES ARE DESCRIBED IN DETAIL
		3	IN INTEL CORPORATION'S APPLICATION NOTE AP-29, "USING THE 8085
		4	SERIAL I/O LINES". THE FIRST SECTION IS A GENERAL PURPOSE CRT
		5	INTERFACE WITH AUTOMATIC BAUD RATE IDENTIFICATION; THE SECOND
		6	SECTION IS A MAGNETIC TAPE INTERFACE FOR STORING DATA ON CASSETTE
		7	TAPE. THE CODE PRESENTED HERE IS ORIGINATED AT LOCATION 800H,
		8	AND MIGHT BE PART OF AN EXPANSION PROM IN AN INTEL 80K-85
		9	SYSTEM DESIGN KIT.
		10	
		11	
		12	
20C8		13	BITTIME EQU 20C8H ;ADDRESS OF STORAGE FOR COMPUTED BIT DELAY
20CA		14	HALFBIT EQU 20CAH ;ADDRESS OF STORAGE FOR HALF BIT DELAY
800B		15	BITSO EQU 11 ;DATA BITS PUT OUT (INCLUDING TWO STOP BITS)
8009		16	BITSI EQU 9 ;DATA BITS TO BE RECEIVED (INCLUDING ONE STOP BIT)
		17	
8800		18	ORG 880H ;STARTING ADDRESS OF 80K-85 EXPANSION PROM
		19	
		20	:CRTTST CRT INTERFACE TEST. WHEN CALLED, AWAITS THE SPACE BAR BEING PRESSED ON
		21	THE SYSTEM CONSOLE, AND THEN RESPONDS WITH A DATA RATE VERIFICATION
		22	MESSAGE. THEREAFTER, CHARACTERS TYPED ON THE KEYBOARD ARE ECHOED
		23	ON THE DISPLAY TUBE. WHEN A BREAK KEY IS TYPED, THE ROUTINE IS
		24	RE-STARTED, ALLOWING A DIFFERENT BAUD RATE TO BE SELECTED ON THE CRT.
8800	31C820	25	CRTTST LMI 31C820H
8803	3EC0	26	CRTI1 MVI A,0C0H ;S0D MUST BE HIGH BETWEEN CHARACTERS
8805	38	27	SIM
8806	0D1A08	28	CALL BRID ;IDENTIFY DATA RATE USED BY TERMINAL
8809	0D4708	29	CALL SIGNON ;OUTPUT SIGNON MESSAGE AT RATE DETECTED
880C	0D8A08	30	ECHO1 CALL CIN ;READ NEXT KEYSTROKE INTO REGISTER C
880F	79	31	MOV A,C
8810	B7	32	ORA A ;CHECK IF CHARACTER WAS A (BREAK) (ASCII 00H)
8811	0A0308	33	JZ CRTI1 ;IF S0, RE-IDENTIFY DATA RATE
		34	;THIS ALLOWS ANOTHER RATE TO BE SELECTED ON CRT
8814	0D6908	35	CALL COUT ;OTHERWISE COPY REGISTER C TO THE SCREEN
8817	030C08	36	JMP ECHO ;CONTINUE INDEFINITELY (UNTIL BREAK)
		37	
		38	:BRID BAUD RATE IDENTIFICATION SUBROUTINE
		39	EXPECTS A (CR) (ASCII 0DH) TO BE RECEIVED FROM THE CONSOLE.
		40	THE LENGTH OF THE INITIAL ZERO LEVEL (SIX BITS WIDE) IS MEASURED
		41	IN ORDER TO DETERMINE THE DATA RATE FOR FUTURE COMMUNICATIONS.
881A	28	42	BRID1 PIM ;VERIFY THAT THE "ONE" LEVEL HAS BEEN ESTABLISHED
881B	B7	43	ORA A ;AS THE CRT IS POWERING UP
881C	F21A08	44	JP BRID
881F	28	45	BR11 RIM ;MONITOR SID LINE STATUS
8820	B7	46	ORA A
8821	F81F08	47	JM BR11 ;LOOP UNTIL START BIT IS RECEIVED
8824	21FAFF	48	LXI H,-6 ;BIAS COUNTER USED IN DETERMINING ZERO DURATION
8827	1E84	49	BR13 MVI E,04H
8829	10	50	BR14 DCP E ;53 MACHINE CYCLE DELAY LOOP
882A	022908	51	INZ BR14
882D	23	52	INX H ;INCREMENT COUNTER EVERY 84 CYCLES WHILE SID IS LOW
882E	28	53	RIM

## CRT and Cassette Code (Cont'd)

1515-II 8080/8085 ASSEMBLER V1.0      MODULE      PAGE    3  
 8085 SERIAL I/O NOTE APPENDIX

LOC	OBJ	SEQ	SOURCE STATEMENT
082F	B7	54	ORA    A
0830	F22708	55	JP     BR13
		56	;CHLD NOW CORRESPONDS TO INCOMING DATA RATE
0832	E5	57	PUSH   H     ;SAVE COUNT FOR HALFBIT TIME COMPUTATION
0834	24	58	INR    H     ;BITTIME IS DETERMINED BY INCREMENTING
0835	20	59	INR    L     ;  H AND L INDIVIDUALLY
0836	220820	60	SHLD   BITTIME
0839	E1	61	POP    H     ;RESTORE COUNT FOR HALFBIT DETERMINATION
083A	87	62	ORA    A     ;CLEAR CARRY
083B	70	63	MOV    R,H   ;ROTATE RIGHT EXTENDED (CHLD)
083C	1F	64	RAR           ;  TO DIVIDE COUNT BY 2
083D	67	65	MOV    H,A
083E	70	66	MOV    A,L
083F	1F	67	RAR           ;
0840	6F	68	MOV    L,A
0841	24	69	INP    H     ;PUT H AND L IN PROPER FORMAT FOR DELAY
0842	20	70	INP    L     ;  SEGMENTS (INCREMENT EACH)
0843	220A20	71	SHLD   HALFBIT ;SAVE AS HALF-BIT TIME DELAY PARAMETER
0846	09	72	PET           ;
		73	
		74	;SIGNON WRITES A SIGN-ON MESSAGE TO THE CRT AT WHAT SHOULD BE THE CORRECT RATE.
		75	;  IF THE MESSAGE IS UNINTELLIGIBLE, WELL, SO IT GOES.
0847	215508	76	SIGNON: LMI    H,STRING ;LOAD START OF SIGN-ON MESSAGE
084A	4E	77	SI     C,M     ;GET NEXT CHARACTER
084B	AF	78	XRA    A     ;CLEAR ACCUMULATOR
084C	B1	79	ORA    C     ;CHECK IF CHARACTER IS END OF STRING
084D	02	80	RZ           ;RETURN IF SIGN-ON COMPLETE
084E	006908	81	CALL   COUT   ;ELSE OUTPUT CHARACTER TO CRT
0851	23	82	INR    H     ;INDEXY POINTER
0852	024A08	83	JMP   S1     ;ECHO NEXT CHARACTER
		84	
0855	00	85	STRNG DB     '00H,00H' ;(CR)<LF>
0856	0A		
0857	42415544	86	DB     'BRAUD RATE CHECK'
0858	20524154		
085F	45204348		
0862	454348		
0865	00	87	DB     '00H,00H' ;(CR)<LF>
0867	0A		
0868	00	88	DB     '00H'    ;END-OF-STRING ESCAPE CODE
		89	
0869	F3	90	;COUT    CONSOLE OUTPUT SUBROUTINE
		91	;  WRITES THE CONTENTS OF THE C REGISTER TO THE CRT DISPLAY SCREEN
086A	C5	92	COUT DB     ;
086B	E5	93	PUSH   B     ;
086C	0608	94	PUSH   H     ;
086E	AF	95	MVI    B,BIT50 ;SET NUMBER OF BITS TO BE TRANSMITTED
086F	DE80	96	XRA    A     ;CLEAR CARRY
0871	1F	97	MVI    A,80H ;SET WHAT WILL BECOME S00 ENABLE BIT
0872	30	98	RAR           ;MOVE CARRY INTO S00 DATA BIT OF ACC
0873	2A0820	99	STB           ;OUTPUT DATA BIT TO S00
0876	20	100	SHLD   BITTIME ;WAIT UNTIL APPROPRIATE TIME HAS PASSED

## CRT and Cassette Code (Cont'd)

ISIS-II 8080/8085 ASSEMBLER, V1.0  
8085 SERIAL I/O NOTE APPENDIX

MODULE

PAGE 4

LOC	OBJ	SEQ	SOURCE STATEMENT
0877	C27608	102	JNZ C02
087A	25	103	DCP H
087B	C27608	104	JNZ C02
087E	37	105	STC ;SET WHAT WILL EVENTUALLY BECOME A STOP BIT
087F	79	106	MOV A,C ;ROTATE CHARACTER RIGHT ONE BIT,
0880	1F	107	RAR ;\ MOVING NEXT DATA BIT INTO CARRY
0881	4F	108	MOV C,A
0882	05	109	DCP B ;CHECK IF CHARACTER (AND STOP BIT(S)) DONE
0883	C26F08	110	JNZ C01 ;IF NOT, OUTPUT CURRENT CARRY
0886	E1	111	POP H ;RESTORE STATUS AND RETURN
0887	01	112	POP B
0888	FB	113	EI
0889	09	114	RET
		115	
		116	COIN CONSOL INPUT SUBROUTINE WAITS FOR A KEYSTROKE AND
		117	RETURNS WITH 8 BITS IN REG C.
089A	F3	119	CIN DI
089B	E5	119	PUSH H
089C	0609	120	MVI B,BITSI ;DATA BITS TO BE READ (LAST RETURNED IN CY)
088E	20	121	RIM ;WAIT FOR SYNC BIT TRANSITION
088F	B7	122	ORA A
0890	FABE08	123	JM C11
0893	2AC020	124	LHLD HALFBIT
0896	20	125	DCP L ;WAIT UNTIL MIDDLE OF START BIT
0897	C29608	126	JNE C12
089A	25	127	DCP H
089B	C29608	128	JNZ C12
089E	2AC020	129	LHLD BITTIME ;WAIT OUT BIT TIME
08A1	20	130	DCP L
08A2	C2A108	131	JNE C14
08A5	25	132	DCP H
08A6	C2A108	132	JNZ C14
08A9	20	134	RIM ;CHECK SIG LINE LEVEL
08AA	17	135	RAL ;DATA BIT IN CY
08AB	05	136	DCP B ;DETERMINE IF THIS IS FIRST STOP BIT
08AC	CABE08	137	JZ C15 ;IF SO, JUMP OUT OF LOOP
08AF	79	138	MOV A,C ;ELSE ROTATE INTO PARTIAL CHARACTER IN C
08B0	1F	139	RAR ;ACC HOLDS UPDATED CHARACTER
08B1	4F	140	MOV C,A
08B2	00	141	NOP ;EQUALIZES COUT AND CIN LOOP TIMES
08B3	C2AE08	142	JMP C13
08B6	E1	143	POP H
08B7	FB	144	EI
08B8	09	145	RET ;CHARACTER COMPLETE
		146	
		147	*****
		148	
		149	THE FOLLOWING CODE IS USED BY THE CASSETTE INTERFACE.
		150	SUBROUTINES TAPEO AND TAPEIN ARE USED RESPECTIVELY
		151	TO OUTPUT OR RECEIVE AN EIGHT BIT BYTE OF DATA. REGISTER C
		152	HOLDS THE DATA IN EITHER CASE. REGISTERS A,B,&C ARE ALL DESTROYED.
0810	153	RYCND EQU 16 ;TWICE THE NUMBER OF CYCLES PER TONE BURST	
081E	154	HALFCYQ EQU 20 ;DETERMINES TONE FREQUENCY	

## CRT and Cassette Code (Cont'd)

TS15-II 9090/9095 ASSEMBLER V1.0  
9095 SERIAL I/O NOTE APPENDIX

MODULE

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LOC	OP1	SEQ	SOURCE	STATEMENT
0016		155	CHRATE	EQJ 22 ;SETS SAMPLE RATE
00FA		156	LEADER	EQJ 250 ;NUMBER OF SUCCESSIVE TONE BURSTS COMPRISING LEADER
00FA		157	LOFCH	EQJ 250 ;USED IN PLAYER TO VERIFY PRESENCE OF LEADER
		158		
		159	BLKPRD	OUTPUTS A VERY LONG TONE BURST (LEADER) TIMES
		160		THE NORMAL BURST DURATION) TO ALLOW RECORDER ELECTRONICS
		161		AND ABC TO STABILIZE. THEN OUTPUTS THE REMAINDER OF THE
		162		056 BYTE PAGE POINTED TO BY CH. STARTING AT BYTE (LD).
00B9	0EFA	163	BLKPRD	MVI ;C LEADER:SET UP LEADER BURST LENGTH
00BB	3E02	164		MVI A,00FH ;SET ACCUMULATOR TO RESULT IN TONE BURST
00BD	0DF008	165	BR1	CALL BURST ;OUTPUT TONE
00C0	00	166	DCR	C
00C1	02B008	167	JNZ	BR1 ;SUSTAIN LEADER TONE
00C4	AF	168	XRA	A ;CLEAR ACCUMULATOR & OUTPUT SPACE, SO THAT
00C5	0DF008	169	CALL	BURST ;IN START OF FIRST DATA BYTE CAN BE DETECTED
00C8	4E	170	MOV	C,M ;GET DATA BYTE TO BE RECORDED
00C9	000108	171	CALL	TAPEO ;OUTPUT REGISTER C TO RECORDER
00CC	2C	172	INR	L ;POINT TO NEXT BYTE
00CD	02C008	173	JNZ	BR2
00D0	09	174	RET	;AFTER BLOCK IS COMPLETE
		175		
		176		
		177	TAPEO	OUTPUTS THE BYTE IN REGISTER C TO THE RECORDER.
		178		REGISTERS A,B,C,D,&E ARE ALL USED.
00D1	F3	179	TAPEO	DI
00D2	05	180	PUSH	D ;D&E USED AS COUNTERS BY SUBROUTINE BURST
00D3	0609	181	MVI	E,9 ;WILL RESULT IN 8 DATA BITS AND ONE STOP BIT
00D5	AF	182	XRA	A ;CLEAR ACCUMULATOR
00D6	3E00	183	MVI	A,00FH ;SET ACCUMULATOR TO CAUSE A TONE BURST
00D8	0DF008	184	CALL	BURST
00DB	79	185	MOV	A,C ;MOVE NEXT DATA BIT INTO THE CARRY
00DC	1F	186	RRR	
00DD	4F	187	MOV	C,A ;CARRY WILL BECOME S00 ENABLE IN BURST ROUTINE
00DE	3E01	188	MVI	A,01H ;SET BIT TO BE REPEATEDLY COMPLEMENTED IN BURST
00E0	1F	189	RRR	
00E1	1F	190	RRR	
00E2	0DF008	191	CALL	BURST ;OUTPUT EITHER A TONE OR A PAUSE
00E5	AF	192	XRA	A ;CLEAR ACCUMULATOR
00E6	0DF002	193	CALL	BURST ;OUTPUT PAUSE
00E9	05	194	DCR	B
00EA	02D508	195	JNZ	T01 ;REPEAT UNTIL BYTE FINISHED
00ED	D1	196	POP	D ;RESTORE STATUS AND RETURN
00EE	FB	197	EI	
00EF	09	198	RET	
		199		
00F0	1610	200	BURST	MVI D,CYCNO ;SET NUMBER OF CYCLES
00F2	30	201	BUI	SIM ;COMPLEMENT S00 LINE IF S00 ENABLE BIT SET
00F3	1E1E	202	MVI	E,HALFCYC
00F5	10	203	BUI	E ;REGULATE TONE FREQUENCY
00F6	02F508	204	JNZ	BUI
00F9	EE00	205	XRI	80H ;COMPLEMENT S00 DATA BIT IN ACCUMULATOR
00FB	15	206	DCR	D
00FC	02F208	207	JNZ	BUI ;CONTINUE UNTIL BURST (OR EQUIVLENT PAUSE) FINISHED

## CRT and Cassette Code (Cont'd)

ISIS-II 8080/8085 ASSEMBLER, V1.0  
8085 SERIAL I/O NOTE APPENDIX

MODULE

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LOC	OBJ	SEQ	SOURCE STATEMENT
08FF	C9	208	RET
		209	
		210	:PLAYBK           WAITS FOR THE LONG LEADER BURST TO ARRIVE, THEN CONTINUES
		211	:                   READING BYTES FROM THE RECORDER AND STORING THEM
		212	:                   IN MEMORY STARTING AT LOCATION <HL>.
		213	:                   CONTINUES UNTIL THE END OF THE CURRENT PAGE (<CL>=08FFH) IS REACHED.
0900	0EFA	214	PLAYBK: MVI   C, <LDRCHK>           <<LDRCHK>> SUCCESSIVE HIGHS MUST BE READ
0902	CD3D09	215	PB1: CALL   BITIN                   TO VERIFY THAT THE LEADER IS PRESENT
0905	D20809	216	JNC   PLAYBK                   IF A, AND ELECTRONICS HAS STABILIZED
0908	00	217	DCR   C
0909	C20209	218	JNZ   PB1
090C	CD1509	219	PB2: CALL   TAPEIN               GET DATA BYTE FROM RECORDER
090F	71	220	MOV   M, C                   STORE IN MEMORY
0910	2C	221	INR   L                   INCREMENT POINTER
0911	C20C09	222	JNZ   PB2                   REPEAT FOR REST OF CURRENT PAGE
0914	C9	223	RET
		224	
		225	:TAPEIN CASSETTE TAPE INPUT SUBROUTINE.   READS ONE BYTE OF DATA
		226	:                   FROM THE RECORDER INTERFACE AND RETURNS WITH THE BYTE IN REGISTER C.
0915	0609	227	TAPEIN: MVI   B, 9               READ EIGHT DATA BITS
0917	1600	228	TI1: MVI   D, 00H               CLEAR UP/DOWN COUNTER
0919	15	229	TI2: DCR   D                   DECREMENT COUNTER EACH TIME ONE LEVEL IS READ
091A	CD3D09	230	CALL   BITIN
091D	DA1909	231	JC   TI2                   REPEAT IF STILL AT ONE LEVEL
0920	CD3D09	232	CALL   BITIN
0923	DA1909	233	JC   TI2
0926	14	234	TI3: INR   D                   INCREMENT COUNTER EACH TIME ZERO IS READ
0927	CD3D09	235	CALL   BITIN
092A	D22609	236	JNC   TI3                   REPEAT EACH TIME ZERO IS READ
092D	CD3D09	237	CALL   BITIN
0930	D22609	238	JNC   TI3
0933	7A	239	MOV   A, D
0934	17	240	RAL                       MOVE COUNTER MOST SIGNIFICANT BIT INTO CARRY
0935	79	241	MOV   A, C
0936	1F	242	RAR                       MOVE DATA BIT RECEIVED (CY) INTO BYTE REGISTER
0937	4F	243	MOV   C, A
0938	05	244	DCR   B
0939	C21709	245	JNZ   TI1                   REPEAT UNTIL FULL BYTE ASSEMBLED
093C	C9	246	RET
		247	
093D	1E16	248	BITIN: MVI   E, <KRATE>
093F	1D	249	BI1: DCR   E
0940	C23F09	250	JNZ   BI1                   LIMIT INPUT SAMPLING RATE
0943	20	251	PIM                       SAMPLE SID LINE
0944	17	252	RAL                       MOVE DATA INTO CY BIT
0945	C9	253	RET
		254	
		255	END

PUBLIC SYMBOLS

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## CRT and Cassette Code (Cont'd)

ISIS-II 9090/9095 ASSEMBLER, V1.0  
9095 SERIAL I/O NOTE APPENDIX

MODULE

PAGE 7

### EXTERNAL SYMBOLS

#### USER SYMBOLS

BIT1	A 093F	BITIN	A 0950	BITEI	A 0909	BITSO	A 090B	BITTIM	A 20C8	BLKRCO	A 0889	BR1	A 088D
BR2	A 09C9	BR11	A 091F	BR13	A 0927	BR14	A 0929	BR1D	A 091A	BU1	A 08F2	BU2	A 08F5
BURET	A 09FA	C11	A 099E	C12	A 0996	C13	A 099E	C14	A 09A1	C15	A 08B6	CIN	A 089A
CKRATE	A 0916	CO1	A 096F	CO2	A 0976	COUT	A 0969	CRT1	A 0903	CRTTST	A 0800	CYCNO	A 0910
ECHO	A 080C	HALFEI	A 20CA	HALFCY	A 091E	LDRCHK	A 09FA	LEADCP	A 09FA	PB1	A 0902	PB2	A 090C
PLAYBK	A 0900	S1	A 094A	SIGNON	A 0947	STENG	A 0955	TAPEIN	A 0915	TAPEO	A 09D1	TI1	A 0917
TI2	A 0919	TI3	A 0926	TO1	A 0905								

ASSEMBLY COMPLETE. NO ERRORS.

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## CRT and Cassette Code (Cont'd)

ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE V1.0

PAGE 1

PI1	249#	250				
BITIN	215	230	222	225	227	245#
BITS1	16#	120				
BITS0	15#	95				
BITTIM	12#	60	100	129		
BLKRC0	163#					
BR1	165#	167				
BR2	170#	173				
BR11	45#	47				
BR12	49#	55				
BR14	50#	51				
BR10	28	42#	44			
BU1	201#	207				
BU2	203#	204				
BURST	165	169	184	191	193	200#
CI1	121#	123				
CI2	125#	126	128			
CI3	129#	142				
CI4	130#	131	123			
CI5	137	143#				
CIN	30	118#				
CKPATE	155#	248				
CO1	97#	110				
CO2	101#	102	104			
COUT	25	81	92#			
CRT1	26#	33				
CRTTST	25#					
CYCNO	153#	200				
ECHO	30#	36				
HALFBI	14#	71	124			
HALFCY	154#	202				
LDRCHK	157#	214				
LEADER	156#	163				
PE1	215#	218				
PE2	219#	222				
PLAYBK	214#	216				
S1	77#	83				
SIGNON	29	76#				
STRNG	76	85#				
TAPEIN	219	227#				
TAPE0	171	179#				
TI1	228#	245				
TI2	229#	231	232			
TI3	234#	236	238			
TO1	192#	195				

CROSS REFERENCE COMPLETE





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