Chapter 6

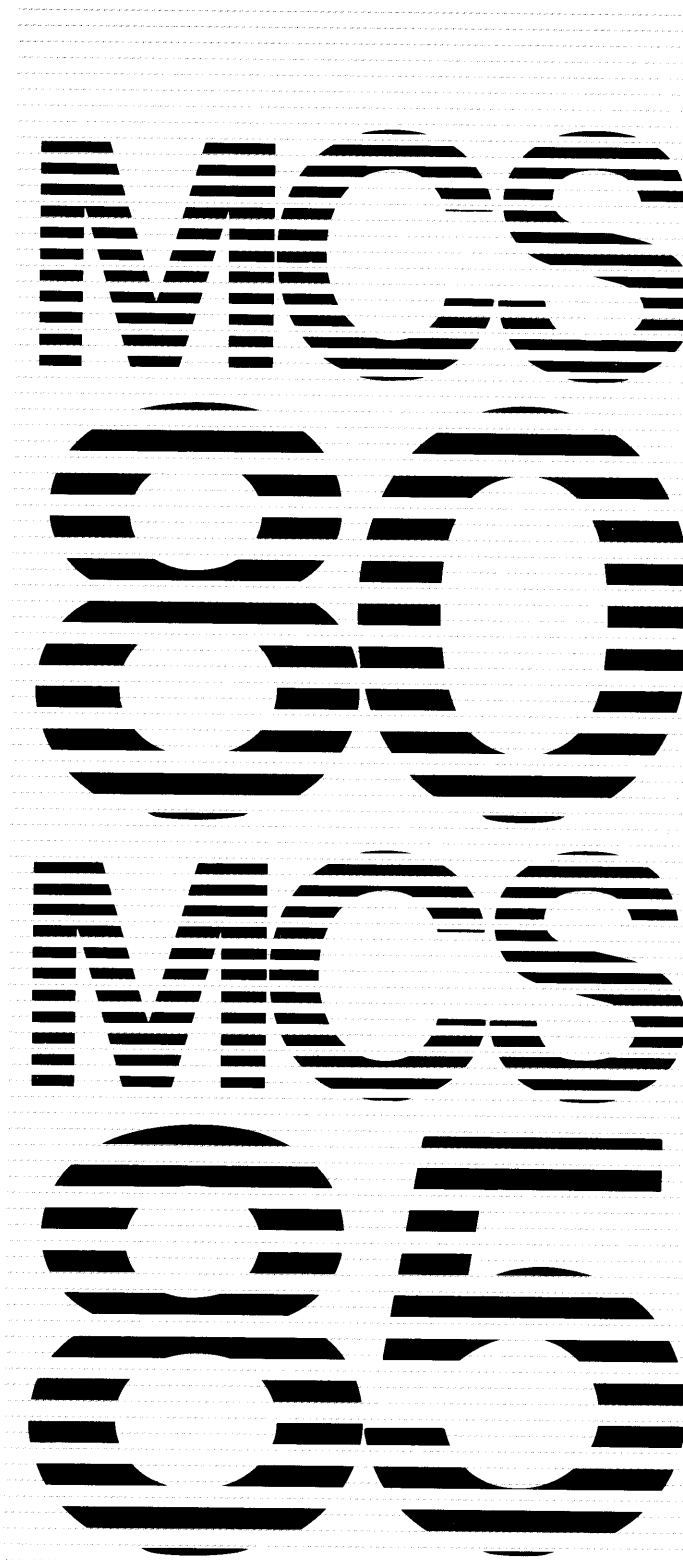
MCS-85™
MCS-80™

Systems
Support
Components

Peripherals

Static RAMs

ROMs-EPROMs



2114A
1024 X 4 BIT STATIC RAM

	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
Max. Access Time (ns)	120	150	200	200	250
Max. Current (mA)	40	40	40	70	70

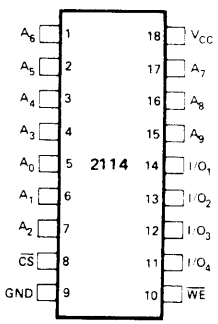
- **HMOS Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18 Pin Package**
- **Completely Static Memory - No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **2114 Replacement**

The Intel 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

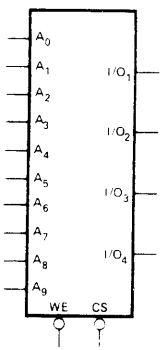
The 2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

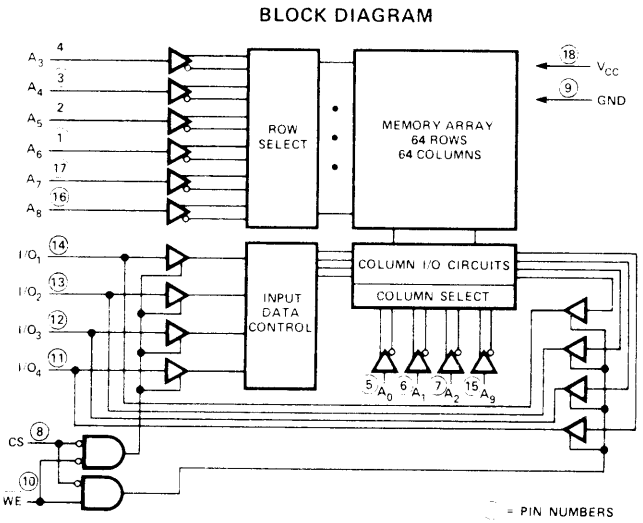
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

2141
4096 X 1 BIT STATIC RAM

	2141-2	2141-3	2141-4	2141-5	2141L-3	2141L-4	2141L-5
Max. Access Time (ns)	120	150	200	250	150	200	250
Max. Active Current (mA)	70	70	55	55	40	40	40
Max. Standby Current (mA)	20	20	12	12	5	5	5

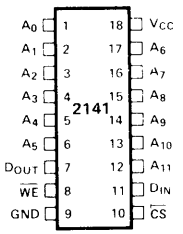
- **HMOS Technology**
- **Industry Standard 2147 Pinout**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **Directly TTL Compatible — All Inputs and Output**
- **Separate Data Input and Output**
- **Three-State Output**
- **High Density 18-Pin Package**

The Intel® 2141 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

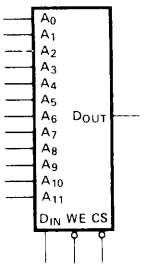
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2141 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The 2141 is placed in an 18-pin package configured with the industry standard pinout, the same as the 2147. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

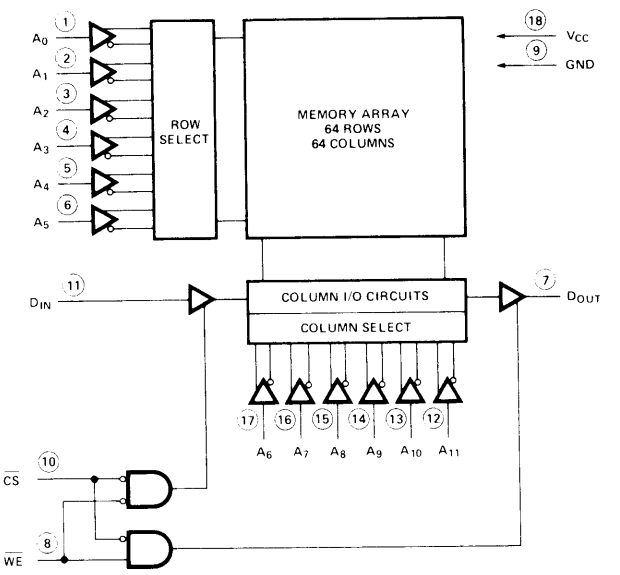
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

2142
1024 X 4 BIT STATIC RAM

	2142-2	2142-3	2142	2142L2	2142L3	2142L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 20 Pin Package**
- **Access Time Selections From 200-450ns**
- **Identical Cycle and Access Times**
- **Low Operating Power Dissipation .1mW/Bit Typical**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**

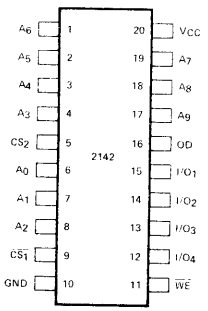
The Intel® 2142 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply.

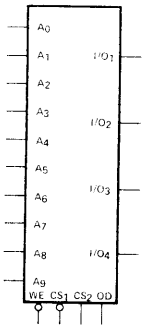
The 2142 is placed in a 20-pin package. Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided for easy and flexible selection of individual packages when outputs are OR-tied. An Output Disable is included for direct control of the output buffers.

The 2142 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

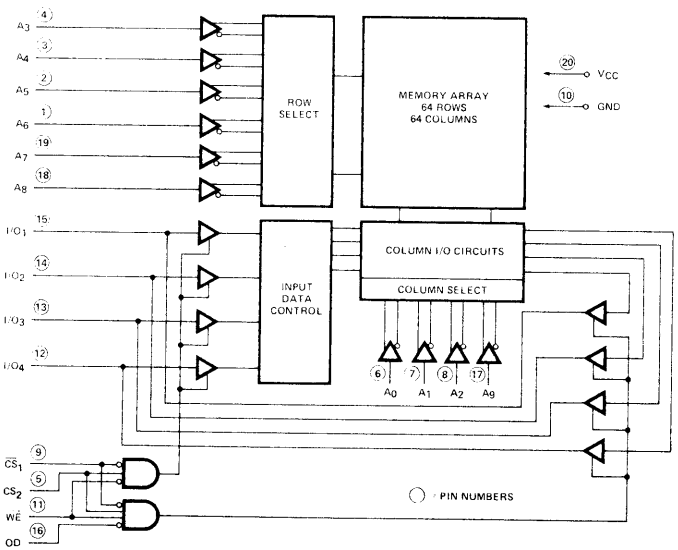
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
I/O_1–I/O_4	DATA INPUT/OUTPUT		

2148
1024 x 4 BIT STATIC RAM

	2148-3	2148	2148-6
Max. Access Time (ns)	55	70	85
Max. Active Current (mA)	125	125	125
Max. Standby Current (mA)	30	30	30

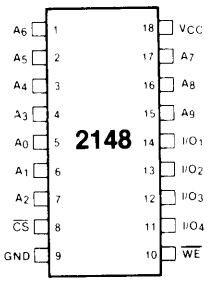
- **HMOS Technology**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Common Data Input and Output**
- **Three-State Output**

The Intel® 2148 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

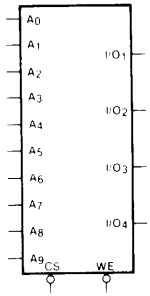
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — disabling the 2148 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are disabled.

The 2148 is assembled in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

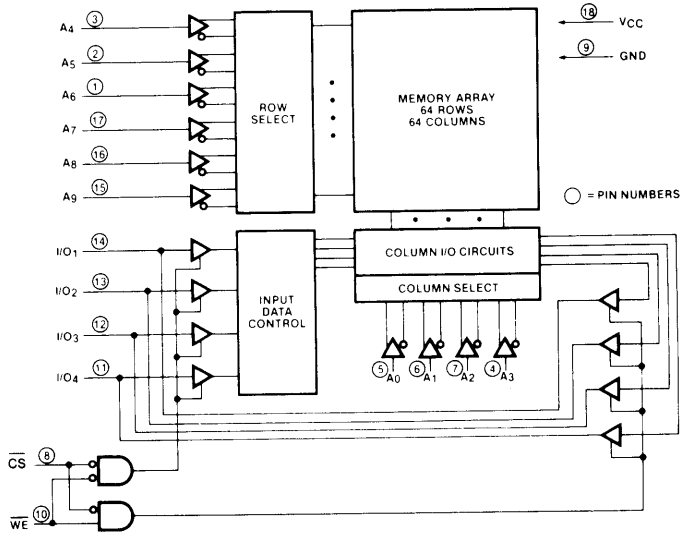
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

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MCS-85™
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Static RAMs

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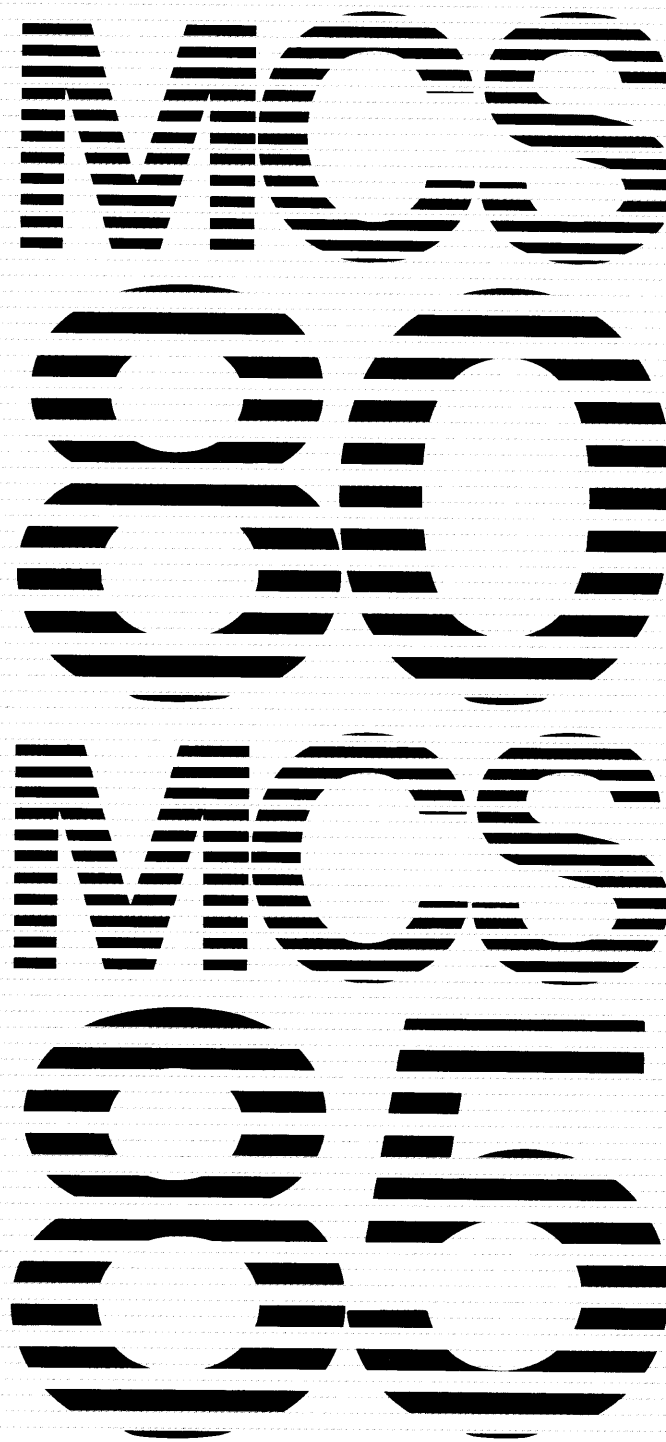


2716
16K (2K x 8) UV ERASABLE PROM

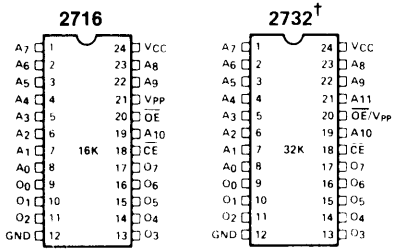
- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
  - **— 650 ns Max. 2716-6**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 2732 EPROM**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

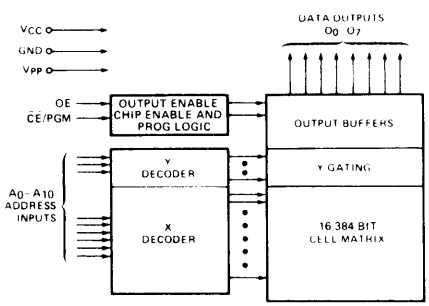
PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



2732
32K (4K x 8) UV ERASABLE PROM

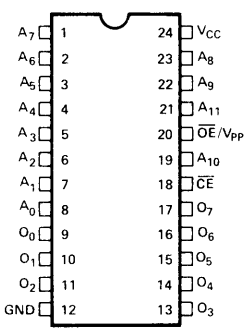
- **Fast Access Time:**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  150mA Max. Active Current
  30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50ms Pulse**
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-30 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-30 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION



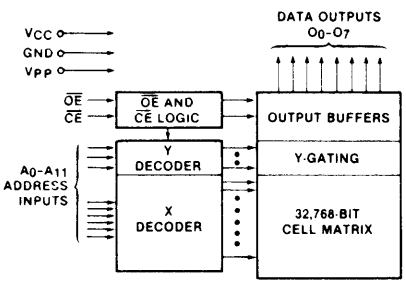
PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

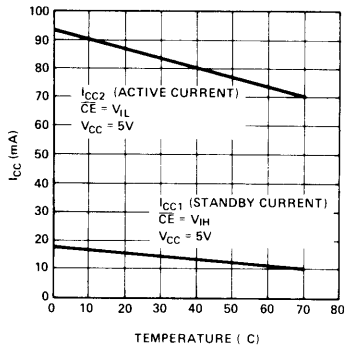
READ OPERATION

Symbol	Parameter	Limits Min.	Typ. [1]	Max.	Unit	Conditions
I_{LI1}	Input Load Current (except $\overline{OE}/V_{PP}$)			10	μA	V_{IN} = 5.25V
I_{LI2}	$\overline{OE}/V_{PP}$ Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{CC1}	V_{CC} Current (Standby)		15	30	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)		85	150	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400μA

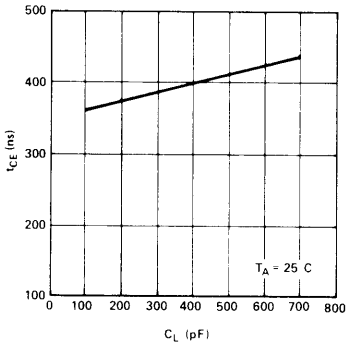
Note: 1. Typical values are for T_A = 25°C and nominal supply voltages.

TYPICAL CHARACTERISTICS

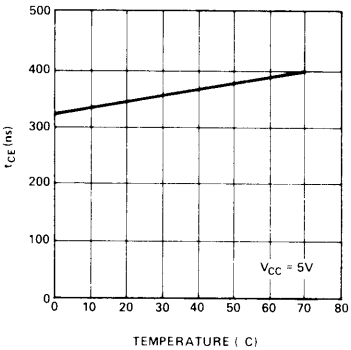
I_{CC} CURRENT VS. TEMPERATURE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. CAPACITANCE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. TEMPERATURE



A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	2732 Limits		2732-6 Limits		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address to Output Delay		450		550	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		450		550	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

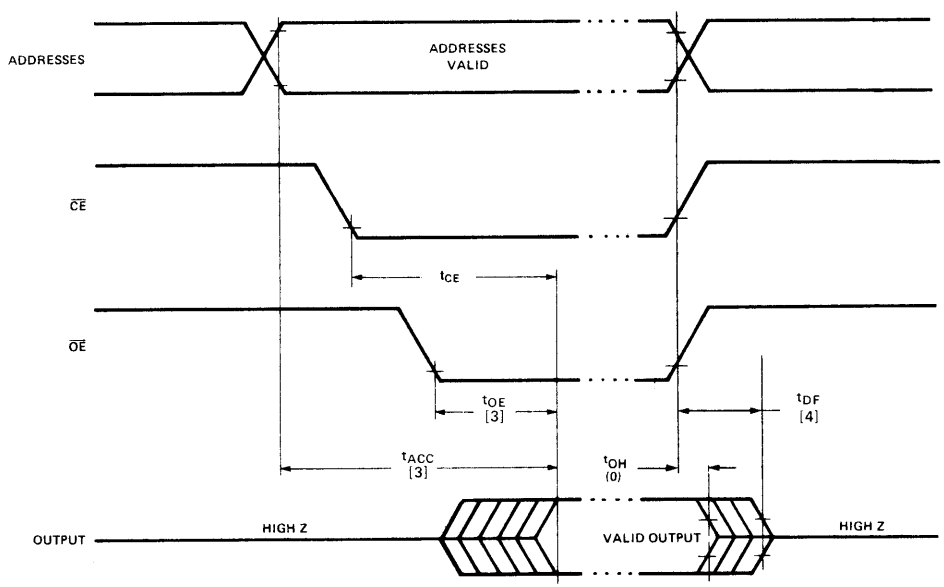
CAPACITANCE [1] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS [2]



NOTES:
1. THIS PARAMETER IS ONLY SAMPLED AND IS NOT 100% TESTED.
2. ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE NSEC UNLESS OTHERWISE SPECIFIED.
3. $\overline{OE}$ MAY BE DELAYED UP TO 330ns AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
4. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2732 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2732 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog page 4-83) for the 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2732 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2732 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

TABLE 1. Mode Selection

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The 2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The 2732 has a standby mode which reduces the active power current by 80%, from 150mA to 30mA. The 2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

Programming

Initially, and after each erasure, all bits of the 2732 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55msec. The 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732s.

Program Inhibit

Programming of multiple 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732s may be common. A TTL level program pulse applied to a 2732's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that 2732. A high level $\overline{CE}$ input inhibits the other 2732s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

2758
8K (1K x 8) UV ERASABLE LOW POWER PROM

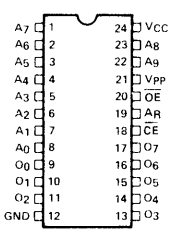
- **Single +5V Power Supply**
- **Simple Programming Requirements**
  - **Single Location Programming**
  - **Programs with One 50 ms Pulse**
- **Low Power Dissipation**
  525 mW Max. Active Power
  132 mW Max. Standby Power
- **Fast Access Time: 450 ns Max. in Active and Standby Power Modes**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**
- **Three-State Outputs for OR-Ties**

The Intel® 2758 is a 8192-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2758 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. The total programming time for all 8192 bits is 50 seconds.

The 2758 has a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW, while the maximum standby power dissipation is only 132 mW, a 75% savings. Power-down is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

A 2758 system may be designed for total upwards compatibility with Intel's 16K 2716 EPROM (see Applications Note 30). The 2758 maintains the simplest and fastest method yet devised for programming EPROMs — single pulse TTL-level programming. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time — either individually, sequentially, or at random, with the single address location programming.

PIN CONFIGURATION



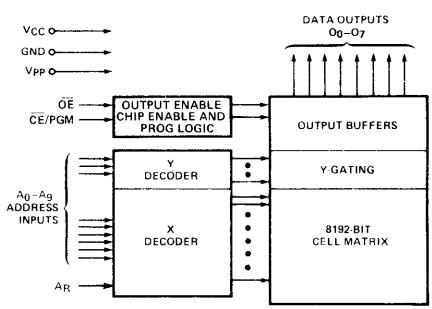
MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	A_R (19)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS
A_R	SELECT REFERENCE INPUT LEVEL

BLOCK DIAGRAM



3604A, 3624A FAMILY
4K (512 x 8) HIGH-SPEED PROM

	3604A-2 3624A-2	3604A 3624A	3604AL
Max. T_A(ns)	60	70	90
Max. I_{CC}(mA)	170	170	130/25*

***Standby Current When The Chip is Deselected.**

- **Fast Access Time --60ns Max (3604A-2, 3624A-2)**
- **Low Standby Power Dissipation (3604AL) --32 μW/Bit Max**
- **Open Collector (3604A) or Three State (3624A) Outputs**
- **Four Chip Select Inputs For Easy Memory Expansion**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 24 Pin DIP**

The Intel® 3604A/3624A are 4096-bit bipolar PROMs organized as 512 words by 8 bits. The fast second generation 3604A/3624A replaces its Intel predecessor, the 3604/3624. Higher speed PROMs, the 3604A-2/3624A-2, are now available at 60 ns. All 3604A/3624A specifications, except programming, are the same as or better than the 3604/3624. Once programmed, the 3604A/3624A are interchangeable with the 3604/3624

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. Low standby power dissipation can be achieved with the 3604AL. The standby power dissipation is approximately 20% of the active power dissipation.

The 3604A/3624A are available in a hermetic 24-pin dual in-line package. These PROMs are manufactured with the time-proven polycrystalline silicon fuse technology.

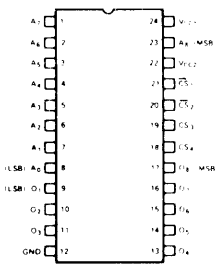
Mode/Pin Connection		Pin 22	Pin 24
READ:	3604A, 3604A-2 3624A, 3624A-2	No Connect or 5V	5V
	3604AL	+5V	Must be Left Open
PROGRAM:	3604A, 3604A-2 3624A, 3624A-2	Pulsed 12.5V	Pulsed 12.5V
	3604AL	Pulsed 12.5V	Pulsed 12.5V
STANDBY:	3604AL	Power dissipation is automatically reduced whenever the 3604AL is deselected.	

PIN NAMES

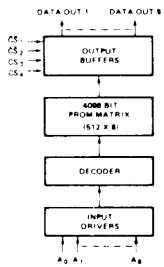
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$, CS_3–CS_4 [1]	CHIP SELECT INPUTS
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

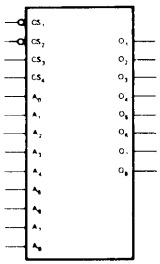
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



3605A, 3625A
4K (1K x 4) PROM

3605A-1, 3625A-1	50 ns Max.
3605A, 3625A	60 ns Max.

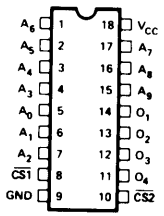
- ± 10% Power Supply Tolerance
- Fast Access Time: 40 ns Typically
- Lower Power Dissipation: 0.14 mW/Bit Typically
- Simple Memory Expansion Two Chip Select Inputs
- Open Collector (3605A) and Three-State (3625A) Outputs
- Polycrystalline Silicon Fuse for Higher Reliability
- Hermetic 18-Pin DIP

The Intel® 3605A and 3625A families are high density, 4096-bit bipolar PROMs organized as 1024 words by 4 bits. The 1024 by 4 organization gives ideal word or bit modularity for memory array expansion. The 3605A has open collector outputs and the 3625A has three-state outputs. The 3605A and 3625A are fully specified over the 0°C to 75°C temperature range with ± 10% power supply variation. Maximum access times of 50 ns (3605A-2/3625A-2) and 60 ns (3605A/3625A) are available at a typical power dissipation of 0.14 mW/bit.

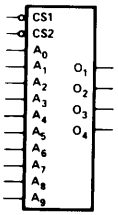
The 3605A/3625A are packaged in an 18-pin dual in-line hermetic package with 300 milli-inch centers. Thus, twice the bit density can be achieved with the 3605A/3625A in the same memory board areas as 512 by 8-bit PROMs in 24-pin packages.

The highly reliable polycrystalline silicon fuse technology is used in the manufacturing of the 3605A and 3625A families. All outputs are initially a logical high and logic low levels can be electrically programmed in selected bit locations.

PIN CONFIGURATION



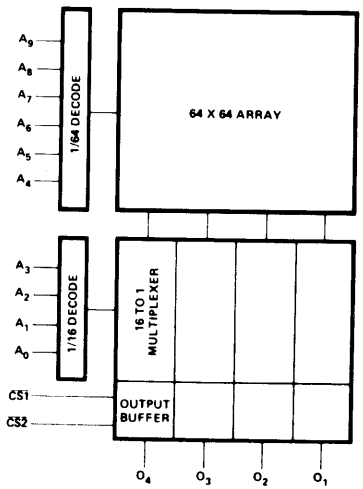
LOGIC SYMBOL



PIN NAMES

A_0 - A_9	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
O_1 - O_4	OUTPUTS

BLOCK DIAGRAM



A. C. Characteristics V_{CC} = +5V ±10%, T_A = 0°C to +75°C

Symbol	Parameter	Max. Limits 3605A-1 3625A-1	Max. Limits 3605A 3625A	Unit	Conditions
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	50	60	ns	$\overline{CS}_1$=$\overline{CS}_2$=V_{IL} to select the PROM.
t_{S++}	Chip Select to Output Delay	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

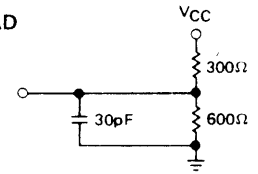
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	3	8	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	4	8	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	5	10	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

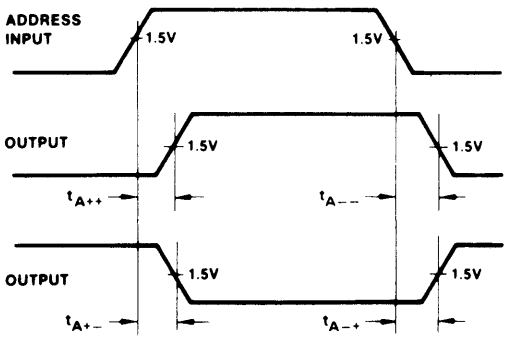
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

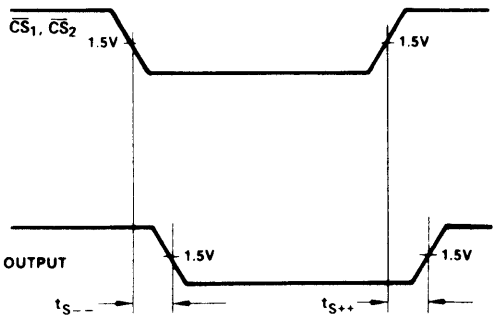


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions on page 4-89.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to +75°C

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.5V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.5V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}=5.5V, V_A = 5.5V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}=5.5V, V_S = 5.5V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.5V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.5V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.5V, I_{OL}=15mA
I_{CEX}	3605A Output Leakage Current			40	μA	V_{CC}=5.5V, V_{CE}=5.5V
I_{CC}	Power Supply Current		110	140	mA	V_{CC}=5.5V, V_{AO}→V_{A9}=0V, $\overline{CS}_1$=$\overline{CS}_2$=V_{IH}
V_{IL}	Input "Low" Voltage			0.85	V	
V_{IH}	Input "High" Voltage	2.0			V	

3625, 3625-2 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	V_O=5.5V or 0.45V, V_{CC}=5.5V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[1]	Output Short Circuit Current	-20	-35	-80	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.4mA, V_{CC} = 4.5V

NOTES: 1. Unmeasured outputs are open during this test.

3628
8K (1K X 8) BIPOLAR PROM

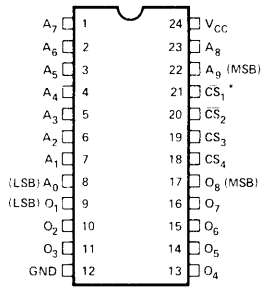
3628	80 ns Max.
3628-4	100 ns Max.

- **Fast Access Time: 65 ns Typically**
- **Low Power Dissipation: 0.09mW/Bit Typically**
- **Four Chip Select Inputs for Easy Memory Expansion**
- **Three-State Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

The Intel* 3628 is a fully decoded 8192-bit PROM organized as 1024 words by 8 bits. The worst case access time of 80 ns is specified over the 0°C to 75°C temperatue range and 5% V_{CC} power supply tolerances. There are four chip selects provided to facilitate expansion into larger PROM arrays. It uses Schottky clamped TTL technology with poly-crystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

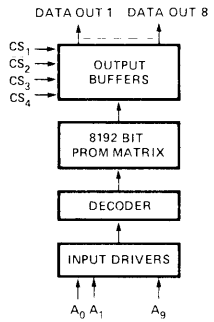
Prior to the 8192 bit 3628, the highest density bipolar PROM available was 4096 bits. The high density of the 3628 now easily doubles the capacity without an increase in area on existing designs currently using 512 words by 8 bit PROMs. There is also little, if any, penalty in power since the 3628 power/bit is approximately one-half that of 4K PROMs. The 3628 is packaged in a hermetic 24-pin dual in-line package.

PIN CONFIGURATION

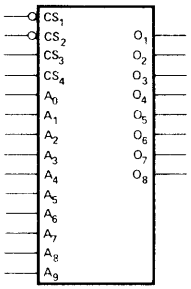


*PROGRAMMING PIN

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A_0 - A_9	ADDRESS INPUTS
$\overline{CS_1}$ - $\overline{CS_2}$, CS_3 - CS_4	CHIP SELECT INPUTS [1]
O_1 - O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS_1} = CS_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$

PROGRAMMING

The programming specifications are described in the PROM programming section of the Data Catalog.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for $V_{CC} = +5.0V \pm 5\%$, $T_A = 0°C$ to $+75°C$

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.25V$, $V_A = 5.25V$
I_{RS}	Chip Select Input Leakge Current			40	μA	$V_{CC} = 5.25V$, $V_S = 5.0V$
$\|I_O\|$	Output Leakge for High Impedance State			100	μA	$V_O = 5.25V$ or 0.45V, $V_{CC} = 5.25V$, $CS_1 = CS_2 = 2.4V$
I_{SC}[2]	Output Short Circuit Current	−20	−35	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_A = -10mA$
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_S = -10mA$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.75V$, $I_{OL} = 10mA$
V_{OH}	Output High Voltage	2.4	3.4		V	$I_{OH} = -2.4mA$, $V_{CC} = 4.75V$
I_{CC}	Power Supply Current		150	190	mA	$V_{CC} = 5.25V$, $V_{A0} \rightarrow V_{A9} = 0V$, PROM deselected
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V$

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A.C. CHARACTERISTICS V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMITS 3628	MAX. LIMITS 3628-4	UNIT	CONDITIONS
t_A	Address to Output Delay	80	100	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	40	45	ns	
t_{DIS}	Output Disable Time	40	45	ns	

CAPACITANCE [1] T_A = 25°C, f = 1 MHz

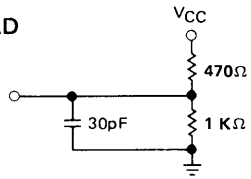
SYMBOL	PARAMETER	TYP. LIMITS TYP.	TYP. LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

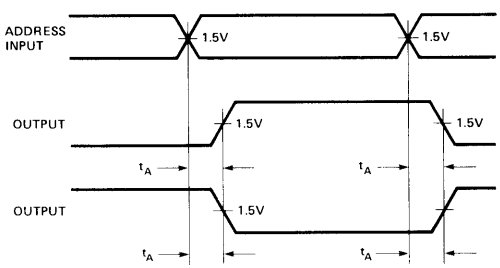
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

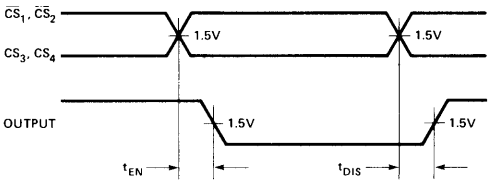


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3636
16K (2K x 8) BIPOLAR PROM

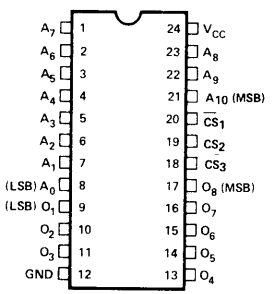
3636-1	65 ns Max.
3636	80 ns Max.

- **Fast Access Time: 50 ns Typically**
- **Low Power Dissipation: 0.05 mW/Bit Typically**
- **Three Chips Select Input for Easy Memory Expansion**
- **Three-State Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

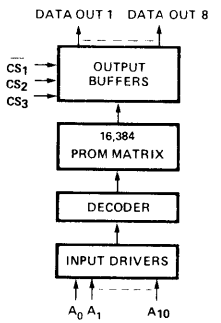
The Intel® 3636 is a fully decoded 16,384 bit PROM organized as 2048 words by 8 bits. The worst case access time of 65 ns is specified over the 0°C to 75°C temperature range and 10% V_{CC} power supply tolerances. There are three chip selects provided to facilitate expansion into larger PROM arrays. The PROMs use the Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

Prior to the 16,384 bit 3636, the highest density bipolar PROM available was 8192 bits. The high density of the 3636 now easily doubles the capacity without an increase in area on existing designs currently using 1024 by 8 bit PROMs. There is also little, if any, penalty in power since the power/bit is approximately one-half that of 8K PROMs. The 3636 is packaged in a hermetic 24-pin dual in-line package.

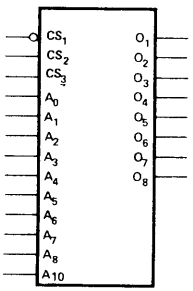
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
$\overline{CS}_1$, CS_2, CS_3	CHIP SELECT INPUTS(1)
O_1-O_8	DATA OUTPUTS

(1) To select the PROM $\overline{CS}_1 = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$

PROGRAMMING

The programming specifications are described in the PROM Programming Section of the Data Catalogue.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for $V_{CC} = +5.0V \pm 10\%$, $T_A = 0°C$ to $+75°C$

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_A = 5.5V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_S = 5.5V$
$\|I_O\|$	Output Leakage for High Impedance State			100	μA	$V_O = 5.5V$ or $0.45V$, $V_{CC} = 5.5V$, $CS_1 = 2.4V$
I_{SC}[2]	Output Short Circuit Current	−20	−40	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_A = -10$ mA
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_S = -10$ mA
V_{OH}	Output High Voltage	2.4	3.2		V	$I_{OH} = -2.4$ mA, $V_{CC} = 4.5V$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.5V$, $I_{OL} = 10$ mA
I_{CC}	Power Supply Current		150	185	mA	$V_{CC} = 5.5V$
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V \pm 10\%$

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. Unmeasured outputs are open during this test.

A.C. CHARACTERISTICS $V_{CC} = \pm 5V \pm 10\%$, $T_A = 0°C$ to $+75°C$

SYMBOL	PARAMETER	MAX. LIMITS		UNIT	CONDITIONS
		3636-1	3636		
t_A	Address to Output Delay	65	80	ns	$\overline{CS_1} = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	40	50	ns	
t_{DIS}	Output Disable Time	40	50	ns	

CAPACITANCE [1] $T_A = 25°C$, f = 1 MHz

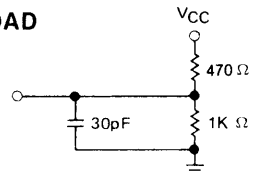
SYMBOL	PARAMETER	TYP. LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

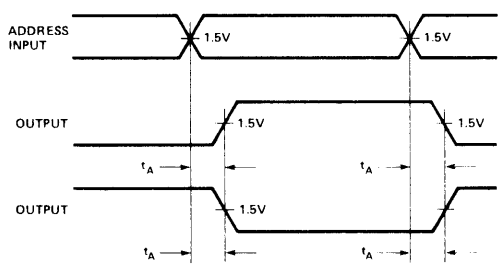
Conditions of Test:
Input pulse amplitudes: 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test: 2.5 MHz

10 mA TEST LOAD



WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY