

Chapter 6

MCS-85™

MCS-80™

Systems
Support
Components

Peripherals

Static RAMs

ROMs-EPROMs

MOS

8085

MOS

8085



8080A/8080A-1/8080A-2 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

- TTL Drive Capability
- 2 μ s (- 1:1.3 μ s, - 2:1.5 μ s) Instruction Cycle
- Powerful Problem Solving Instruction Set
- 6 General Purpose Registers and an Accumulator
- 16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory
- 16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment
- Decimal, Binary, and Double Precision Arithmetic
- Ability to Provide Priority Vectored Interrupts
- 512 Directly Addressed I/O Ports

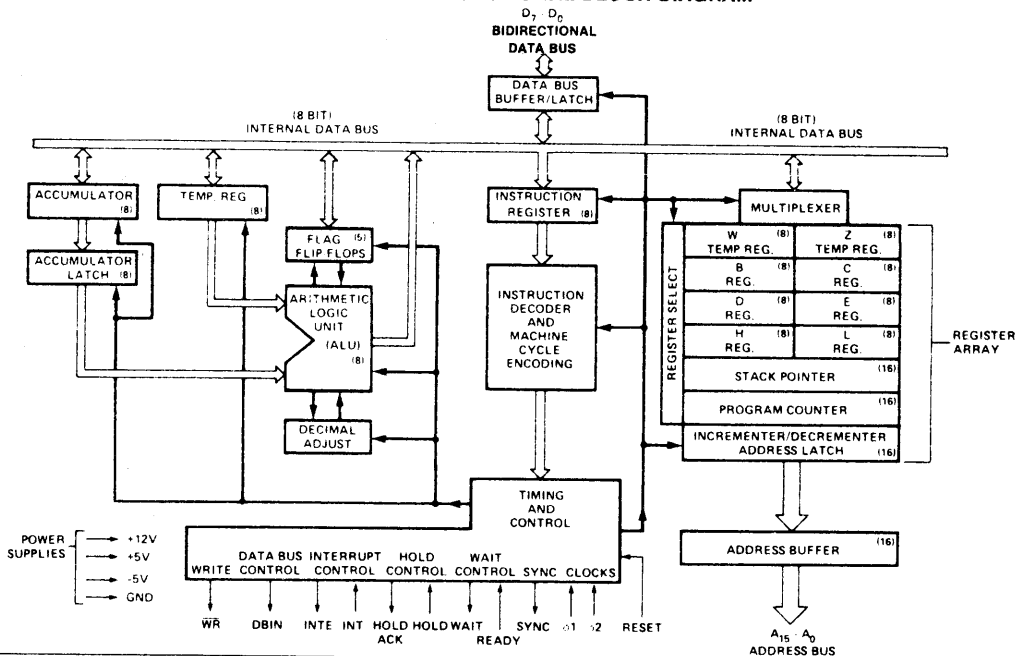
The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data buses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data buses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data buses into a high impedance state. This permits OR-tying these buses with other controlling devices for (DMA) direct memory access or multi-processor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A₁₅-A₀ (output three-state)

ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A₀ is the least significant address bit.

D₇-D₀ (input/output three-state)

DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D₀ is the least significant bit.

SYNC (output)

SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)

DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)

READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)

WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

WR (output)

WRITE; the $\overline{\text{WR}}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{\text{WR}}$ signal is active low ($\overline{\text{WR}} = 0$).

HOLD (input)

HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

- the CPU is in the HALT state.
- the CPU is in the T₂ or T_W state and the READY signal is active. As a result of entering the HOLD state the CPU ADDRESS BUS (A₁₅-A₀) and DATA BUS (D₇-D₀) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)

HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus

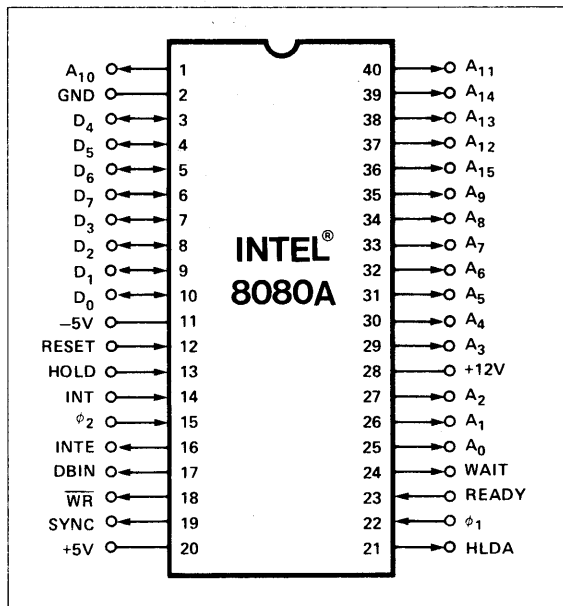


Figure 1. Pin Configuration

will go to the high impedance state. The HLDA signal begins at:

- T₃ for READ memory or input.
- The Clock Period following T₃ for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2 .

INTE (output)

INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T₁ of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)

INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input) [1]

RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

- V_{SS} Ground Reference.
- V_{DD} +12 ± 5% Volts.
- V_{CC} +5 ± 5% Volts.
- V_{BB} -5 ± 5% Volts (substrate bias).
- ϕ_1, ϕ_2 2 externally supplied clock phases. (non TTL compatible)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias 0°C to +70°C
 Storage Temperature -65°C to +150°C
 All Input or Output Voltages
 With Respect to V_{BB} -0.3V to +20V
 V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB} -0.3V to +20V
 Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V _{ILC}	Clock Input Low Voltage	V _{SS} -1		V _{SS} +0.8	V	I _{OL} = 1.9mA on all outputs, I _{OH} = -150µA.
V _{IHC}	Clock Input High Voltage	9.0		V _{DD} +1	V	
V _{IL}	Input Low Voltage	V _{SS} -1		V _{SS} +0.8	V	
V _{IH}	Input High Voltage	3.3		V _{CC} +1	V	
V _{OL}	Output Low Voltage			0.45	V	
V _{OH}	Output High Voltage	3.7			V	
I _{DD(AV)}	Avg. Power Supply Current (V _{DD})		40	70	mA	Operation T _{CY} = .48 µsec
I _{CC(AV)}	Avg. Power Supply Current (V _{CC})		60	80	mA	
I _{BB(AV)}	Avg. Power Supply Current (V _{BB})		.01	1	mA	
I _{IL}	Input Leakage			±10	µA	V _{SS} ≤ V _{IN} ≤ V _{CC}
I _{CL}	Clock Leakage			±10	µA	V _{SS} ≤ V _{CLOCK} ≤ V _{DD}
I _{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	µA mA	V _{SS} ≤ V _{IN} ≤ V _{SS} + 0.8V V _{SS} + 0.8V ≤ V _{IN} ≤ V _{CC}
I _{FL}	Address and Data Bus Leakage During HOLD			+10 -100	µA	V _{ADDR/DATA} = V _{CC} V _{ADDR/DATA} = V _{SS} + 0.45V

CAPACITANCE

T_A = 25°C V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C _φ	Clock Capacitance	17	25	pf	f _c = 1 MHz
C _{IN}	Input Capacitance	6	10	pf	Unmeasured Pins Returned to V _{SS}
C _{OUT}	Output Capacitance	10	20	pf	

NOTES:

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and V_{IN} > V_{IH} an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

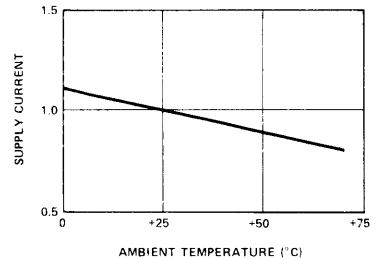


Figure 2. Typical Supply Current vs. Temperature, Normalized^[3]

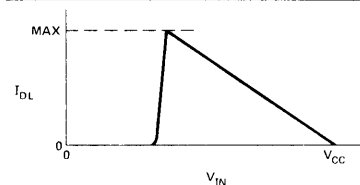


Figure 3. Data Bus Characteristic During DBIN

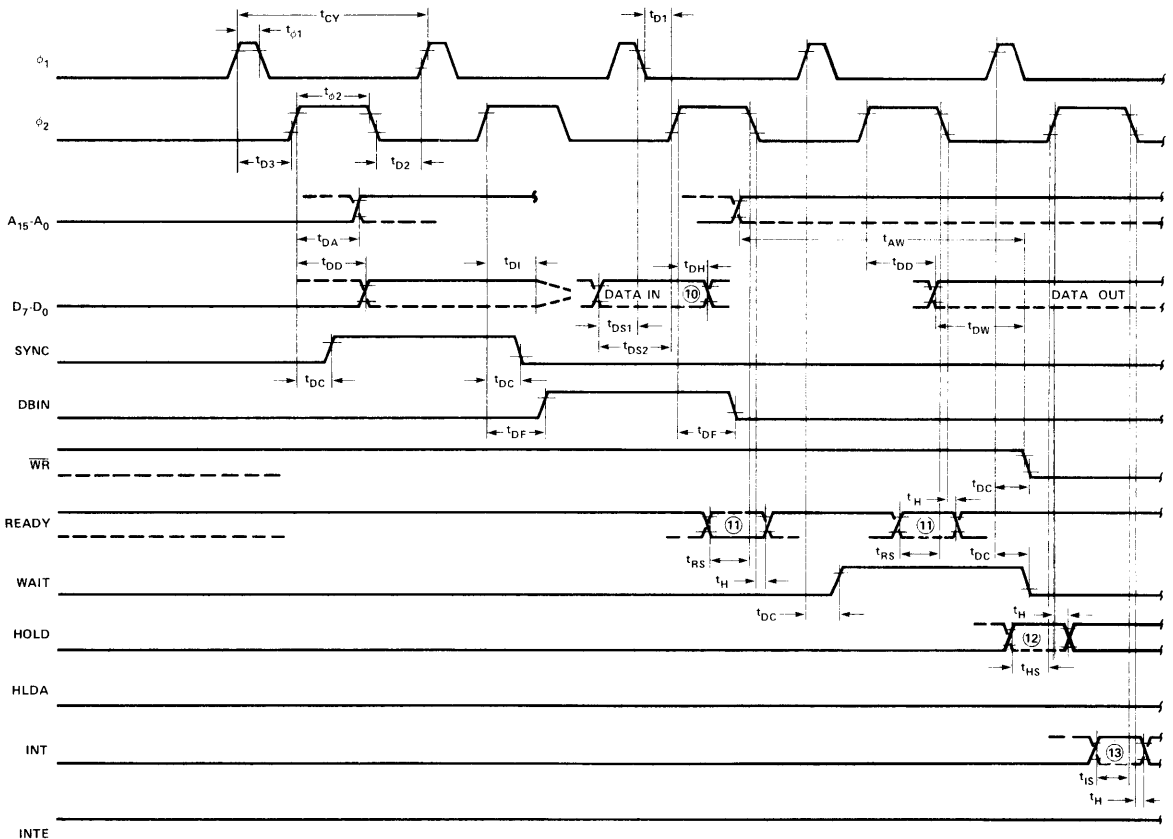
A.C. CHARACTERISTICS (8080A)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = +12\text{V} \pm 5\%$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	-1 Min.	-1 Max.	-2 Min.	-2 Max.	Unit	Test Condition	
$t_{CY}^{[3]}$	Clock Period	0.48	2.0	0.32	2.0	0.38	2.0	μsec		
t_r, t_f	Clock Rise and Fall Time	0	50	0	25	0	50	nsec		
$t_{\phi 1}$	ϕ_1 Pulse Width	60		50		60		nsec		
$t_{\phi 2}$	ϕ_2 Pulse Width	220		145		175		nsec		
t_{D1}	Delay ϕ_1 to ϕ_2	0		0		0		nsec		
t_{D2}	Delay ϕ_2 to ϕ_1	70		60		70		nsec		
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		60		70		nsec		
$t_{DA}^{[2]}$	Address Output Delay From ϕ_2		200		150		175	nsec		} $C_L = 100\text{ pF}$
$t_{DD}^{[2]}$	Data Output Delay From ϕ_2		220		180		200	nsec		
$t_{DC}^{[2]}$	Signal Output Delay From ϕ_2 or ϕ_2 (SYNC, WR, WAIT, HLDA)		120		110		120	nsec		} $C_L = 50\text{ pF}$
$t_{DF}^{[2]}$	DBIN Delay From ϕ_2		25	140	25	130	25	140	nsec	
$t_{DI}^{[1]}$	Delay for Input Bus to Enter Input Mode		t_{DF}		t_{DF}		t_{DF}	nsec		
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		10		20		nsec		

WAVEFORMS

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



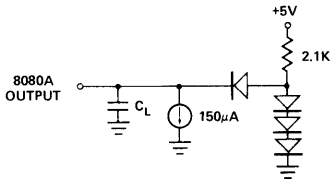
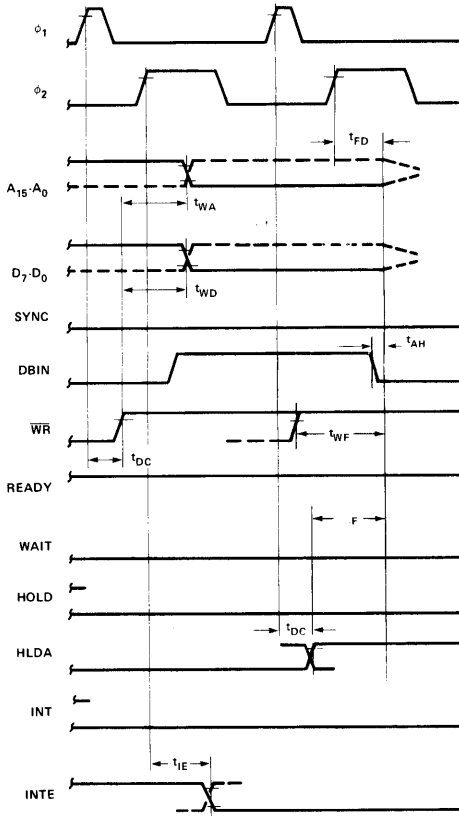
A.C. CHARACTERISTICS (8080A)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = +12\text{V} \pm 5\%$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	-1 Min.	-1 Max.	-2 Min.	-2 Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		120		130		nsec	$C_L = 50\text{ pF}$
$t_{DH}^{[1]}$	Data Hold time From ϕ_2 During DBIN	[1]		[1]		[1]		nsec	
$t_{IE}^{[2]}$	INTE Output Delay From ϕ_2		200		200		200	nsec	
t_{RS}	READY Setup Time During ϕ_2	120		90		90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		120		120		nsec	
t_{IS}	INT Setup Time During ϕ_2	120		100		100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		0		0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120		120		120	nsec	
$t_{AW}^{[2]}$	Address Stable Prior to WR	[5]		[5]		[5]		nsec	
$t_{DW}^{[2]}$	Output Data Stable Prior to WR	[6]		[6]		[6]		nsec	
$t_{WD}^{[2]}$	Output Data Stable From WR	[7]		[7]		[7]		nsec	$C_L = 100\text{ pF}$: Address, Data $C_L = 50\text{ pF}$: WR, HLDA, DBIN
$t_{WA}^{[2]}$	Address Stable From WR	[7]		[7]		[7]		nsec	
$t_{HF}^{[2]}$	HLDA to Float Delay	[8]		[8]		[8]		nsec	
$t_{WF}^{[2]}$	WR to Float Delay	[9]		[9]		[9]		nsec	
$t_{AH}^{[2]}$	Address Hold Time After DBIN During HLDA	-20		-20		-20		nsec	

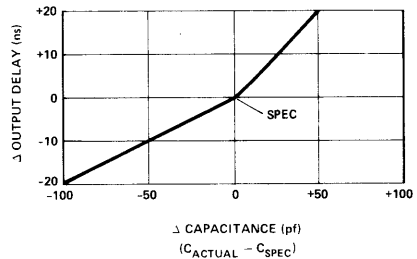
NOTES: (Parenthesis gives -1, -2 specifications, respectively)

- Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. $t_{DH} = 50\text{ ns}$ or t_{DF} , whichever is less.
- Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{D2} + t_{r\phi1} \geq 480\text{ ns}$ (-1:320 ns, -2:380 ns).

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having $V_{IH} = 3.3\text{V}$:

- Maximum output rise time from .8V to 3.3V = 100ns @ $C_L = \text{SPEC}$.
- Output delay when measured to 3.0V = SPEC +60ns @ $C_L = \text{SPEC}$.
- If $C_L \neq \text{SPEC}$, add .6ns/pF if $C_L > C_{\text{SPEC}}$, subtract .3ns/pF (from modified delay) if $C_L < C_{\text{SPEC}}$.
- $t_{AW} = 2 t_{CY} - t_{D3} - t_{r\phi2} - 140\text{ ns}$ (-1:110 ns, -2:130 ns).
- $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170\text{ ns}$ (-1:150 ns, -2:170 ns).
- If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10\text{ns}$. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
- $t_{HF} = t_{D3} + t_{r\phi2} - 50\text{ns}$.
- $t_{WF} = t_{D3} + t_{r\phi2} - 10\text{ns}$.
- Data in must be stable for this period during DBIN $\cdot T_3$. Both t_{DS1} and t_{DS2} must be satisfied.
- Ready signal must be stable for this period during T_2 or T_W . (Must be externally synchronized.)
- Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3 , T_4 , T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
- Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
- This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from sub-routines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to

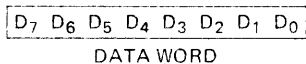
increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

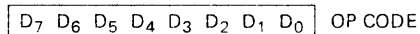
Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.



The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

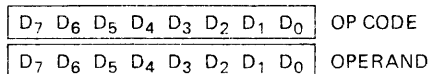
One Byte Instructions



TYPICAL INSTRUCTIONS

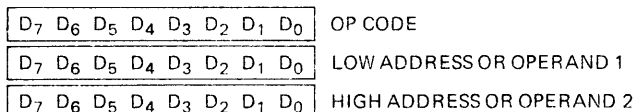
Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable
Interrupt instructions

Two Byte Instructions



Immediate mode or I/O instructions

Three Byte Instructions



Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

8080 INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code(1)								Clock(2)	Mnemonic	Description	Instruction Code(1)								Clock(2)
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				Cycles	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	
MOVE, LOAD, AND STORE																					
MOV _{r1,r2}	Move register to register	0	1	D	D	D	S	S	S	5	JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
MOV _{M,r}	Move register to memory	0	1	1	1	0	S	S	S	7	PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
MOV _{r,M}	Move memory to register	0	1	D	D	D	1	1	0	7	CALL										
MVI _r	Move immediate register	0	0	D	D	D	1	1	0	7	CALL	Call unconditional	1	1	0	0	1	1	0	1	17
MVI _M	Move immediate memory	0	0	1	1	0	1	1	0	10	CC	Call on carry	1	1	0	1	1	1	0	0	11/17
LXI _B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10	CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
LXI _D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10	CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
LXI _H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10	CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
STAX _B	Store A indirect	0	0	0	0	0	0	1	0	7	CP	Call on positive	1	1	1	1	0	1	0	0	11/17
STAX _D	Store A indirect	0	0	0	1	0	0	1	0	7	CM	Call on minus	1	1	1	1	1	1	0	0	11/17
LDAX _B	Load A indirect	0	0	0	0	1	0	1	0	7	CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
LDAX _D	Load A indirect	0	0	0	1	1	0	1	0	7	CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
STA	Store A direct	0	0	1	1	C	0	1	0	13	RETURN										
LDA	Load A direct	0	0	1	1	1	0	1	0	13	RET	Return	1	1	0	0	1	0	0	1	10
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16	RC	Return on carry	1	1	0	1	1	0	0	0	5/11
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16	RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4	RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
STACK OPS																					
PUSH _B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11	RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
PUSH _D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11	RP	Return on positive	1	1	1	1	0	0	0	0	5/11
PUSH _H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11	RM	Return on minus	1	1	1	1	1	0	0	0	5/11
PUSH _{PSW}	Push A and Flags on stack	1	1	1	1	0	1	0	1	11	RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
POP _B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10	RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
POP _D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10	RESTART										
POP _H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10	RST	Restart	1	1	A	A	A	1	1	1	11
POP _{PSW}	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10	INCREMENT AND DECREMENT										
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18	INR _r	Increment register	0	0	D	D	D	1	0	0	5
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5	DCR _r	Decrement register	0	0	D	D	D	1	0	1	5
LXI _{SP}	Load immediate stack pointer	0	0	1	1	0	0	0	1	10	INR _M	Increment memory	0	0	1	1	0	1	0	0	10
INX _{SP}	Increment stack pointer	0	0	1	1	0	0	1	1	5	DCR _M	Decrement memory	0	0	1	1	0	1	0	1	10
DCX _{SP}	Decrement stack pointer	0	0	1	1	1	0	1	1	5	INX _B	Increment B & C registers	0	0	0	0	0	0	1	1	5
JUMP																					
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10	INX _D	Increment D & E registers	0	0	0	1	0	0	1	1	5
JC	Jump on carry	1	1	0	1	1	0	1	0	10	INX _H	Increment H & L registers	0	0	1	0	0	0	1	1	5
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10	DCX _B	Decrement B & C	0	0	0	0	1	0	1	1	5
JZ	Jump on zero	1	1	0	0	1	0	1	0	10	DCX _D	Decrement D & E	0	0	0	1	1	0	1	1	5
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10	DCX _H	Decrement H & L	0	0	1	0	1	0	1	1	5
JP	Jump on positive	1	1	1	1	0	0	1	0	10	ADD										
JM	Jump on minus	1	1	1	1	1	0	1	0	10	ADD _r	Add register to A	1	0	0	0	0	S	S	S	4
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10	ADC _r	Add register to A with carry	1	0	0	0	1	S	S	S	4
											ADD _M	Add memory to A	1	0	0	0	0	1	1	0	7
											ADC _M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
											ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
											ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
											DAD _B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
											DAD _D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
											DAD _H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
											DAD _{SP}	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10

NOTES 1 DDD or SSS B 000. C 001. D 010. E 011. H 100. L 101. Memory 110. A 111

2 Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags

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Summary of Processor Instructions (Cont.)

Mnemonic	Description	Instruction Code[1]								Clock[2] Cycles
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	7

NOTES 1 DDD or SSS B=000. C=001 D=010 E=011 H=100 L=101 Memory=110 A=111
 2 Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags

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8224 CLOCK GENERATOR AND DRIVER FOR 8080A CPU

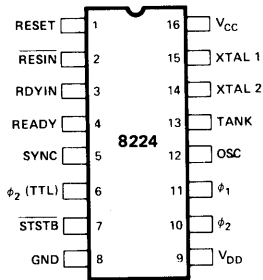
- Single Chip Clock Generator/Driver for 8080A CPU
- Power-Up Reset for CPU
- Ready Synchronizing Flip-Flop
- Advanced Status Strobe
- Oscillator Output for External System Timing
- Crystal Controlled for Stable System Operation
- Reduces System Package Count

The Intel® 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

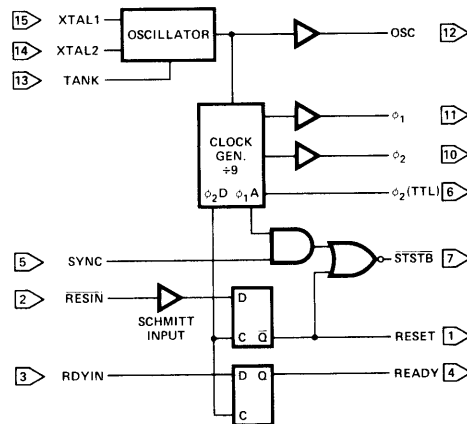
Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
phi_1	8080
phi_2	CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
phi_2 (TTL)	phi_2 CLK (TTL LEVEL)
V _{CC}	+5V
V _{DD}	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to 150°C
Supply Voltage, V _{CC}	-0.5V to +7V
Supply Voltage, V _{DD}	-0.5V to +13.5V
Input Voltage	-1.5V to +7V
Output Current	100mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _F	Input Current Loading			-.25	mA	V _F = .45V
I _R	Input Leakage Current			10	μA	V _R = 5.25V
V _C	Input Forward Clamp Voltage			1.0	V	I _C = -5mA
V _{IL}	Input "Low" Voltage			.8	V	V _{CC} = 5.0V
V _{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
V _{IH} -V _{IL}	RESIN Input Hysteresis	.25			V	V _{CC} = 5.0V
V _{OL}	Output "Low" Voltage			.45	V	(φ ₁ , φ ₂), Ready, Reset, STSTB I _{OL} = 2.5mA All Other Outputs I _{OL} = 15mA
				.45	V	
V _{OH}	Output "High" Voltage				V	I _{OH} = -100μA I _{OH} = -100μA I _{OH} = -1mA
	φ ₁ , φ ₂	9.4			V	
	READY, RESET All Other Outputs	3.6 2.4			V	
I _{SC} ^[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V _O = 0V V _{CC} = 5.0V
I _{CC}	Power Supply Current			115	mA	
I _{DD}	Power Supply Current			12	mA	

Note: 1. Caution, φ₁ and φ₂ output drivers do not have short circuit protection

Crystal Requirements

Tolerance: 0.005% at 0°C-70°C

Resonance: Series (Fundamental)*

Load Capacitance: 20-35 pF

Equivalent Resistance: 75-20 ohms

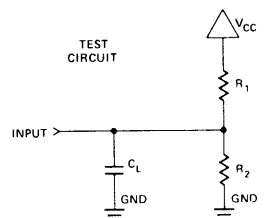
Power Dissipation (Min): 4 mW

*With tank circuit use 3rd overtone mode.

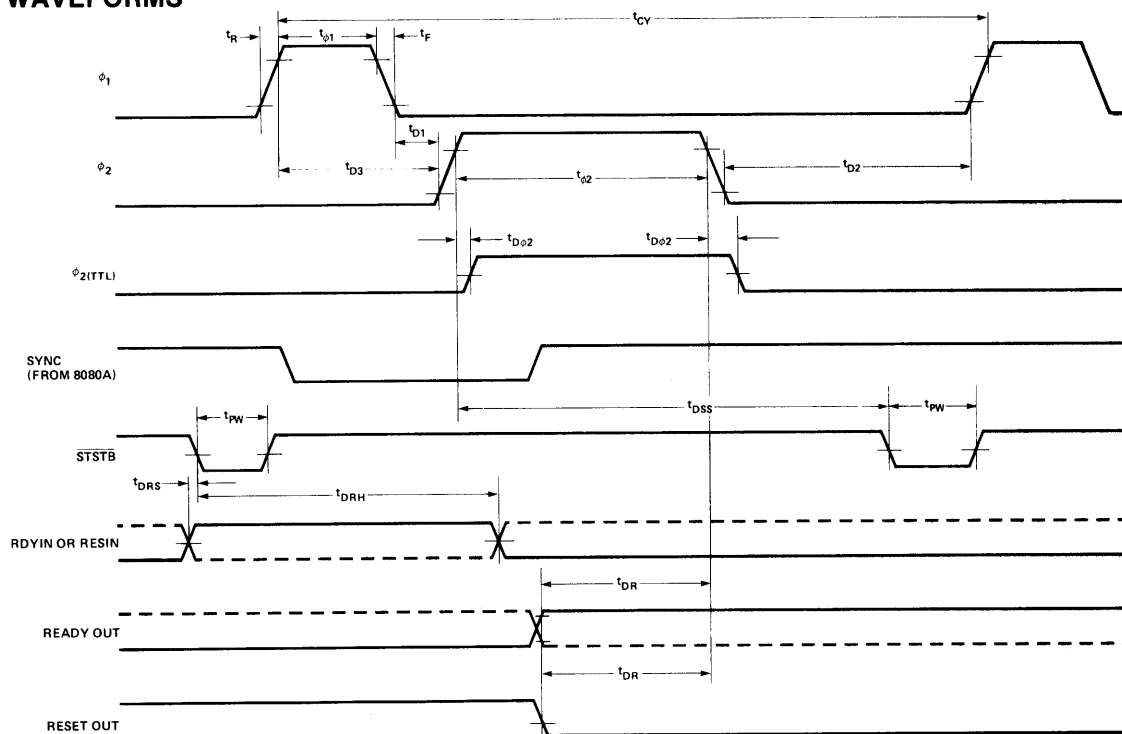
A.C. CHARACTERISTICS

 $V_{CC} = +5.0V \pm 5\%$; $V_{DD} = +12.0V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9} - 20ns$			ns	$C_L = 20pF$ to $50pF$
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9} - 35ns$				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9} - 14ns$				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9} + 20ns$		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2 TTL, $C_L=30$ $R_1=300\Omega$ $R_2=600\Omega$
t_{DSS}	ϕ_2 to \overline{STSTB} Delay	$\frac{6tcy}{9} - 30ns$		$\frac{6tcy}{9}$		\overline{STSTB} , $C_L=15pF$ $R_1 = 2K$ $R_2 = 4K$
t_{PW}	\overline{STSTB} Pulse Width	$\frac{tcy}{9} - 15ns$				
t_{DRS}	RDYIN Setup Time to Status Strobe	$50ns - \frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After \overline{STSTB}	$\frac{4tcy}{9}$				Ready & Reset $C_L=10pF$ $R_1=2K$ $R_2=4K$
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\frac{4tcy}{9} - 25ns$				
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency			27	MHz	
C_{in}	Input Capacitance			8	pF	$V_{CC}=+5.0V$ $V_{DD}=+12V$ $V_{BIAS}=2.5V$ $f=1MHz$



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

EXAMPLE:

A.C. CHARACTERISTICS (For $t_{CV} = 488.28 \text{ ns}$)

$T_A = 0^\circ\text{C}$ to 70°C ; $V_{DD} = +5V \pm 5\%$; $V_{DD} = +12V \pm 5\%$.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	$t_{CV} = 488.28 \text{ ns}$ ϕ_1 & ϕ_2 Loaded to $C_L = 20$ to 50 pF
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{\text{STSTB}}$ Delay	296		326	ns	Ready & Reset Loaded to $2 \text{ mA}/10 \text{ pF}$ All measurements referenced to 1.5V unless specified otherwise.
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	
t_{DRS}	RDYIN Setup Time to $\overline{\text{STSTB}}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{\text{STSTB}}$	217			ns	
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	



8228/8238

SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- Single Chip System Control for MCS-80™ Systems
- Built-In Bidirectional Bus Driver for Data Bus Isolation
- Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge
- User Selected Single Level Interrupt Vector (RST 7)
- 28-Pin Dual In-Line Package
- Reduces System Package Count
- *8238 Has Advanced IOW/MEMW for Large System Timing Control

The Intel® 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

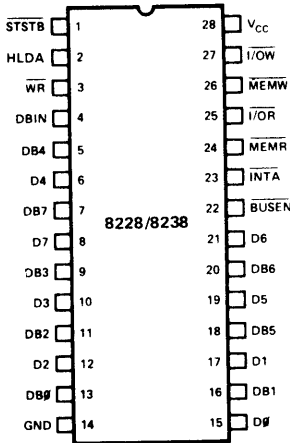
A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

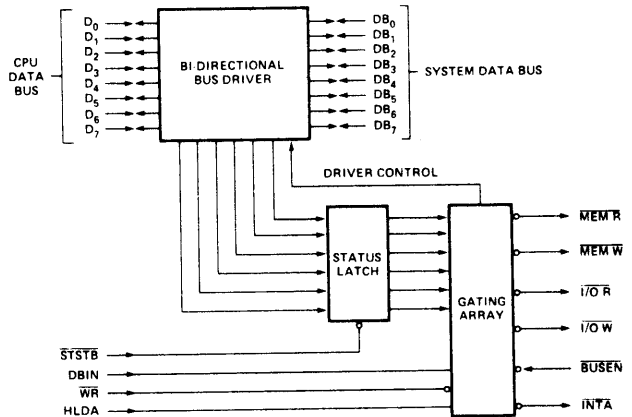
The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable design of the MCS-80 systems.

Note: The specifications for the 3228/3238 are identical with those for the 8228/8238

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D7: D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7: DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/O R	I/O READ	WR	WR (FROM 8080)
I/O W	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	Vcc	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias.....	-0°C to 70°C
Storage Temperature.....	-65°C to 150°C
Supply Voltage, V _{CC}	-0.5V to +7V
Input Voltage.....	-1.5V to +7V
Output Current.....	100 mA

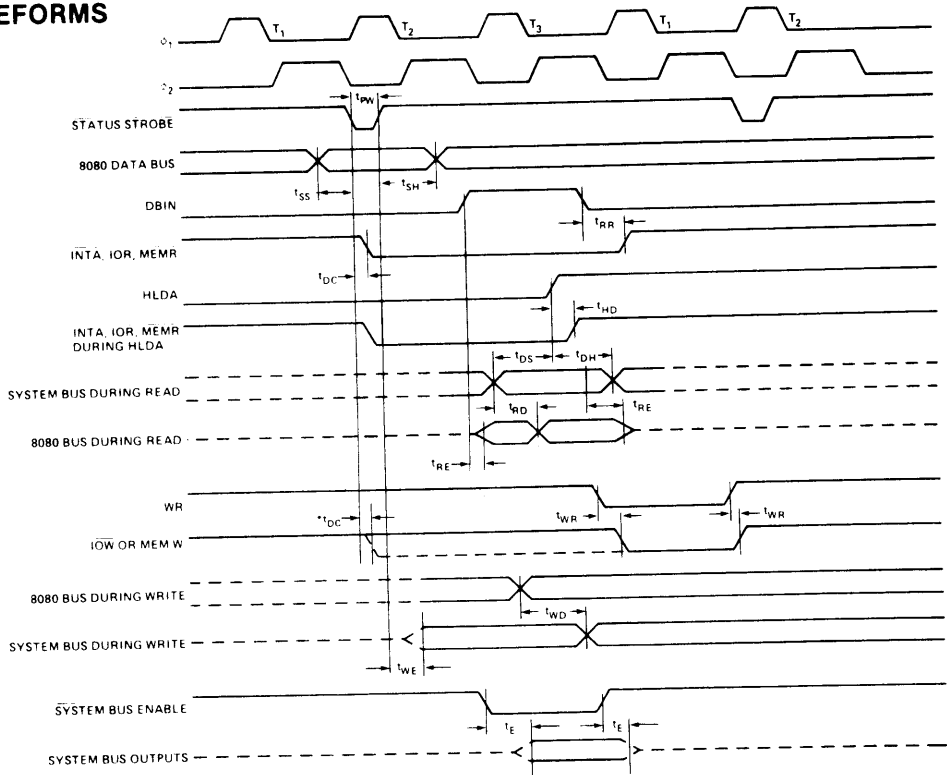
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = 5V ±5%.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ. [1]	Max.		
V _C	Input Clamp Voltage, All Inputs		.75	-1.0	V	V _{CC} =4.75V; I _C =-5mA
I _F	Input Load Current, STSTB			500	μA	V _{CC} = 5.25V V _F = 0.45V
	D ₂ & D ₆			750	μA	
	D ₀ , D ₁ , D ₄ , D ₅ , & D ₇			250	μA	
	All Other Inputs			250	μA	
I _R	Input Leakage Current STSTB			100	μA	V _{CC} = 5.25V V _R = 5.25V
	DB ₀ -DB ₇			20	μA	
	All Other Inputs			100	μA	
V _{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V _{CC} = 5V
I _{CC}	Power Supply Current		140	190	mA	V _{CC} = 5.25V
V _{OL}	Output Low Voltage, D ₀ -D ₇			.45	V	V _{CC} = 4.75V; I _{OL} = 2mA
	All Other Outputs			.45	V	
V _{OH}	Output High Voltage, D ₀ -D ₇	3.6	3.8		V	V _{CC} = 4.75V; I _{OH} = -10μA
	All Other Outputs	2.4			V	
I _{OS}	Short Circuit Current, All Outputs	15		90	mA	V _{CC} = 5V
I _{O(off)}	Off State Output Current, All Control Outputs			100	μA	V _{CC} = 5.25V; V _O = 5.25
				-100	μA	
I _{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0 - D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*ADVANCED $\overline{IOW}/\overline{MEMW}$ FOR 8238 ONLY.

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{pw}	Width of Status Strobe	22		ns	
t_{ss}	Setup Time, Status Inputs D_0 - D_7	8		ns	
t_{sh}	Hold Time, Status Inputs D_0 - D_7	5		ns	
t_{DC}	Delay from \overline{STSTB} to any Control Signal	20	60	ns	$C_L = 100\text{pF}$
t_{RR}	Delay from \overline{DBIN} to Control Outputs		30	ns	$C_L = 100\text{pF}$
t_{RE}	Delay from \overline{DBIN} to Enable/Disable 8080 Bus		45	ns	$C_L = 25\text{pF}$
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	$C_L = 25\text{pF}$
t_{WR}	Delay from \overline{WR} to Control Outputs	5	45	ns	$C_L = 100\text{pF}$
t_{WE}	Delay to Enable System Bus $\overline{DB_0-DB_7}$ after \overline{STSTB}		30	ns	$C_L = 100\text{pF}$
t_{WD}	Delay from 8080 Bus D_0 - D_7 to System Bus $\overline{DB_0-DB_7}$ during Write	5	40	ns	$C_L = 100\text{pF}$
t_E	Delay from System Bus Enable to System Bus $\overline{DB_0-DB_7}$		30	ns	$C_L = 100\text{pF}$
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	$C_L = 100\text{pF}$

CAPACITANCE

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
C _{IN}	Input Capacitance		8	12	pF
C _{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

Test Conditions: NS: V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1MHz.

Note 2: For D₀-D₇: R₁ = 4KΩ, R₂ = ∞Ω,
C_L = 25pF. For all other outputs:
R₁ = 500Ω, R₂ = 1KΩ, C_L = 100pF.

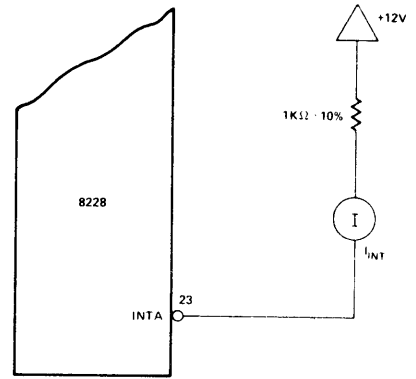
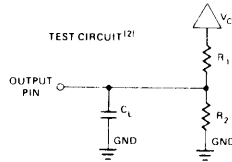


Figure 1. INTA Test Circuit (for RST 7)

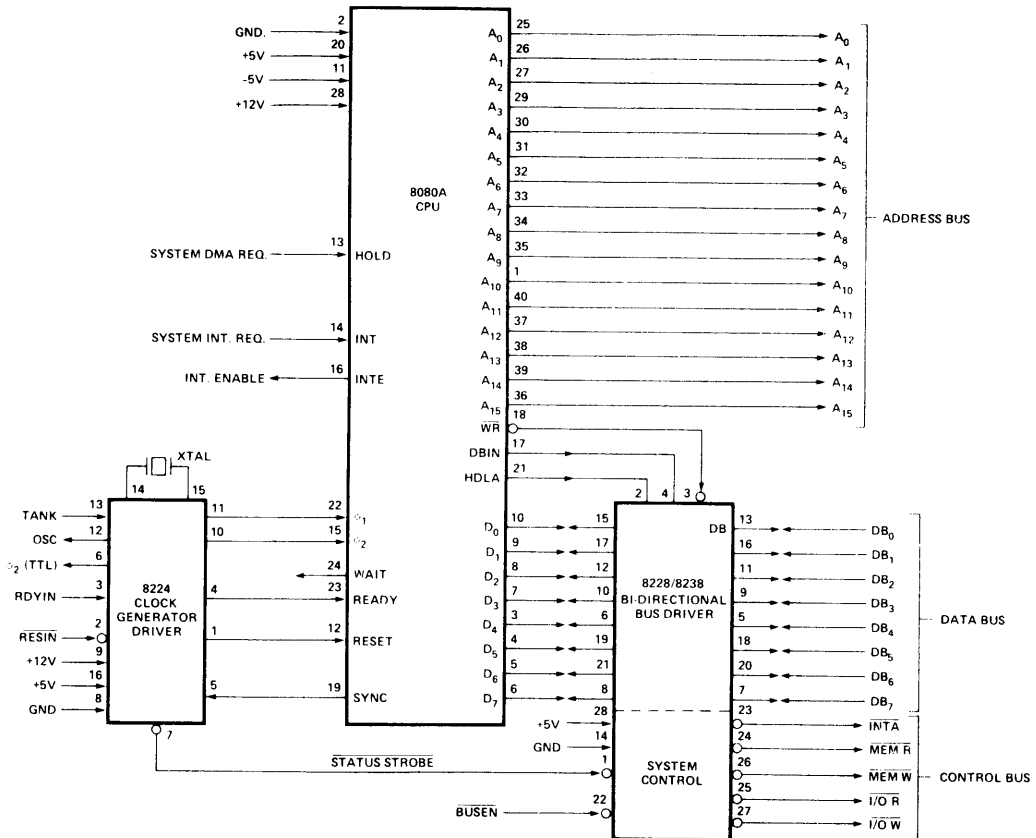


Figure 2. CPU Standard Interface

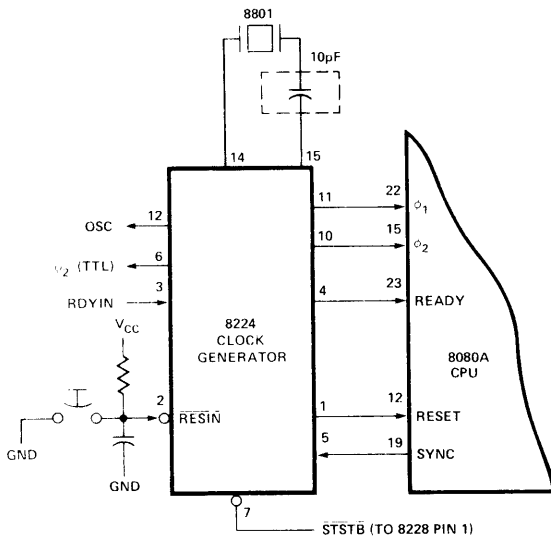


8801 CLOCK GENERATOR CRYSTAL FOR 8224/8080A

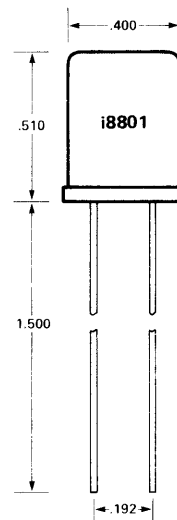
- Specifically Selected for Intel® 8224
- 18.432 MHz for 1.95 μ s 8080A Cycle
- Simple Generation of all Standard Communication Baud Rates
- Frequency Deviation $\pm 0.005\%$
- Fundamental Frequency Mode
- 0°C to 70°C Operating Temperature

The Intel® 8801 is a quartz crystal specifically selected to operate with the 8224 clock generator and the 8080A CPU. It resonates in the fundamental frequency mode at 18.432 MHz. This frequency allows the 8080A at full speed ($T_{CY} = 488$ ns) to have a cycle of 1.95 μ s and also simplifies the generation of all standard communication baud rates. The 8801 crystal is exactly matched to the requirements of the 8080A/8224 and provides both high performance and system flexibility for the microcomputer designer.

8801 INTERFACE



PACKAGING INFORMATION



APPLICATIONS

The selection of 18.432 MHz provides the 8080A with clocks whose period is 488ns. This allows the 8080A to operate at very close to its maximum specified speed (480 ns). The 8224, when used with the 8801, outputs a signal on its OSC pin that is an approximately symmetrical square wave at a frequency of 18.432 MHz. This frequency signal can be easily divided down to generate an accurate, stable baud rate clock that can be connected directly to the transmitter or receiver clocks of the 8251 USART. This feature allows the designer to support most standard communication interfaces with a minimum of extra hardware.

The chart below (Fig. 1) shows the equivalent baud rates that are generated with the corresponding dividers.

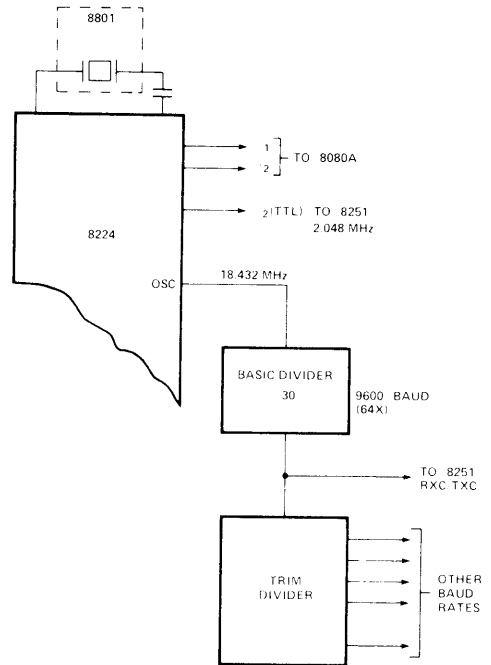


Figure 1. Block Diagram

BAUD RATE 64x	BAUD RATE 16x	FREQUENCY	BASIC DIVIDER	PLUS TRIM DIVIDER
9600		614.4 KH	÷30	—
4800	19.2K	307.2 KH	÷30	÷2
2400	9600	153.6 KH	÷30	÷4
1200	4800	76.8 KH	÷30	÷8
600	2400	38.4 KH	÷30	÷16
300	1200	19.2 KH	÷30	÷32
	600	9.6 KH	÷30	÷64
	300	4.8 KH	÷30	÷128
*109.1		6.982 KH	÷30	÷88

*For 109.1 (64x) Baud rate divide 1200 Baud Frequency (76.8 KH) by 11.

Figure 2. Baud Rate Chart

ELECTRICAL CHARACTERISTICS

Recommended Drive Level	5mW
Type of Resonance	Series
Equivalent Resistance	20 ohms
Maximum Shunt Capacity	7pF
Maximum Frequency Deviation	
0° — 70°C	±.005%
-55° — 125°C	±.002%

