

Chapter 6

MCS-85™

MCS-80™

Systems
Support
Components

Peripherals

Static RAMs

ROMs–EPROMs

MOS

8085

MOS

8085



8085A/8085A-2

SINGLE CHIP 8-BIT N-CANNEL MICROPROCESSORS

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μ s Instruction Cycle (8085A); 0.8 μ s (8085A-2)**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64k Bytes of Memory**

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

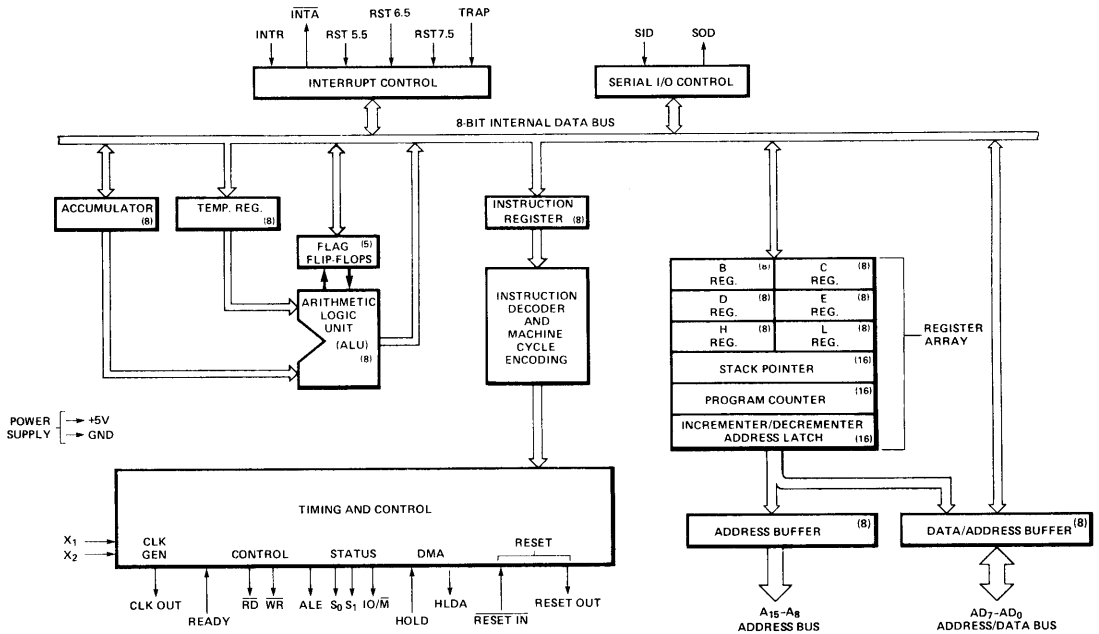


Figure 1. 8085A CPU Functional Block Diagram

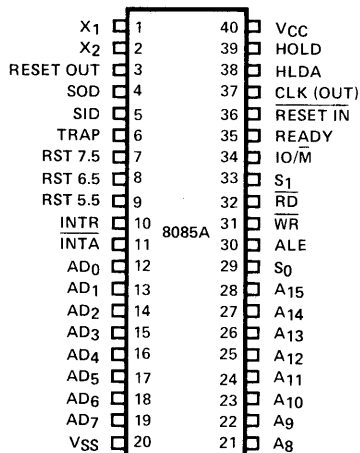


Figure 2. 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

<u>Symbol</u>	<u>Function</u>																																								
A₈-A₁₅ (Output, 3-state)	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.																																								
AD₀₋₇ (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.																																								
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.																																								
S₀, S₁, and IO/M (Output)	Machine cycle status: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>IO/M</th> <th>S₁</th> <th>S₀</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Memory write</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Memory read</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>I/O write</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>I/O read</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Opcode fetch</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Interrupt Acknowledge</td> </tr> <tr> <td>*</td> <td>0</td> <td>0</td> <td>Halt</td> </tr> <tr> <td>*</td> <td>X</td> <td>X</td> <td>Hold</td> </tr> <tr> <td>*</td> <td>X</td> <td>X</td> <td>Reset</td> </tr> </tbody> </table> <p>* = 3-state (high impedance) X = unspecified</p>	IO/M	S ₁	S ₀	Status	0	0	1	Memory write	0	1	0	Memory read	1	0	1	I/O write	1	1	0	I/O read	0	1	1	Opcode fetch	1	1	1	Interrupt Acknowledge	*	0	0	Halt	*	X	X	Hold	*	X	X	Reset
IO/M	S ₁	S ₀	Status																																						
0	0	1	Memory write																																						
0	1	0	Memory read																																						
1	0	1	I/O write																																						
1	1	0	I/O read																																						
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*	0	0	Halt																																						
*	X	X	Hold																																						
*	X	X	Reset																																						

<u>Symbol</u>	<u>Function</u>
S₁	S ₁ can be used as an advanced R/W status. IO/M, S ₀ and S ₁ become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
RD (Output, 3-state)	READ control: A low level on RD indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
WR (Output, 3-state)	WRITE control: A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

8085A FUNCTIONAL PIN DESCRIPTION (Continued)

<u>Symbol</u>	<u>Function</u>	<u>Symbol</u>	<u>Function</u>
INTA (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) \overline{RD} during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.		Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as RESET \overline{IN} is applied.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.	RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)	X₁, X₂ (Input)	X ₁ and X ₂ are connected to a crystal, LC, or RC network to drive the internal clock generator. X ₁ can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
RESET IN (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET \overline{IN} is a	CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X ₁ , X ₂ input period.
		SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
		SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
		V_{CC}	+5 volt supply.
		V_{SS}	Ground Reference.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

- (1) The processor pushes the PC on the stack before branching to the indicated address.
- (2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

FUNCTIONAL DESCRIPTION

The 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085A) or 5 MHz (8085A-2), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

The 8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085A provides \overline{RD} , \overline{WR} , S_0 , S_1 , and $\overline{IO/\overline{M}}$ signals for bus control. An Interrupt Acknowledge signal (\overline{INTA}) is also provided. HOLD and all interrupts are synchronized with the processor's internal clock. The 8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The 8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive*.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. (See Section 5.2.7.) The RST 7.5 request flip-flop remains

set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN. (See SIM, Chapter 5.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP — highest priority, RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive*. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the 8085A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

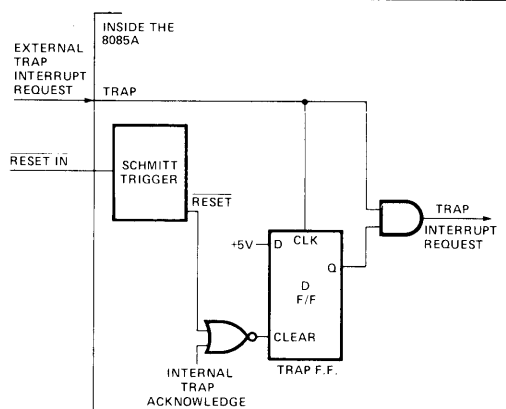


Figure 3. TRAP and RESET IN Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled. See the description of the RIM instruction in Chapter 5.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X₁ AND X₂ INPUTS

You may drive the clock inputs of the 8085A or 8085A-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085A is operated with a 6 MHz crystal (for 3 MHz clock), and the 8085A-2 can be operated with a 10 MHz crystal (for 5 MHz clock). If a crystal is used, it must have the following characteristics:

- Parallel resonance at twice the clock frequency desired
- C_L (load capacitance) ≤ 30 pf
- C_S (shunt capacitance) ≤ 7 pf
- R_S (equivalent shunt resistance) ≤ 75 Ohms
- Drive level: 10 mW
- Frequency tolerance: ±.005% (suggested)

Note the use of the 20pF capacitor between X₂ and ground. This capacitor is required with crystal frequencies below 4MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085A, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

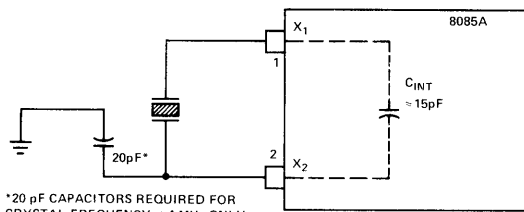
$$f = \frac{1}{2\pi\sqrt{L(C_{EXT} + C_{INT})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5MHz.

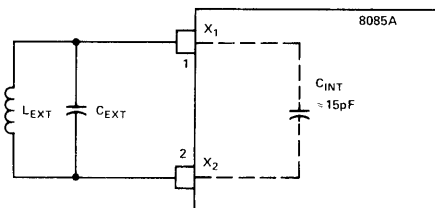
An RC circuit may be used as the frequency-determining network for the 8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 4 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4 V.

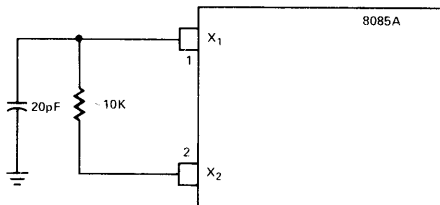
For driving frequencies up to and including 6 MHz you may supply the driving signal to X₁ and leave X₂ open-circuited (Figure 4D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X₁ and X₂ with a push-pull source (Figure 4E). To prevent self-oscillation of the 8085A, be sure that X₂ is not coupled back to X₁ through the driving circuit.



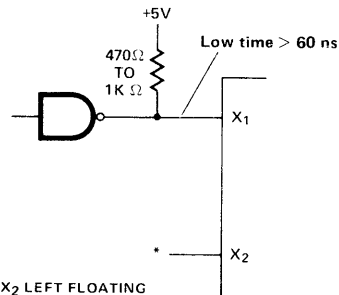
A. Quartz Crystal Clock Driver



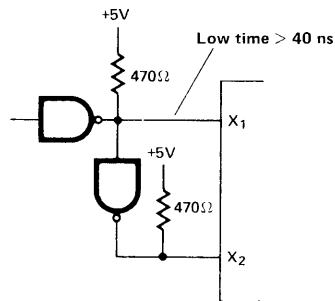
B. LC Tuned Circuit Clock Driver



C. RC Circuit Clock Driver



D. 1-6 MHz Input Frequency External Clock Driver Circuit



E. 1-10 MHz Input Frequency External Clock Driver Circuit

Figure 4. Clock Driver Circuits

GENERATING AN 8085A WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 5 may be used to insert one WAIT state in each 8085A machine cycle

The D flip-flops should be chosen so that

- CLK is rising edge-triggered
- CLEAR is low-level active.

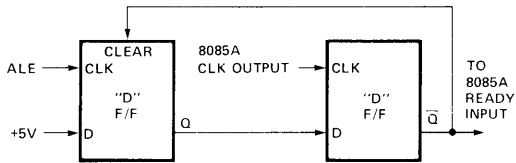


Figure 5. Generation of a Wait State for 8085A CPU

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085A can be used with slow memory. HOLD causes the cpu to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

The 8085A family includes memory components, which are directly compatible to the 8085A cpu. For example, a system consisting of the three chips, 8085A, 8156, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serrial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 6.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 7 shows the system configuration of Memory Mapped I/O using 8085A.

The 8085A cpu can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 8.

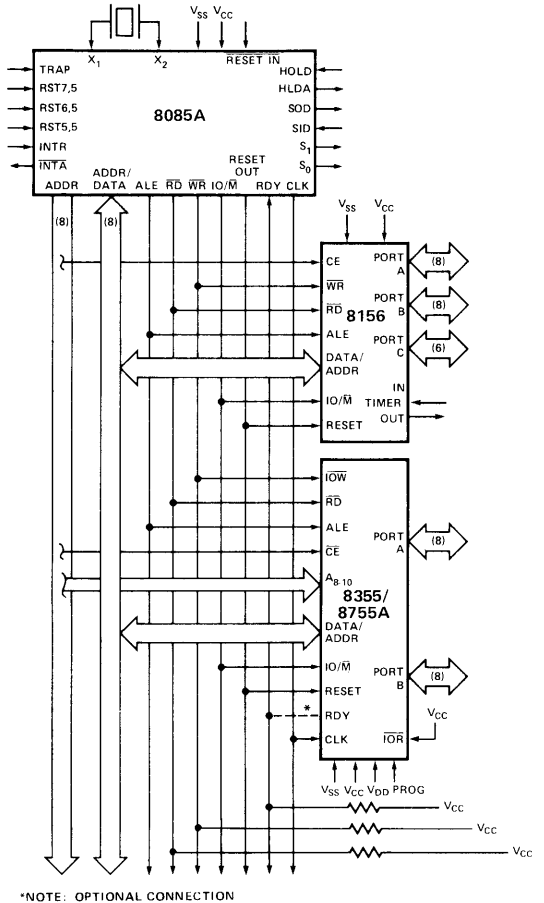


Figure 6. 8085A Minimum System (Standard I/O Technique)

BASIC SYSTEM TIMING

The 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($\overline{IO/\overline{M}}$, S_1 , S_0) and the three control signals (\overline{RD} , \overline{WR} , and \overline{INTA}). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines \overline{RD} and \overline{WR} become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

TABLE 2. 8085A MACHINE CYCLE CHART

MACHINE CYCLE	STATUS			CONTROL		
	$\overline{IO/\overline{M}}$	S_1	S_0	\overline{RD}	\overline{WR}	\overline{INTA}
OPCODE FETCH (OF)	0	1	1	0	1	1
MEMORY READ (MR)	0	1	0	0	1	1
MEMORY WRITE (MW)	0	0	1	1	0	1
I/O READ (IOR)	1	1	0	0	1	1
I/O WRITE (IOW)	1	0	1	1	0	1
ACKNOWLEDGE OF INTR (INA)	1	1	1	1	1	0
BUS IDLE (BI): DAD	0	1	0	1	1	1
ACK. OF RST, TRAP	1	1	1	1	1	1
HALT	TS	0	0	TS	TS	1

TABLE 3. 8085A MACHINE STATE CHART

Machine State	Status & Buses					Control		
	S_1, S_0	$\overline{IO/\overline{M}}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}, \overline{WR}$	\overline{INTA}	ALE	
T_1	X	X	X	X	1	1	1*	
T_2	X	X	X	X	X	X	0	
T_{WAIT}	X	X	X	X	X	X	0	
T_3	X	X	X	X	X	X	0	
T_4	1	0†	X	TS	1	1	0	
T_5	1	0†	X	TS	1	1	0	
T_6	1	0†	X	TS	1	1	0	
T_{RESET}	X	TS	TS	TS	TS	1	0	
T_{HALT}	0	TS	TS	TS	TS	1	0	
T_{HOLD}	X	TS	TS	TS	TS	1	0	

0 = Logic "0" TS = High Impedance
 1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
 † $\overline{IO/\overline{M}} = 1$ during $T_4 - T_6$ of INA machine cycle.

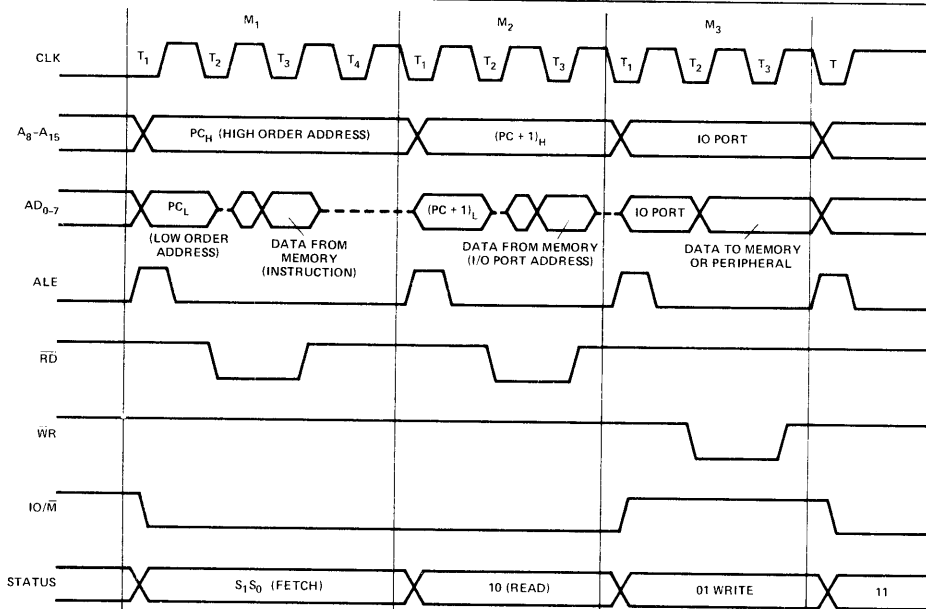


Figure 9. 8085A Basic System Timing

TABLE 4. ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 5. D.C. CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5\text{V} \pm 5\%$; $V_{SS} = 0\text{V}$; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2\text{mA}$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\mu\text{A}$
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		± 10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		± 10	μA	$0.45\text{V} \leq V_{out} \leq V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	$V_{CC} + 0.5$	V	
V_{HY}	Hysteresis, RESET	0.25		V	

TABLE 6. A.C. CHARACTERISTICS
 $T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5\text{V} \pm 5\%$; $V_{SS} = 0\text{V}$

Symbol	Parameter	8085A ^[2]		8085A-2 ^[2] (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80		40		ns
t_2	CLK High Time (Standard CLK Loading)	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	30	120	30	100	ns
t_{XKF}	X_1 Rising to CLK Falling	30	150	30	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control ^[1]	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float After Leading Edge of $\overline{\text{READ}}$ ($\overline{\text{INTA}}$)		0		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of $\overline{\text{ALE}}$ ^[1]	115		50		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of $\overline{\text{ALE}}$	90		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		60		ns
t_{CC}	Width of Control Low ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{INTA}}$)					
	Edge of $\overline{\text{ALE}}$	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of $\overline{\text{ALE}}$	50		25		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{\text{WRITE}}$	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float After HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time After $\overline{\text{ALE}}$	100		50		ns
t_{LC}	Trailing Edge of $\overline{\text{ALE}}$ to Leading Edge of Control	130		60		ns
t_{LCK}	$\overline{\text{ALE}}$ Low During CLK High	100		50		ns
t_{LDR}	$\overline{\text{ALE}}$ to Valid Data During Read		460		270	ns
t_{LDW}	$\overline{\text{ALE}}$ to Valid Data During Write		200		120	ns
t_{LL}	$\overline{\text{ALE}}$ Width	140		80		ns
t_{LRY}	$\overline{\text{ALE}}$ to READY Stable		110		30	ns

Table 6. A.C. Characteristics (Cont.)

Symbol	Parameter	8085A ^[2]		8085A-2 ^[2] (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t _{RAE}	Trailing Edge of $\overline{\text{READ}}$ to Re-Enabling of Address	150		90		ns
t _{RD}	$\overline{\text{READ}}$ (or $\overline{\text{INTA}}$) to Valid Data		300		150	ns
t _{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t _{RDH}	Data Hold Time After $\overline{\text{READ}}$ $\overline{\text{INTA}}$ ^[7]	0		0		ns
t _{RYH}	READY Hold Time	0		0		ns
t _{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t _{WD}	Data Valid After Trailing Edge of $\overline{\text{WRITE}}$	100		60		ns
t _{WDL}	LEADING Edge of WRITE to Data Valid		40		20	ns

Notes:

- A₈-A₁₅ address Specs apply to IO/M, S₀, and S₁ except A₈-A₁₅ are undefined during T₄-T₆ of OF cycle whereas IO/M, S₀, and S₁ are stable.
- Test conditions: t_{CYC} = 320 ns (8085A)/200 ns (8085A-2); C_L = 150 pF.
- For all output timing where C_L = 150 pF use the following correction factors:
25 pF ≤ C_L < 150 pF: -0.10 ns/pF
150 pF < C_L ≤ 300 pF: +0.30 ns/pF
- Output timings are measured with purely capacitive load.
- All timings are measured at output voltage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20 ns rise and fall time on inputs.
- To calculate timing specifications at other values of t_{CYC} use Table 7.
- Data hold time is guaranteed under all loading conditions.

Input Waveform for A.C. Tests:

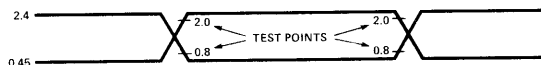


TABLE 7. BUS TIMING SPECIFICATION AS A T_{CYC} DEPENDENT

8085A				8085A-2 (Preliminary)			
t_{AL}	—	$(1/2) T - 45$	MIN	t_{AL}	—	$(1/2) T - 50$	MIN
t_{LA}	—	$(1/2) T - 60$	MIN	t_{LA}	—	$(1/2) T - 50$	MIN
t_{LL}	—	$(1/2) T - 20$	MIN	t_{LL}	—	$(1/2) T - 20$	MIN
t_{LCK}	—	$(1/2) T - 60$	MIN	t_{LCK}	—	$(1/2) T - 50$	MIN
t_{LC}	—	$(1/2) T - 30$	MIN	t_{LC}	—	$(1/2) T - 40$	MIN
t_{AD}	—	$(5/2 + N) T - 225$	MAX	t_{AD}	—	$(5/2 + N) T - 150$	MAX
t_{RD}	—	$(3/2 + N) T - 180$	MAX	t_{RD}	—	$(3/2 + N) T - 150$	MAX
t_{RAE}	—	$(1/2) T - 10$	MIN	t_{RAE}	—	$(1/2) T - 10$	MIN
t_{CA}	—	$(1/2) T - 40$	MIN	t_{CA}	—	$(1/2) T - 40$	MIN
t_{DW}	—	$(3/2 + N) T - 60$	MIN	t_{DW}	—	$(3/2 + N) T - 70$	MIN
t_{WD}	—	$(1/2) T - 60$	MIN	t_{WD}	—	$(1/2) T - 40$	MIN
t_{CC}	—	$(3/2 + N) T - 80$	MIN	t_{CC}	—	$(3/2 + N) T - 70$	MIN
t_{CL}	—	$(1/2) T - 110$	MIN	t_{CL}	—	$(1/2) T - 75$	MIN
t_{ARY}	—	$(3/2) T - 260$	MAX	t_{ARY}	—	$(3/2) T - 200$	MAX
t_{HACK}	—	$(1/2) T - 50$	MIN	t_{HACK}	—	$(1/2) T - 60$	MIN
t_{HABF}	—	$(1/2) T + 50$	MAX	t_{HABF}	—	$(1/2) T + 50$	MAX
t_{HABE}	—	$(1/2) T + 50$	MAX	t_{HABE}	—	$(1/2) T + 50$	MAX
t_{AC}	—	$(2/2) T - 50$	MIN	t_{AC}	—	$(2/2) T - 85$	MIN
t_1	—	$(1/2) T - 80$	MIN	t_1	—	$(1/2) T - 60$	MIN
t_2	—	$(1/2) T - 40$	MIN	t_2	—	$(1/2) T - 30$	MIN
t_{RV}	—	$(3/2) T - 80$	MIN	t_{RV}	—	$(3/2) T - 80$	MIN
t_{LDR}	—	$(4/2) T - 180$	MAX	t_{LDR}	—	$(4/2) T - 130$	MAX

NOTE: N is equal to the total WAIT states.
 $T = t_{CYC}$.

NOTE: N is equal to the total WAIT states.
 $T = t_{CYC}$.

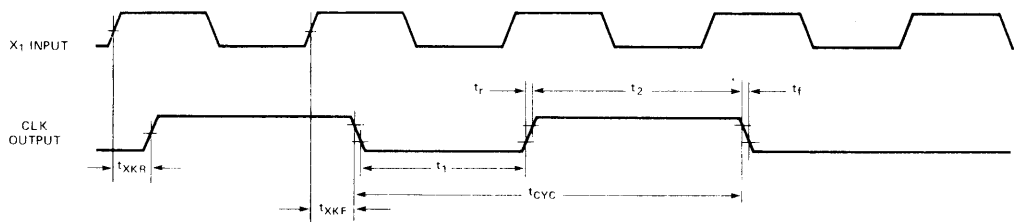
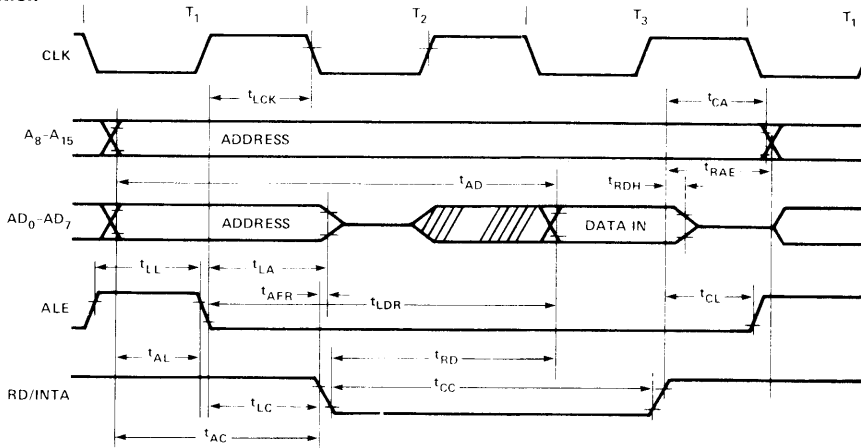
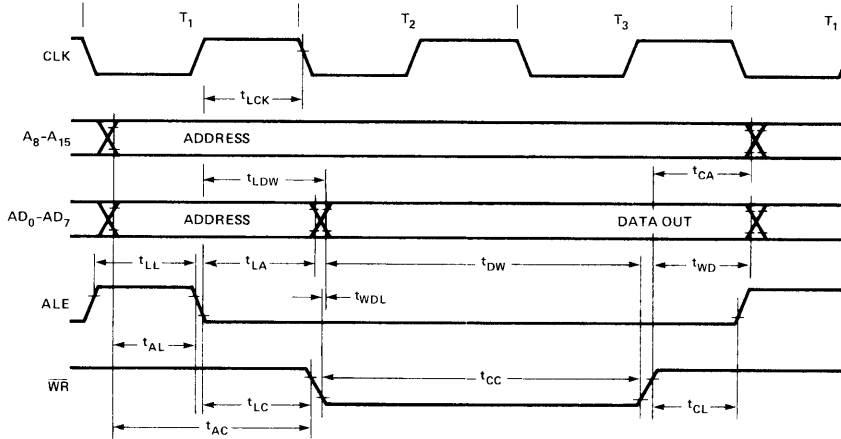


Figure 10. Clock Timing Waveform

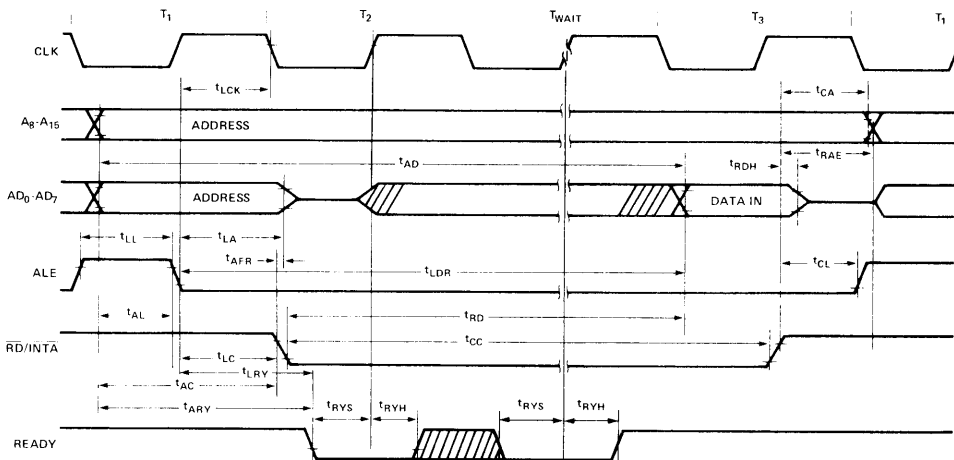
Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.



NOTE 1: READY MUST REMAIN STABLE DURING SETUP AND HOLD TIMES.

Figure 11. 8085A Bus Timing, With and Without Wait

Hold Operation

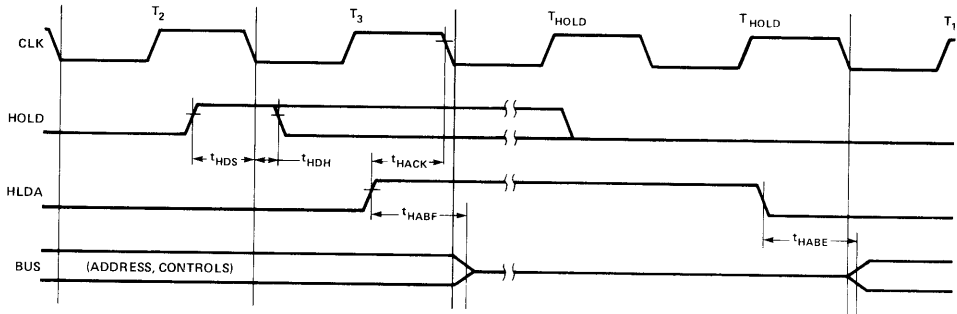


Figure 12. 8085A Hold Timing.

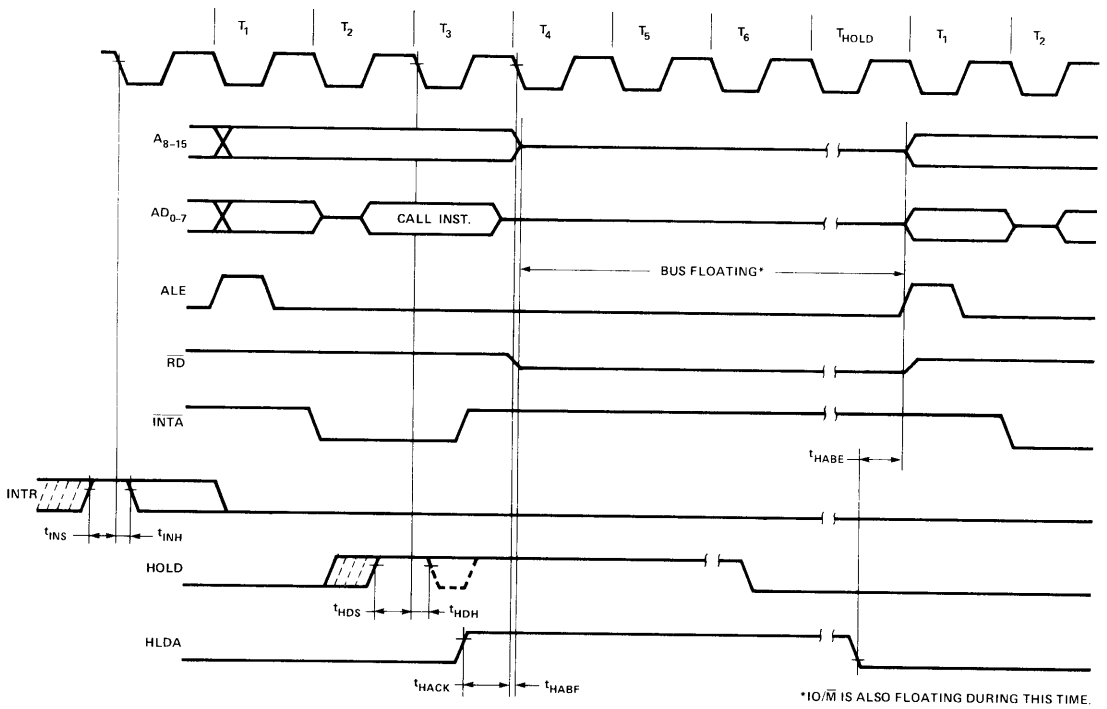


Figure 13. 8085A Interrupt and Hold Timing

8085A INSTRUCTION SET SUMMARY BY FUNCTIONAL GROUPING

Table 6-1

Mnemonic	Description	Instruction Code (1)								Page	Mnemonic	Description	Instruction Code (1)								Page
		D7	D6	D5	D4	D3	D2	D1	D0				D7	D6	D5	D4	D3	D2	D1	D0	
MOVE, LOAD, AND STORE																					
MOV r1 r2	Move register to register	0	1	0	0	0	S	S	S	5-4	CZ	Call on zero	1	1	0	0	1	1	0	0	5-14
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	5-4	CNZ	Call on no zero	1	1	0	0	0	1	0	0	5-14
MOV r,M	Move memory to register	0	1	0	0	0	1	1	0	5-4	CP	Call on positive	1	1	1	1	0	1	0	0	5-14
MVI r	Move immediate register	0	0	0	0	0	1	1	0	5-4	CM	Call on minus	1	1	1	1	1	1	0	0	5-14
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	5-4	CPE	Call on parity even	1	1	1	0	1	1	0	0	5-14
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	5-5	CPO	Call on parity odd	1	1	1	0	0	1	0	0	5-14
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	5-5	RETURN										
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	5-5	RET	Return	1	1	0	0	1	0	0	1	5-14
STAX B	Store A indirect	0	0	0	0	0	0	1	0	5-6	RC	Return on carry	1	1	0	1	1	0	0	0	5-14
STAX D	Store A indirect	0	0	0	1	0	0	1	0	5-6	RNC	Return on no carry	1	1	0	1	0	0	0	0	5-14
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	5-5	RZ	Return on zero	1	1	0	0	1	0	0	0	5-14
LDAX D	Load A indirect	0	0	0	1	0	1	0	1	5-5	RNZ	Return on no zero	1	1	0	0	0	0	0	0	5-14
STA	Store A direct	0	0	1	1	0	0	1	0	5-5	RP	Return on positive	1	1	1	1	0	0	0	0	5-14
LDA	Load A direct	0	0	1	1	1	0	1	0	5-5	RM	Return on minus	1	1	1	1	1	0	0	0	5-14
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	5-5	RPE	Return on parity even	1	1	1	0	1	0	0	0	5-14
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	5-5	RPO	Return on parity odd	1	1	1	0	0	0	0	0	5-14
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	5-6	RESTART										
STACK OPS																					
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	5-15	RST	Restart	1	1	A	A	A	1	1	1	5-14
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	5-15	INPUT/OUTPUT										
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	5-15	IN	Input	1	1	0	1	1	0	1	1	5-16
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	5-15	OUT	Output	1	1	0	1	0	0	1	1	5-16
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	5-15	INCREMENT AND DECREMENT										
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	5-15	INR r	Increment register	0	0	0	0	0	1	0	0	5-8
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	5-15	DCR r	Decrement register	0	0	0	0	0	1	0	1	5-8
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	5-15	INR M	Increment memory	0	0	1	1	0	1	0	0	5-8
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	5-16	DCR M	Decrement memory	0	0	1	1	0	1	0	1	5-8
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5-16	INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5-9
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	5-5	INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5-9
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5-9	INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5-9
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5-9	DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5-9
JUMP																					
JMP	Jump unconditional	1	1	0	0	0	0	1	1	5-13	DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5-9
JC	Jump on carry	1	1	0	1	1	0	1	0	5-13	DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5-9
JNC	Jump on no carry	1	1	0	1	0	0	1	0	5-13	ADD r	Add register to A	1	0	0	0	0	S	S	S	5-6
JZ	Jump on zero	1	1	0	0	1	0	1	0	5-13	ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	5-6
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	5-13	ADD M	Add memory to A	1	0	C	0	0	1	1	0	5-6
JP	Jump on positive	1	1	1	1	0	0	1	0	5-13	ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	5-7
JM	Jump on minus	1	1	1	1	1	0	1	0	5-13	ADI	Add immediate to A	1	1	0	0	0	1	1	0	5-6
JPE	Jump on parity even	1	1	1	0	1	0	1	0	5-13	ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	5-7
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	5-13	DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	5-9
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5-15	DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	5-9
CALL																					
CALL	Call unconditional	1	1	C	0	1	1	0	1	5-13	DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	5-9
CC	Call on carry	1	1	0	1	1	1	0	0	5-14	DAD SP	Add stack pointer to H & L	0	G	1	1	1	0	0	1	5-9
CNC	Call on no carry	1	1	0	1	0	1	0	0	5-14	SUBTRACT										
CALL																					
CALL	Call unconditional	1	1	C	0	1	1	0	1	5-13	SUB r	Subtract register from A	1	0	0	1	0	S	S	S	5-7
CC	Call on carry	1	1	0	1	1	1	0	0	5-14	SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	5-7
CNC	Call on no carry	1	1	0	1	0	1	0	0	5-14	SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	5-7
CALL																					
CALL	Call unconditional	1	1	C	0	1	1	0	1	5-13	SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	5-8
CC	Call on carry	1	1	0	1	1	1	0	0	5-14	SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	5-7
CNC	Call on no carry	1	1	0	1	0	1	0	0	5-14											

8085A INSTRUCTION SET SUMMARY (Cont'd)

Table 6-1

Mnemonic	Description	Instruction Code (1)								Page	Mnemonic	Description	Instruction Code (1)								Page	
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	5-8	RRC	Rotate A right	0	0	0	0	1	1	1	1	5-12	
LOGICAL											RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	5-12	
ANA r	And register with A	1	0	1	0	0	S	S	S	5-9	RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	5-12	
XRA r	Exclusive OR register with A	1	0	1	0	1	S	S	S	5-10	SPECIALS											
ORA r	OR register with A	1	0	1	1	0	S	S	S	5-10	CMA	Complement A	0	0	1	0	1	1	1	1	5-12	
CMP r	Compare register with A	1	0	1	1	1	S	S	S	5-11	STC	Set carry	0	0	1	1	0	1	1	1	5-12	
ANA M	And memory with A	1	0	1	0	0	1	1	0	5-10	CMC	Complement carry	0	0	1	1	1	1	1	1	5-12	
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	5-10	DAA	Decimal adjust A	0	0	1	0	0	1	1	1	5-9	
ORA M	OR memory with A	1	0	1	1	0	1	1	0	5-11	CONTROL											
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	5-11	EI	Enable Interrupts	1	1	1	1	1	0	1	1	5-17	
ANI	And immediate with A	1	1	1	0	0	1	1	0	5-10	DI	Disable Interrupt	1	1	1	1	0	0	1	1	5-17	
XRI	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	5-10	NOP	No-operation	0	0	0	0	0	0	0	0	5-17	
ORI	OR immediate with A	1	1	1	1	0	1	1	0	5-11	HLT	Halt	0	1	1	1	0	1	1	0	5-17	
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	5-11	NEW 8085A INSTRUCTIONS											
ROTATE											RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	0	5-17
RLC	Rotate A left	0	0	0	0	0	1	1	1	5-11	SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	5-18	

NOTES: 1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.

2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.

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8155/8156/8155-2/8156-2 2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

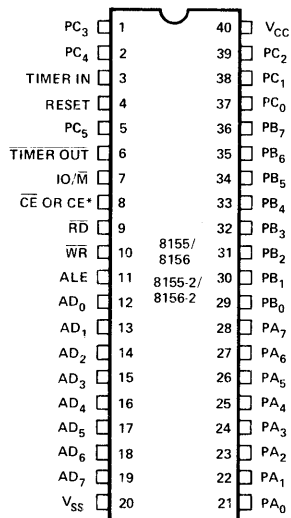
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 89156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

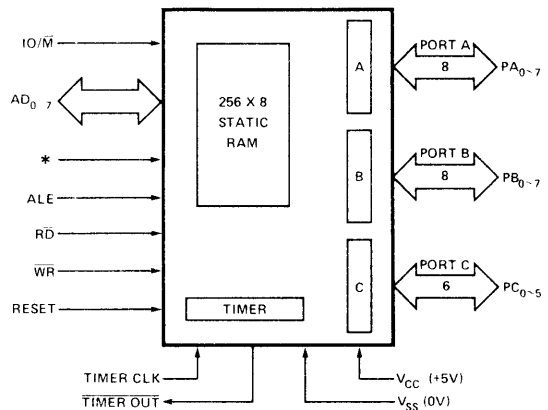
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



*: 8155/8155-2 = $\overline{\text{CE}}$, 8156/8156-2 = CE

8155/8156 PIN FUNCTIONS

<u>Symbol</u>	<u>Function</u>	<u>Symbol</u>	<u>Function</u>
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulses should typically be two 8085A clock cycle times.	ALE (input)	Address Latch Enable: This control signal latches both the address on the AD ₀₋₇ lines and the state of the Chip Enable and IO/ \overline{M} into the chip at the falling edge of ALE.
AD ₀₋₇ (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/56 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/ \overline{M} input. The 8-bit data is either written into the chip or read from the chip, depending on the \overline{WR} or \overline{RD} input signal.	IO/ \overline{M} (input)	Selects memory if low and I/O and command/status registers if high.
CE or \overline{CE} (input)	Chip Enable: On the 8155, this pin is \overline{CE} and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.	PA ₀₋₇ (8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
\overline{RD} (input)	Read control: Input low on this line with the Chip Enable active enables and AD ₀₋₇ buffers. If IO/ \overline{M} pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.	PB ₀₋₇ (8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
\overline{WR} (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/ \overline{M} .	PC ₀₋₅ (6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC ₀₋₅ are used as control signals, they will provide the following: PC ₀ — A INTR (Port A Interrupt) PC ₁ — \overline{ABF} (Port A Buffer Full) PC ₂ — $\overline{A STB}$ (Port A Strobe) PC ₃ — B INTR (Port B Interrupt) PC ₄ — $\overline{B BF}$ (Port B Buffer Full) PC ₅ — B STB (Port B Strobe)
		TIMER IN (input)	Input to the counter-timer.
		$\overline{TIMER OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
		V _{CC}	+5 volt supply.
		V _{SS}	Ground Reference.

DESCRIPTION

The 8155/8156 contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The $\overline{\text{IO/M}}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA₀₋₇, PB₀₋₇, PC₀₋₅) or the memory (RAM) portion. (See Figure 1.)

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{\text{CE}}$, and IO/M are all latched on-chip at the falling edge of ALE. (See Figure 2.)

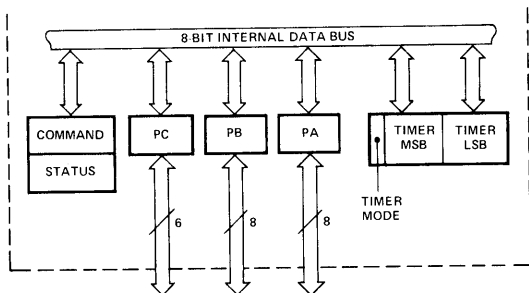
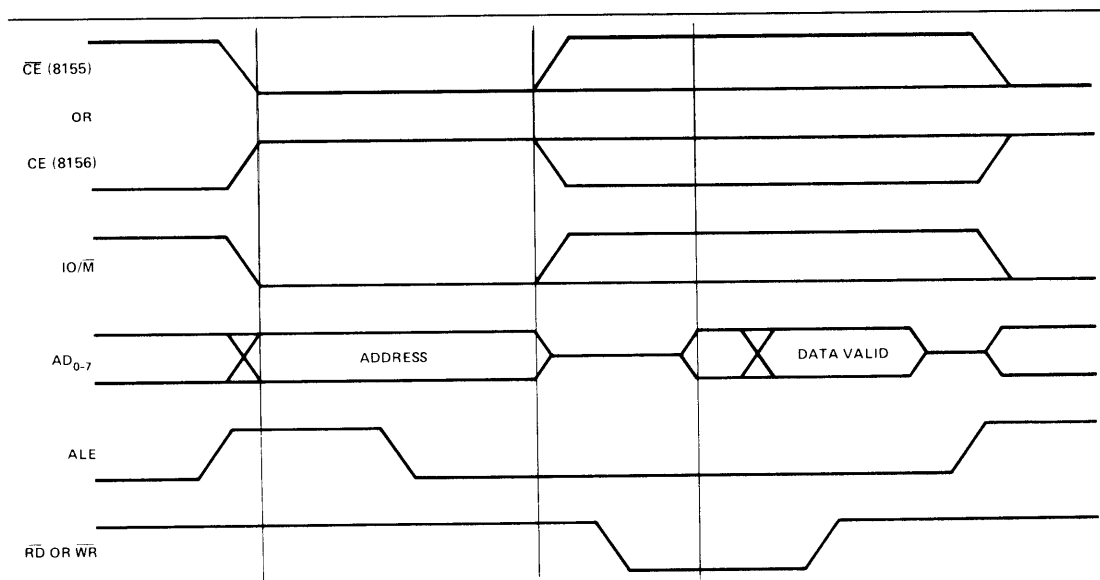


Figure 1. 8155/8156 Internal Registers



NOTE: FOR DETAILED TIMING INFORMATION, SEE FIGURE 12 AND A.C. CHARACTERISTICS.

Figure 2. 8155/8156 On-Board Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/M = 1. The meaning of each bit of the command byte is defined in Figure 3. The contents of the command register may never be read.

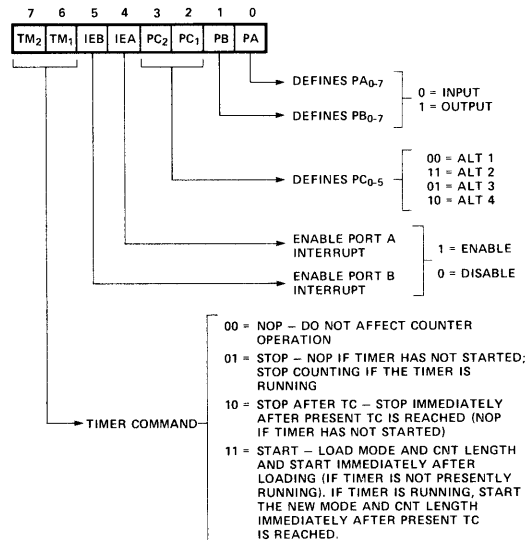


Figure 3. Command Register Bit Assignment

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 4. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

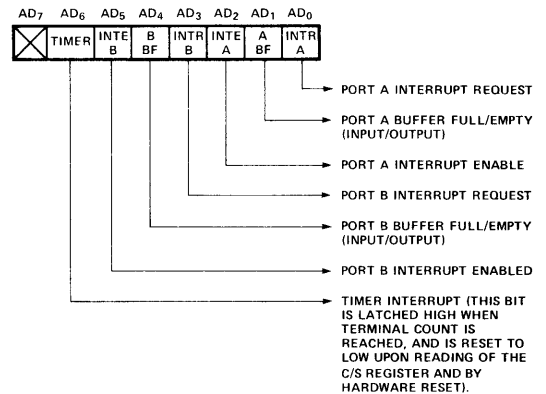


Figure 4. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the 8155/8156 consists of five registers: (See Figure 5.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD₀₋₇ lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA₀₋₇. The address of this register is XXXXX001.
- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB₀₋₇. The address of this register is XXXXX010.
- **PC Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD₂ and AD₃ bits of the C/S register.

When PC₀₋₅ is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								SELECTION
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C - General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.
†: I/O Address must be qualified by CE = 1 (8156) or CE = 0 (8155) and IO/M = 1 in order to select the appropriate register.

Figure 5. I/O port and Timer Addressing Scheme

Figure 6 shows how I/O PORTS A and B are structured within the 8155 and 8156:

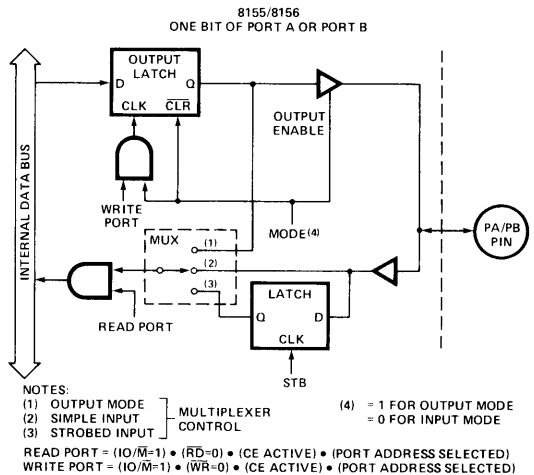


Figure 6. 8155/8156 Port Functions

TABLE 1. TABLE OF PORT CONTROL ASSIGNMENT.

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B STB (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155/8156 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155/56 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 7 shows how the 8155/8156 I/O ports might be configured in a typical MCS-85 system.

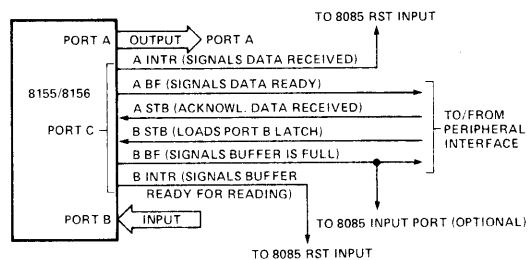


Figure 7. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 5).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 8). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

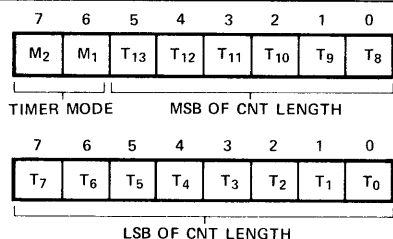


Figure 8. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

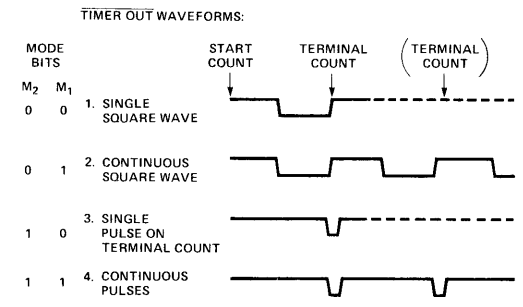


Figure 9. Timer Modes

Bits 6-7 (TM₂ and TM₁) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM ₂	TM ₁	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 10.

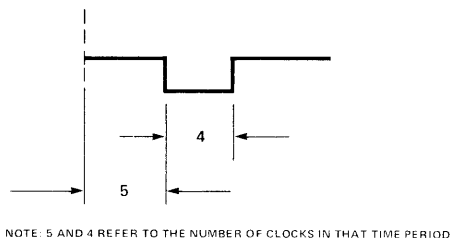


Figure 10. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155/8156 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by two twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155/56 always counts out the right number of pulses in generating the TIMER OUT waveforms.

EXAMPLE PROGRAM

Following is an actual sequence of program steps that adjusts the 8155/56 count register contents to obtain the count, extracted from Intel® Application Note AP38. "Application Techniques for the Intel 8085A Bus." First store the value of the full original count in register HL of the 8085A. Then stop the count to avoid getting an incorrect count value. Then sample the timer-counter, storing the lower-order byte of the current count register in register C and the higher-order count byte in register B. Then, call the following 8080A/8085A subroutine:

ADJUST, 78	MOV A,B	;Load accumulator with upper half ; of count.
E63F	ANI 3F	;Reset upper 2 bits and clear carry.
1F	RAR	;Rotate right through carry.
47	MOV B,A	;Store shifted value back in B.
79	MOV A,C	;Load accumulator with lower half.
1F	RAR	;Rotate right through carry.
4F	MOV C,A	;Store lower byte in C.
D0	RNC	;If in 2nd half of count, return. ;If in 1st half, go on.
3F	CMC	;Clear carry.
7C	MOV A,H	;Divide full count by 2. (If HL ;is odd, disregard remainder.)
1F	RAR	
67	MOV H,A	
7D	MOV A,L	
1F	RAR	
6F	MOV L,A	
09	DAD B	;Double-precision add HL and BC.
44	MOV B,H	;Store results back in BC.
4D	MOV C,L	
C9	RET	;Return.

After executing the subroutine, BC will contain the remaining count in the current count cycle.

8085A MINIMUM SYSTEM CONFIGURATION

Figure 11a shows a minimum system using three chips, containing:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

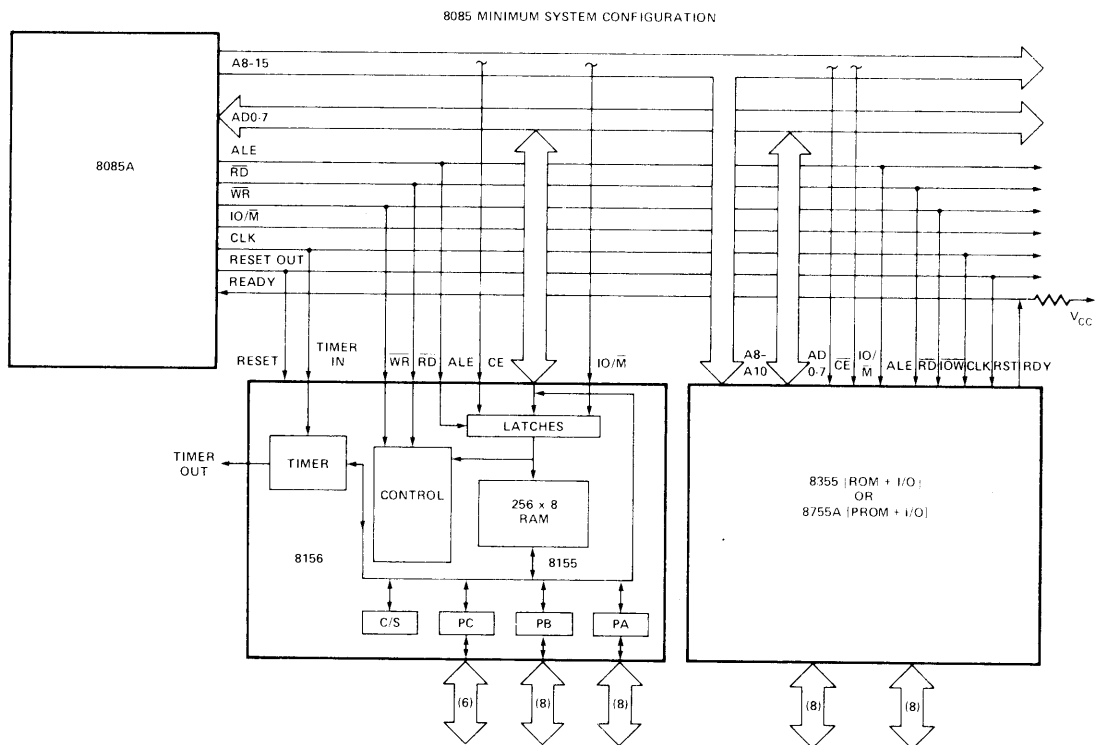


Figure 11a. 8085A Minimum System Configuration. (Memory Mapped I/O)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

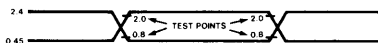
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2\text{mA}$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\mu\text{A}$
I_{IL}	Input Leakage		± 10	μA	$V_{IN} = V_{CC}$ to 0V
I_{LO}	Output Leakage Current		± 10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	
I_{IL} (CE)	Chip Enable Leakage				
	8155		+100	μA	$V_{IN} = V_{CC}$ to 0V
	8156		-100	μA	

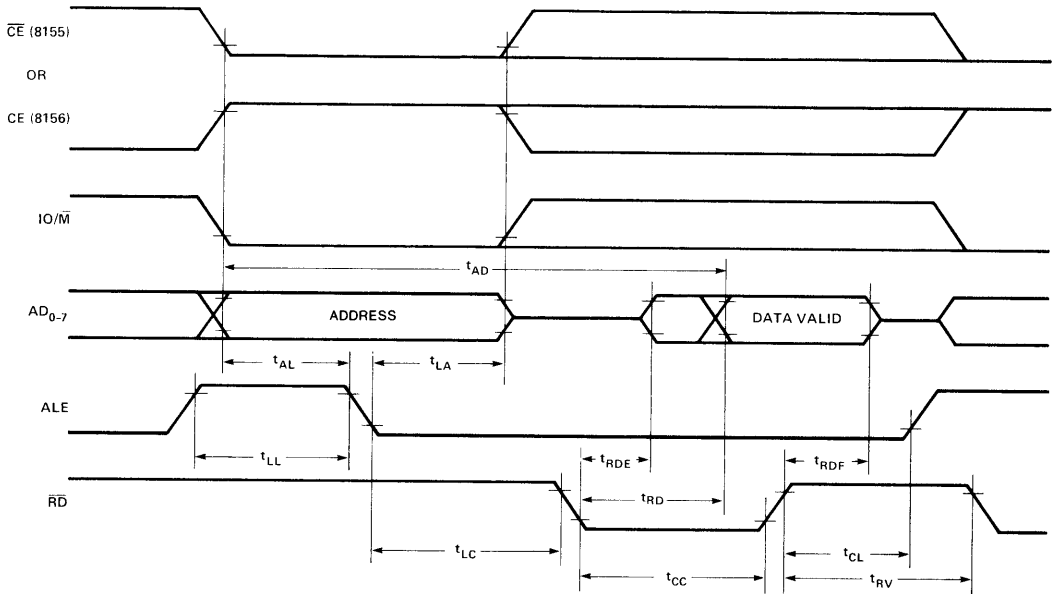
A.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5\text{V} \pm 5\%$)

SYMBOL	PARAMETER	8155/8156		8155-2/8156-2 (Preliminary)		UNITS
		MIN.	MAX.	MIN.	MAX.	
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float After READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to WRITE Set Up Time	150		100		ns
t_{WD}	Data In Hold Time After WRITE	0		0		ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{WP}	WRITE to Port Output		400		300	ns
t_{PR}	Port Input Setup Time	70		50		ns
t_{RP}	Port Input Hold Time	50		10		ns
t_{SBF}	Strobe to Buffer Full		400		300	ns
t_{SS}	Strobe Width	200		150		ns
t_{RBE}	READ to Buffer Empty		400		300	ns
t_{SI}	Strobe to INTR On		400		300	ns
t_{RDI}	READ to INTR Off		400		300	ns
t_{PSS}	Port Setup Time to Strobe Strobe	50		0		ns
t_{PHS}	Port Hold Time After Strobe	120		100		ns
t_{SBE}	Strobe to Buffer Empty		400		300	ns
t_{WBF}	WRITE to Buffer Full		400		300	ns
t_{WI}	WRITE to INTR Off		400		300	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400		300	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400		300	ns
t_{RDE}	Data Bus Enable from READ Control	10		10		ns
t_1	TIMER-IN Low Time	80		40		ns
t_2	TIMER-IN High Time	120		70		ns

Input Waveform for A.C. Tests:

WAVEFORMS

a. Read Cycle



b. Write Cycle

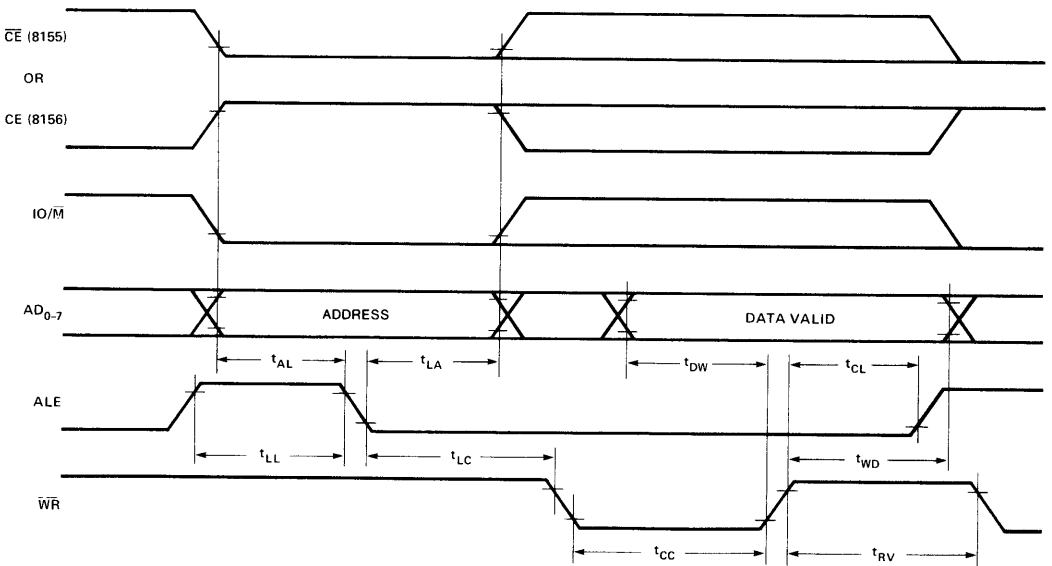
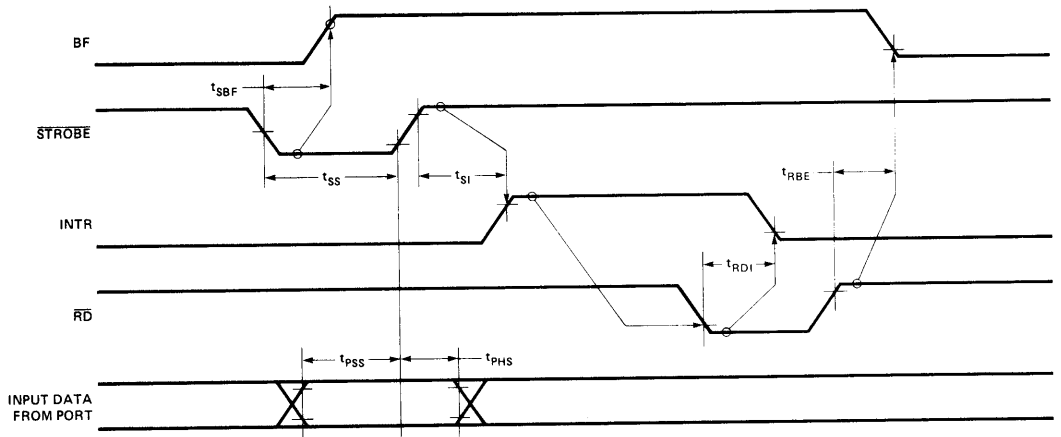


Figure 12. 8155/8156 Read/Write Timing Diagrams

a. Strobed Input Mode



b. Strobed Output Mode

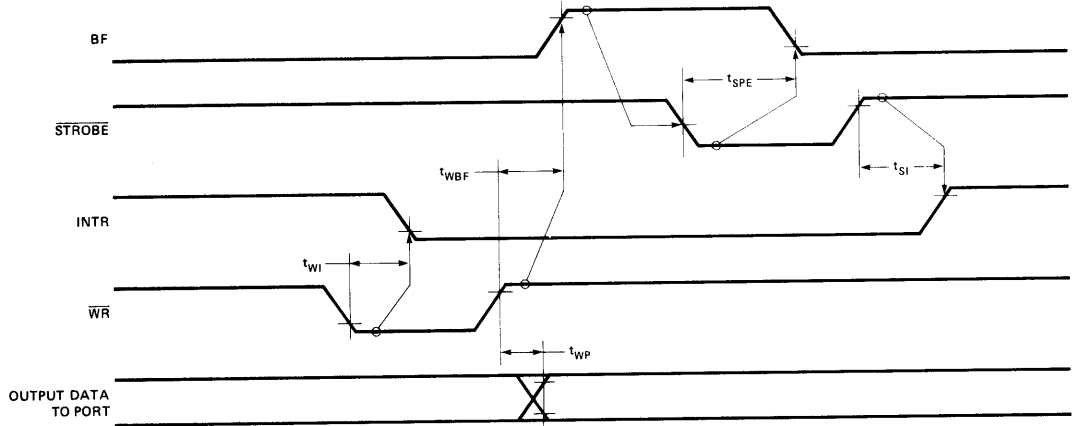
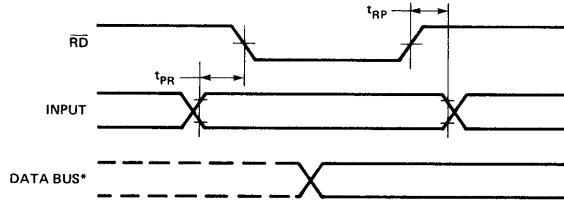
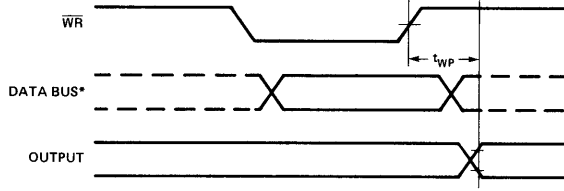


Figure 13. Strobed I/O Timing

a. Basic Input Mode



b. Basic Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 7.

Figure 14. Basic I/O Timing Waveform

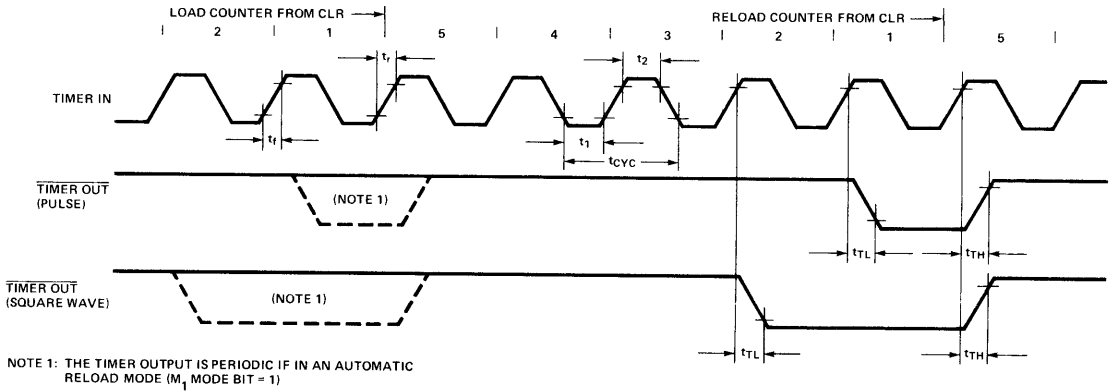


Figure 15. Timer Output Waveform Countdown from 5 to 1



PRELIMINARY
 Notice: This is not a final specification. Some
 parametric limits are subject to change.

8185/8185-2

1024 x 8-BIT STATIC RAM FOR MCS-85™

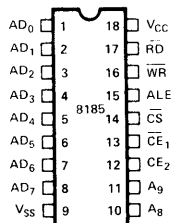
- **Multiplexed Address and Data Bus**
- **Low Standby Power Dissipation**
- **Directly Compatible with 8085A and 8088 Microprocessors**
- **Single +5V Supply**
- **Low Operating Power Dissipation**
- **High Density 18-Pin Package**

The Intel® 8185 is an 8192-bit static random access memory (RAM) organized as 1024 words by 8-bits using N-channel Silicon-Gate MOS technology. The multiplexed address and data bus allows the 8185 to interface directly to the 8085A and 8088 microprocessors to provide a maximum level of system integration.

The low standby power dissipation minimizes system power requirements when the 8185 is disabled.

The 8185-2 is a high-speed selected version of the 8185 that is compatible with the 5 MHz 8085A-2 and the full speed 5 MHz 8088.

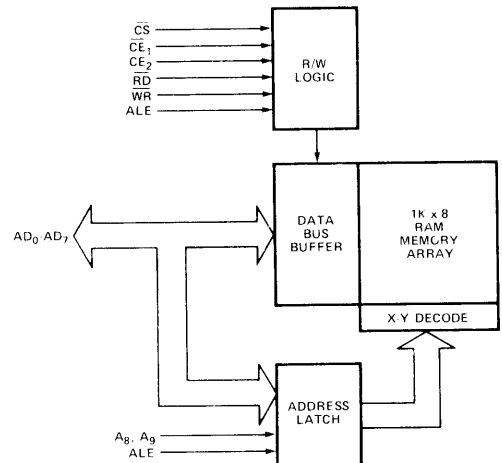
PIN CONFIGURATION



PIN NAMES

AD ₀ -AD ₇	ADDRESS/DATA LINES
A ₈ , A ₉	ADDRESS LINES
CS	CHIP SELECT
CE ₁	CHIP ENABLE (I/O/M)
CE ₂	CHIP ENABLE
ALE	ADDRESS LATCH ENABLE
RD	READ ENABLE
WR	WRITE ENABLE

BLOCK DIAGRAM



PRELIMINARY
 Notice: This is not a final specification. Some parametric limits are subject to change.

OPERATIONAL DESCRIPTION

The 8185 has been designed to provide for direct interface to the multiplexed bus structure and bus timing of the 8085A microprocessor.

At the beginning of an 8185 memory access cycle, the 8-bit address on AD₀₋₇, A₈ and A₉, and the status of \overline{CE}_1 and \overline{CE}_2 are all latched internally in the 8185 by the falling edge of ALE. If the latched status of both \overline{CE}_1 and \overline{CE}_2 are active, the 8185 powers itself up, but no action occurs until the \overline{CS} line goes low and the appropriate \overline{RD} or \overline{WR} control signal input is activated.

The \overline{CS} input is not latched by the 8185 in order to allow the maximum amount of time for address decoding in selecting the 8185 chip. Maximum power consumption savings will occur, however, only when \overline{CE}_1 and \overline{CE}_2 are activated selectively to power down the 8185 when it is not in use. A possible connection would be to wire the 8085A's IO/M line to the 8185's \overline{CE}_1 input, thereby keeping the 8185 powered down during I/O and interrupt cycles.

**TABLE 1.
 TRUTH TABLE FOR
 POWER DOWN AND FUNCTION ENABLE**

\overline{CE}_1	\overline{CE}_2	\overline{CS}	(\overline{CS}^*) ²	8185 Status
1	X	X	0	Power Down and Function Disable ₁
X	0	X	0	Power Down and Function Disable ₁
0	1	1	0	Powered Up and Function Disable ₁
0	1	0	1	Powered Up and Enabled

Notes:

X: Don't Care.

1: Function Disable implies Data Bus in high impedance state and not writing.

2: $\overline{CS}^* = (\overline{CE}_1 = 0) \cdot (\overline{CE}_2 = 1) \cdot (\overline{CS} = 0)$

$\overline{CS}^* = 1$ signifies all chip enables and chip select active

**TABLE 2.
 TRUTH TABLE FOR
 CONTROL AND DATA BUS PIN STATUS**

(\overline{CS}^*)	\overline{RD}	\overline{WR}	AD ₀₋₇ During Data Portion of Cycle	8185 Function
0	X	X	Hi-Impedance	No Function
1	0	1	Data from Memory	Read
1	1	0	Data to Memory	Write
1	1	1	Hi-Impedance	Reading, but not Driving Data Bus

Note:

X: Don't Care.

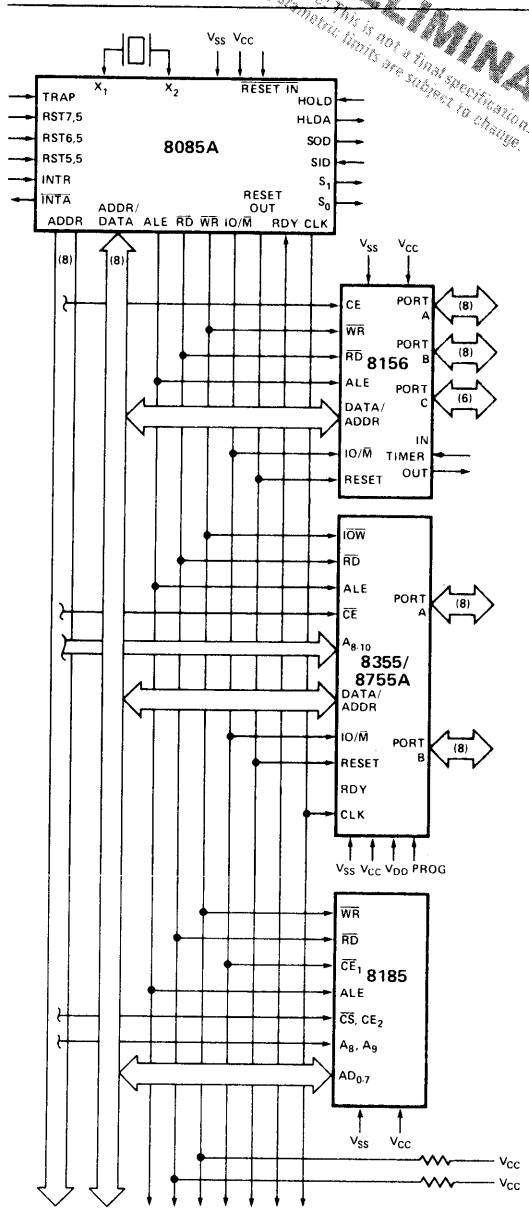


Figure 1. 8185 in an MCS-85 System.

- 4 Chips:
- 2K Bytes ROM
- 1.25K Bytes RAM
- 38 I/O Lines
- 1 Counter/Timer
- 2 Serial I/O Lines
- 5 Interrupt Inputs

PRELIMINARY
 Notice: This is not a final specification. Some parametric limits are subject to change.

8088 FIVE CHIP SYSTEM

Figure 2 shows a five chip system containing:

- 1.25 K Bytes RAM
- 2 K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

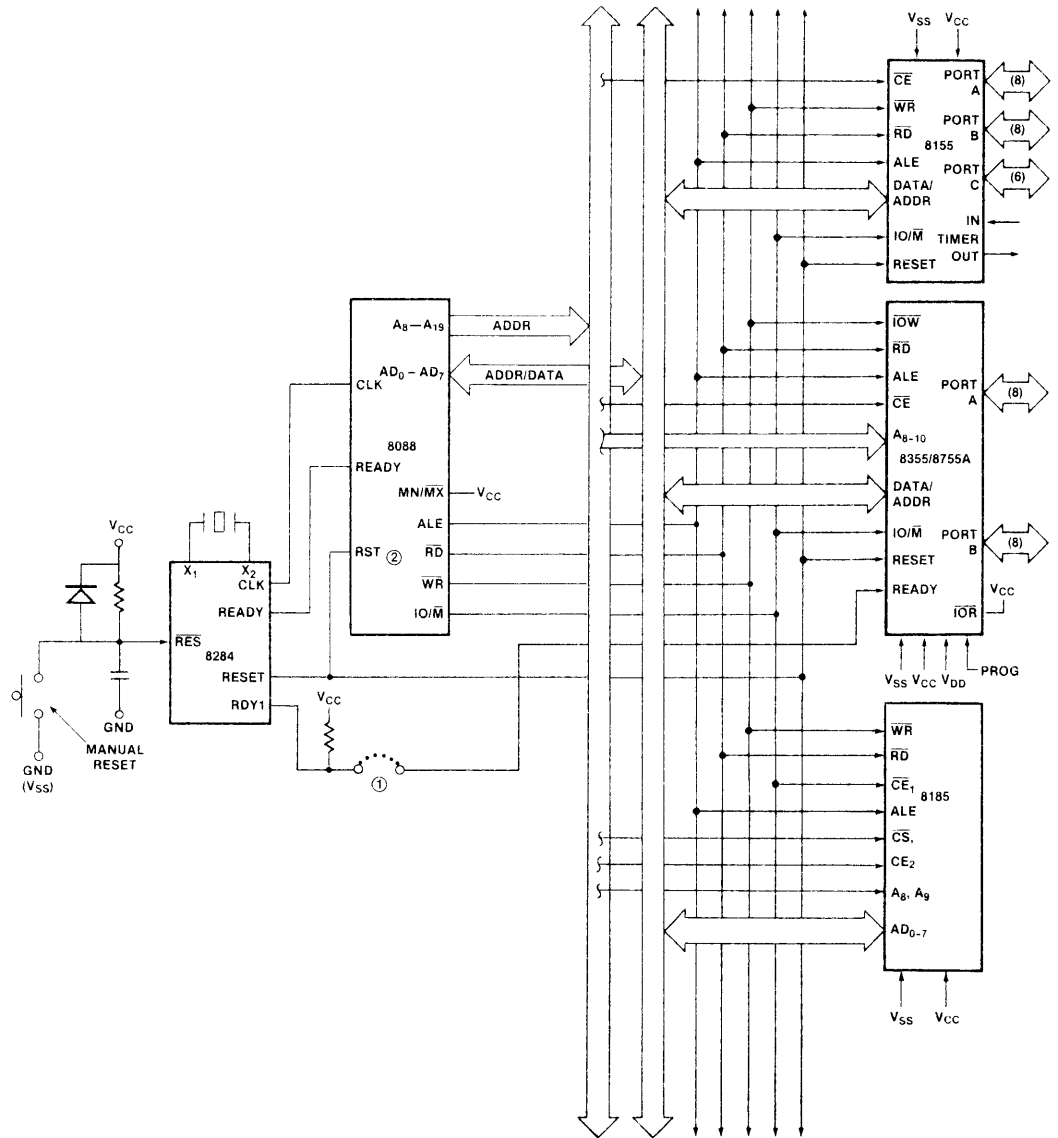


Figure 2. 8088 Five Chip System Configuration.

PRELIMINARY
 Notice: This is not a final
 packaging label.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
with Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V _{IL}	Input Low Voltage	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	V	
V _{OL}	Output Low Voltage		0.45	V	I _{OL} = 2mA
V _{OH}	Output High Voltage	2.4			I _{OH} = 400μA
I _{IL}	Input Leakage		±10	μA	V _{IN} = V _{CC} to 0V
I _{LO}	Output Leakage Current		±10	μA	0.45V ≤ V _{OUT} ≤ V _{CC}
I _{CC}	V _{CC} Supply Current				
	Powered Up		100	mA	
	Powered Down		25	mA	

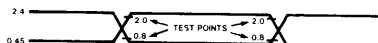
A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter ^[1]	8185 Preliminary		8185-2 Preliminary		Units
		Min.	Max.	Min.	Max.	
t _{AL}	Address to Latch Set Up Time	50		30		ns
t _{LA}	Address Hold Time After Latch	80		30		ns
t _{LC}	Latch to READ/WRITE Control	100		40		ns
t _{RD}	Valid Data Out Delay from READ Control		170		140	ns
t _{LD}	ALE to Data Out Valid		300		200	ns
t _{LL}	Latch Enable Width	100		70		ns
t _{RDF}	Data Bus Float After READ	0	100	0	80	ns
t _{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t _{CC}	READ/WRITE Control Width	250		200		ns
t _{DW}	Data In to WRITE Set Up Time	150		150		ns
t _{WD}	Data In Hold Time After WRITE	20		20		ns
t _{SC}	Chip Select Set Up to Control Line	10		10		ns
t _{CS}	Chip Select Hold Time After Control	10		10		ns
t _{ALCE}	Chip Enable Set Up to ALE Falling	30		10		ns
t _{LACE}	Chip Enable Hold Time After ALE	50		30		ns

Notes:

- All AC parameters are referenced at
 - 2.4V and .45V for inputs
 - 2.0V and .8V for outputs.

Input Waveform for A.C. Tests:



PRELIMINARY
 Notice: This is not a final specification. Some
 parametric limits are subject to change.

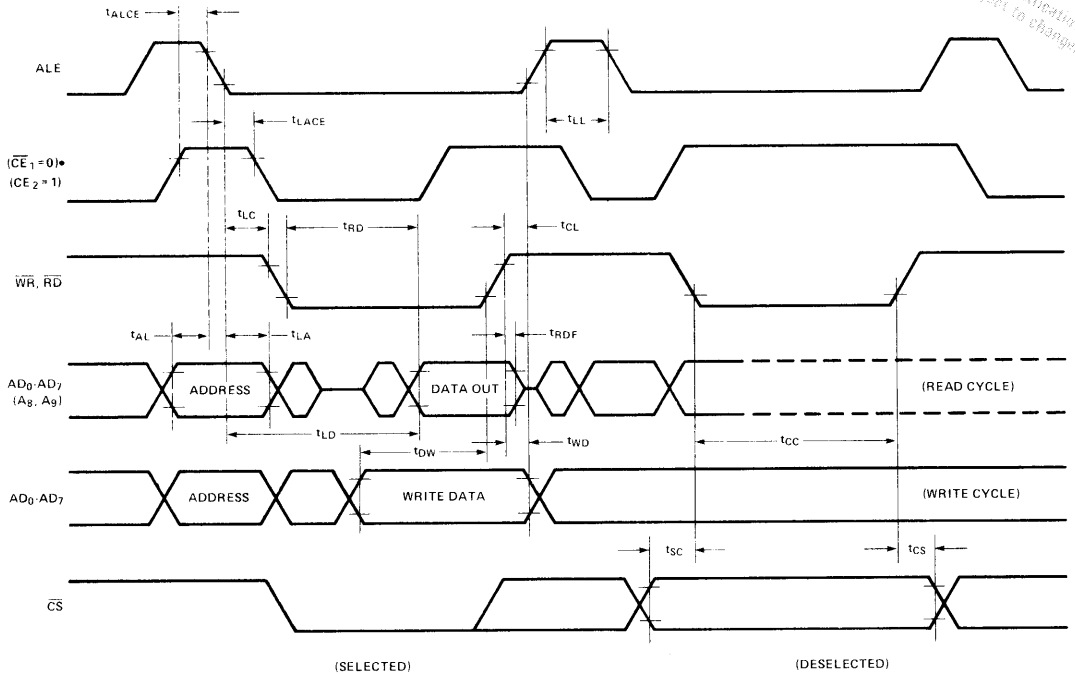


Figure 3. 8185 Timing.



8355/8355-2 16,384-BIT ROM WITH I/O

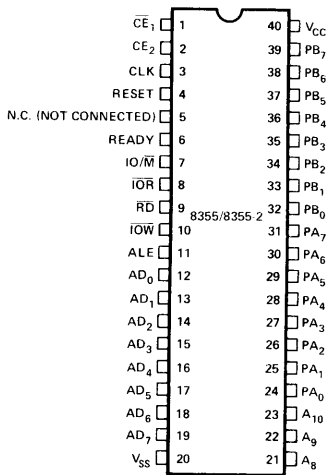
- 2048 Words x 8 Bits
- Single +5V Power Supply
- Directly compatible with 8085A and 8088 Microprocessors
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- Internal Address Latch
- 40-Pin DIP

The Intel® 8355 is a ROM and I/O chip to be used in the 8085A and 8088 microprocessor systems. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 400 ns to permit use with no wait states in the 8085A CPU.

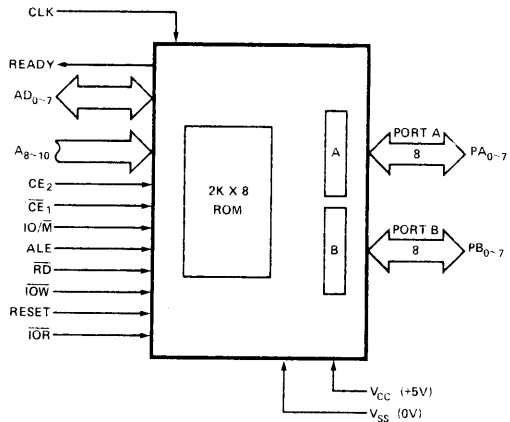
The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines and each I/O port line is individually programmable as input or output.

The 8355-2 has a 300ns access time for compatibility with the 8085A-2 and full speed 5 MHz 8088 microprocessors.

PIN CONFIGURATION



BLOCK DIAGRAM



Symbol	Function	Symbol	Function
ALE (Input)	When ALE (Address Latch Enable) is high, AD ₀₋₇ , IO/ \overline{M} , A ₈₋₁₀ , CE, and \overline{CE} enter address latched. The signals (AD, IO/ \overline{M} , A ₈₋₁₀ , CE, \overline{CE}) are latched in at the trailing edge of ALE.	CLK (Input)	The CLK is used to force the READY into its high impedance state after it has been forced low by \overline{CE} low, CE high and ALE high.
AD ₀₋₇ (Input)	Bidirectional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD ₀ . If \overline{RD} or \overline{IOR} is low when the latched chip enables are active, the output buffers present data on the bus.	READY (Output)	<u>Ready</u> is a 3-state output controlled by \overline{CE}_1 , CE ₂ , ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 6).
A ₈₋₁₀ (Input)	These are the high order bits of the ROM address. They do not affect I/O operations.	PA ₀₋₇ (Input/ Output)	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and \overline{IOW} is low and a 0 was previously latched from AD ₀ .
\overline{CE}_1 CE ₂ (Input)	Chip Enable Inputs: \overline{CE}_1 is active low and CE ₂ is active high. The 8355 can be accessed only when <u>BOTH</u> Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD ₀₋₇ and READY outputs will be in a high impedance state.	PB ₀₋₇ (Input/ Output)	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD ₀ .
IO/ \overline{M} (Input)	If the latched IO/ \overline{M} is high when \overline{RD} is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.	RESET (Input)	An input high on RESET causes all pins in Port A and B to assume input mode.
\overline{RD} (Input)	If the latched Chip Enables are active when \overline{RD} goes low, the AD ₀₋₇ output buffers are enabled and output either the selected ROM location or I/O port. When both \overline{RD} and \overline{IOR} are high, the AD ₀₋₇ output buffers are 3-state.	\overline{IOR} (Input)	When the Chip Enables are active, a low on \overline{IOR} will output the selected I/O port onto the AD bus. \overline{IOR} low performs the same function as the combination IO/ \overline{M} high and \overline{RD} low. When \overline{IOR} is not used in a system, \overline{IOR} should be tied to Vcc ("1").
\overline{IOW} (Input)	If the latched Chip Enables are active, a low on \overline{IOW} causes the output port pointed to by the latched value of AD ₀ to be written with the data on AD ₀₋₇ . The state of IO/ \overline{M} is ignored.	Vcc	+5 volt supply.
		Vss	Ground Reference.

FUNCTIONAL DESCRIPTION

ROM Section

The 8355 contains an 8-bit address latch which allows it to interface directly to MCS-48 and MCS-85 Microcomputers without additional hardware.

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/M is low when RD goes low, the contents of the ROM location addressed by the latched address are put out through AD₀₋₇ output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD₀₋₁. Two 8-bit Data Direction Registers (DDR) in 8355 determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8355 are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

AD ₁	AD ₀	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

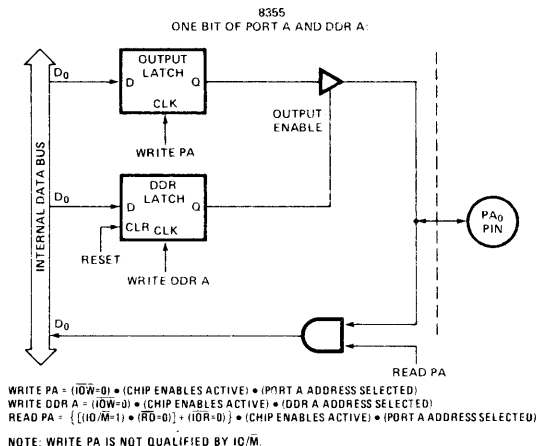
When $\overline{IO\overline{M}}$ goes low and the Chip Enables are active, the data on the AD₀₋₇ is written into I/O port selected by the latched value of AD₀₋₁. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/M. The actual output level does not change until $\overline{IO\overline{M}}$ returns high (glitch free output).

A port can be read out when the latched Chip Enables are active and either RD goes low with IO/M high, or $\overline{IO\overline{R}}$ goes low. Both input and output mode bits of a selected port will appear on lines AD₀₋₇.

To clarify the function of the I/O ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.



System Interface with 8085A and 8088

A system using the 8355 can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE and \overline{CE} . By using a combination of unused address lines A₁₁₋₁₅ and the Chip Enable inputs, the system can use up to 5 each 8355's without requiring a CE decoder. See Figure 2a and 2b.

If a memory mapped I/O approach is used the 8355 will be selected by the combination of both the Chip Enables and IO/M using the AD₈₋₁₅ address lines. See Figure 1.

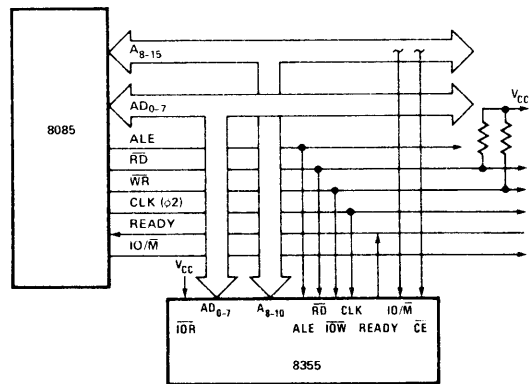


Figure 1. 8355 in 8085A System (Memory-Mapped I/O)

8088 FIVE CHIP SYSTEM

Figure 2a shows a five chip system containing:

- 1.25 K Bytes RAM
- 2 K Bytes ROM
- 38 I/O Pins
- 1 Internal Timer
- 2 Interrupt Levels

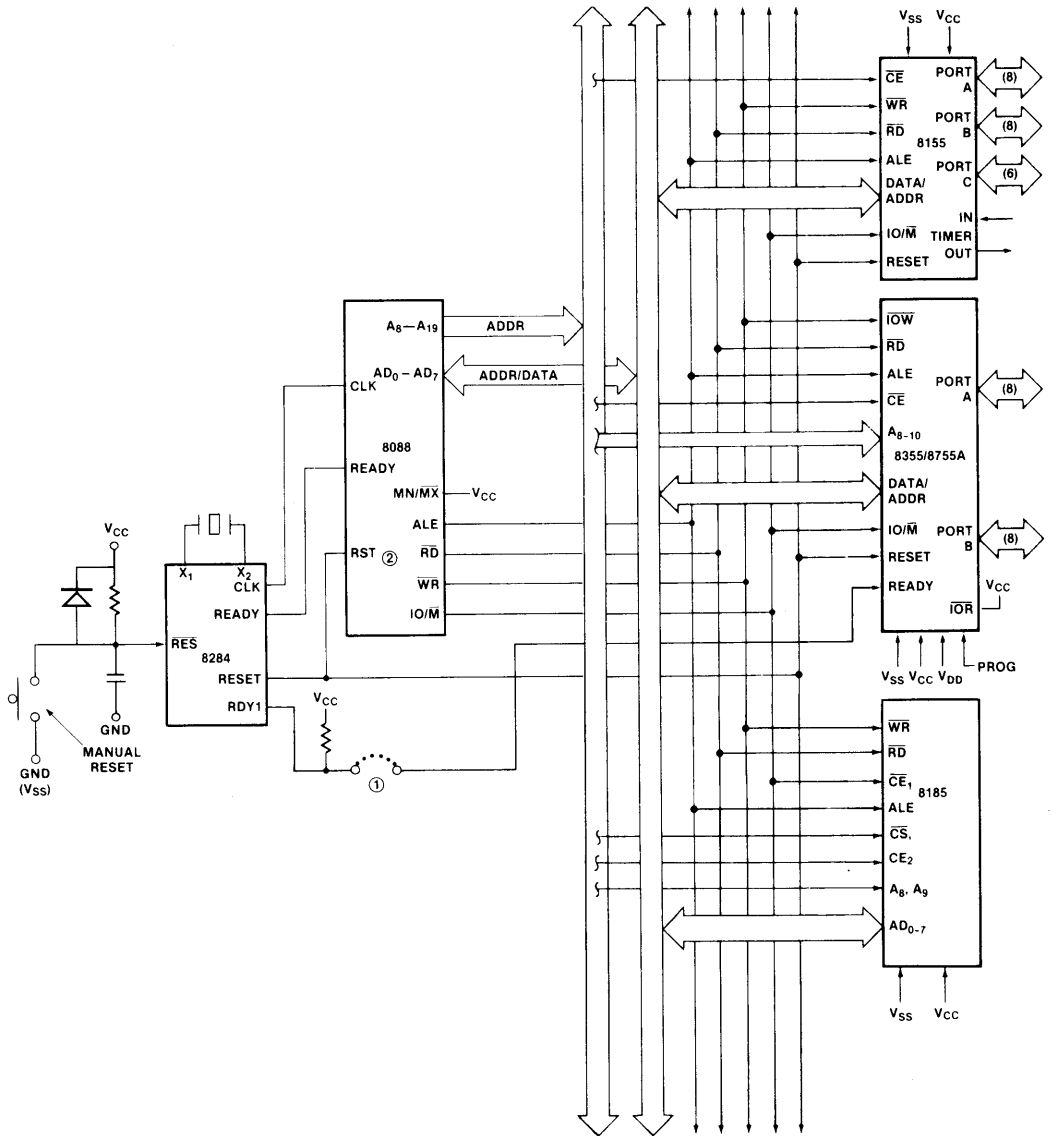
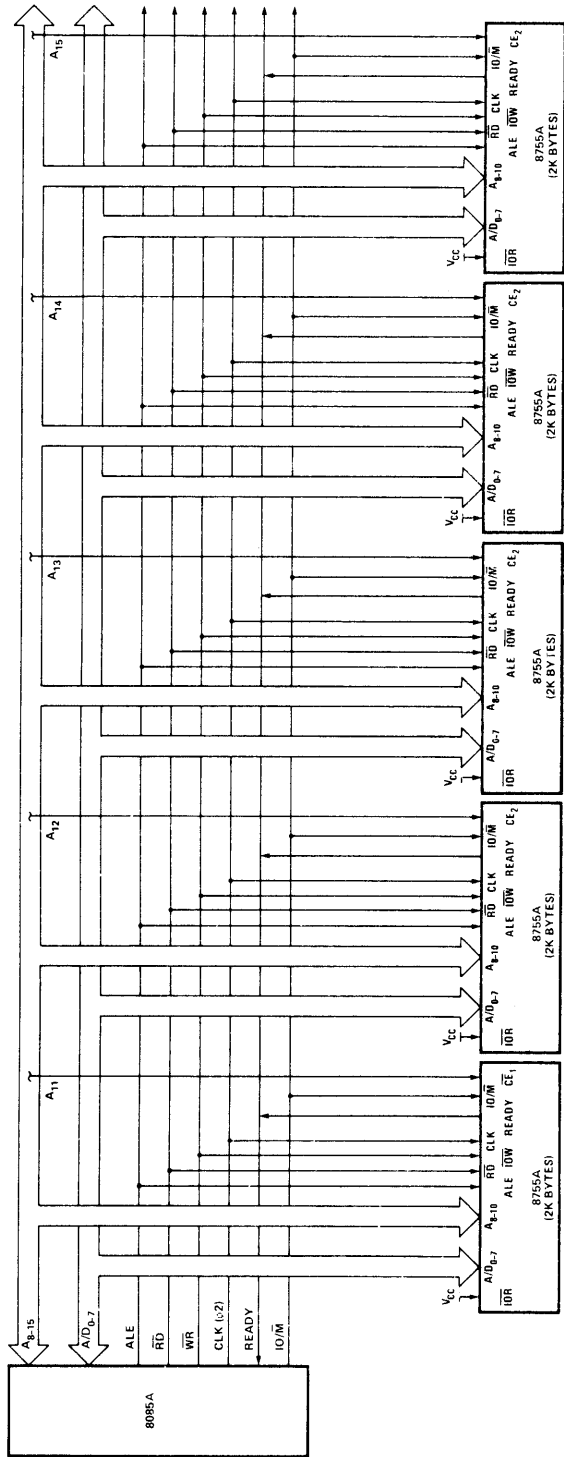


Figure 2a. 8088 Five Chip System Configuration



Note: Use \overline{CE}_1 for the first 8755A in the system, and CE₂ for the other 8755A's in a system without CE decoder.

Figure 2b. 8355 in 8085A System (Standard I/O)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

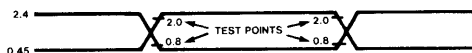
D.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	V	$V_{CC} = 5.0V$
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2mA$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\mu A$
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$ to 0V
I_{LO}	Output Leakage Current		± 10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	8355		8355-2 (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	320		200		ns
T_1	CLK Pulse Width	80		40		ns
T_2	CLK Pulse Width	120		70		ns
$t_{r,tr}$	CLK Rise and Fall Time		30		30	ns
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to Write Set Up Time	150		150		ns
t_{WD}	Data In Hold Time After WRITE	10		10		ns
t_{WP}	WRITE to Port Output		400		400	ns
t_{PR}	Port Input Set Up Time	50		50		ns
t_{RP}	Port Input Hold Time	50		50		ns
t_{RYH}	READY HOLD Time	0	160	0	160	ns
t_{ARY}	ADDRESS CE to READY		160		160	ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{RDE}	READ Control to Data Bus Enable	10		10		ns

Note: $C_{LOAD} = 150pF$

Input Waveform for A.C. Tests:

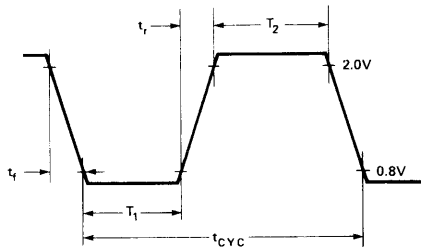


Figure 3. Clock Specification for 8355

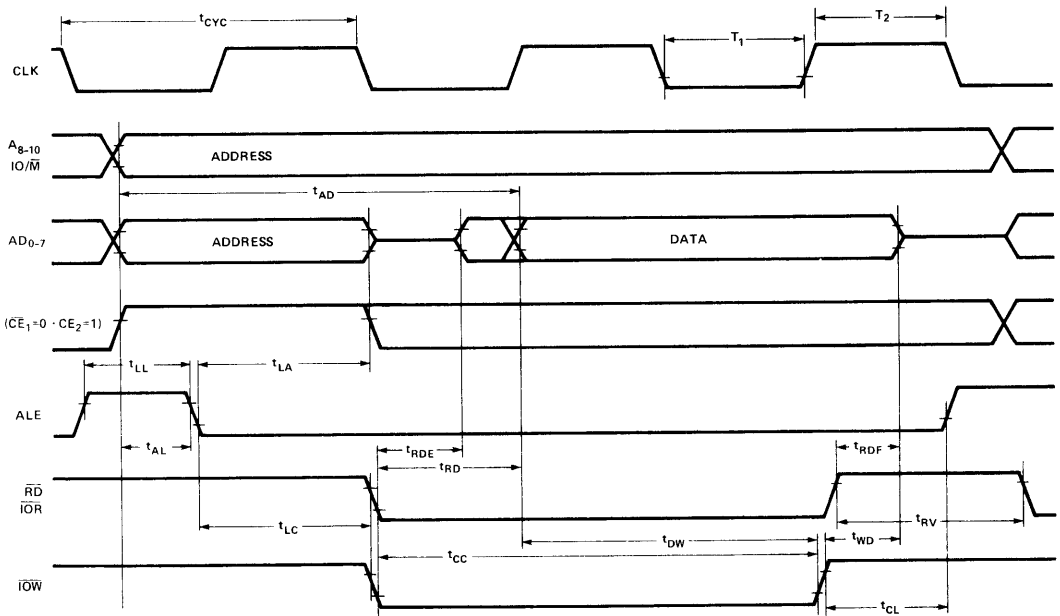
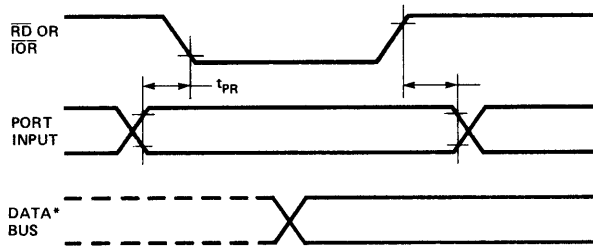


Figure 4. ROM Read and I/O Read and Write

a. Input Mode



b. Output Mode

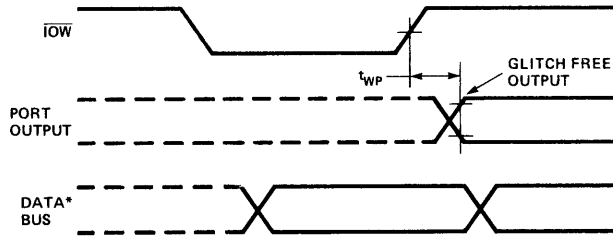


Figure 5. I/O Port Timing

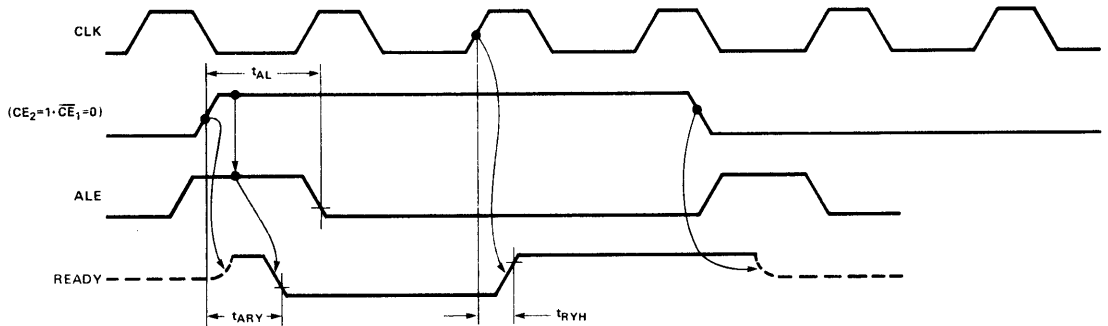


Figure 6. Wait State Timing (Ready = 0)



8755A/8755A-2 16,384-BIT EPROM WITH I/O

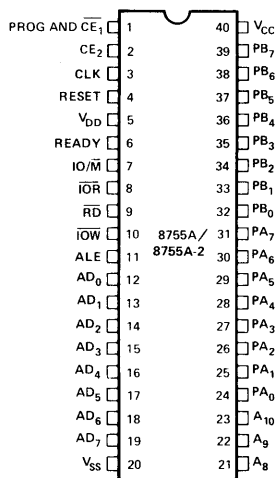
- 2048 Words × 8 Bits
- Single +5V Power Supply (V_{CC})
- Directly Compatible with 8085A and 8088 Microprocessors
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP

The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085A and 8088 microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A CPU.

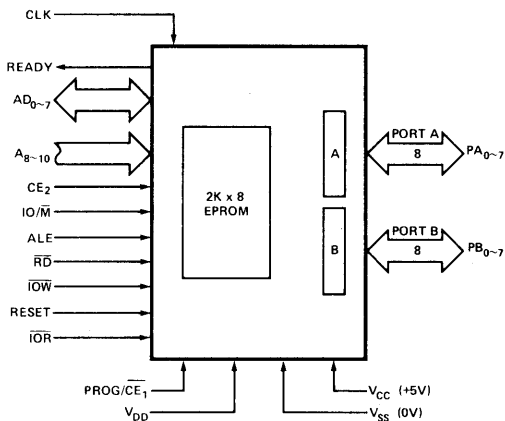
The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

The 8755A-2 is a high speed selected version of the 8755A compatible with the 5 MHz 8085A-2 and the full speed 5 MHz 8088.

PIN CONFIGURATION



BLOCK DIAGRAM



8755A FUNCTIONAL PIN DEFINITION

<u>Symbol</u>	<u>Function</u>	<u>Symbol</u>	<u>Function</u>
ALE (input)	When Address Latch Enable goes high, AD ₀₋₇ , IO/M, A ₈₋₁₀ , CE ₂ , and $\overline{CE_1}$ enter the address latches. The signals (AD, IO/M, A ₈₋₁₀ , CE) are latched in at the trailing edge of ALE.	READY (output)	READY is a 3-state output controlled by CE ₂ , $\overline{CE_1}$, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK. (See Figure 6.)
AD ₀₋₇ (input/output)	Bidirectional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD ₀ . If \overline{RD} or \overline{IOR} is low when the latched Chip Enables are active, the output buffers present data on the bus.	PA ₀₋₇ (input/output)	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and \overline{IOW} is low and a 0 was previously latched from AD ₀ , AD ₁ . Read operation is selected by either \overline{IOR} low and active Chip Enables and AD ₀ and AD ₁ low, or IO/M high, \overline{RD} low, active Chip Enables, and AD ₀ and AD ₁ low.
A ₈₋₁₀ (input)	These are the high order bits of the PROM address. They do not affect I/O operations.	PB ₀₋₇ (input/output)	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD ₀ and a 0 from AD ₁ .
PROG/ $\overline{CE_1}$ CE ₂ (input)	Chip Enable Inputs: $\overline{CE_1}$ is active low and CE ₂ is active high. The 8755A can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD ₀₋₇ and READY outputs will be in a high impedance state. $\overline{CE_1}$ is also used as a programming pin. (See section on programming.)	RESET (input)	In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
IO/ \overline{M} (input)	If the latched IO/ \overline{M} is high when \overline{RD} is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.	\overline{IOR} (input)	When the Chip Enables are active, a low on \overline{IOR} will output the selected I/O port onto the AD bus. \overline{IOR} low performs the same function as the combination of IO/ \overline{M} high and \overline{RD} low. When \overline{IOR} is not used in a system, \overline{IOR} should be tied to V _{CC} ("1").
\overline{RD} (input)	If the latched Chip Enables are active when \overline{RD} goes low, the AD ₀₋₇ output buffers are enabled and output either the selected PROM location or I/O port. When both \overline{RD} and \overline{IOR} are high, the AD ₀₋₇ output buffers are 3-stated.	V _{CC}	+5 volt supply.
\overline{IOW} (input)	If the latched Chip Enables are active, a low on \overline{IOW} causes the output port pointed to by the latched value of AD ₀ to be written with the data on AD ₀₋₇ . The state of IO/ \overline{M} is ignored.	V _{SS}	Ground Reference.
CLK (input)	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE_1}$ low, CE ₂ high, and ALE high.	V _{DD}	V _{DD} is a programming voltage, and must be tied to +5V when the 8755A is being read. For programming, a high voltage is supplied with V _{DD} = 25V, typical. (See section on programming.)

FUNCTIONAL DESCRIPTION

PROM Section

The 8755A contains an 8-bit address latch which allows it to interface directly to MCS-48 and MCS-85 Microcomputers without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and CE. The address, \overline{CE}_1 and CE_2 are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/M is low when \overline{RD} goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines.

I/O Section

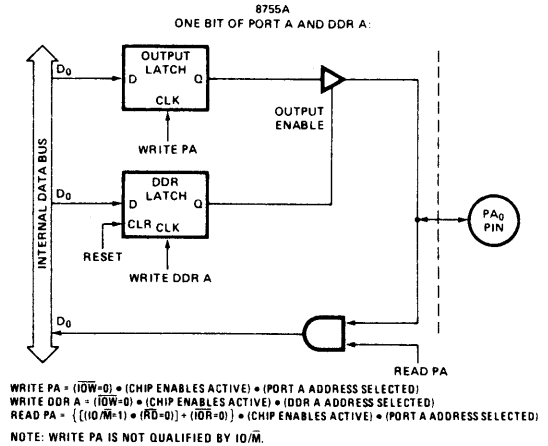
The I/O section of the chip is addressed by the latched value of AD_{0-1} . Two 8-bit Data Direction Registers (DDR) in 8755A determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8755A are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When \overline{IOW} goes low and the Chip Enables are active, the data on the AD is written into I/O port selected by the latched value of AD_{0-1} . During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/M. The actual output level does not change until \overline{IOW} returns high. (glitch free output)

A port can be read out when the latched Chip Enables are active and either \overline{RD} goes low with IO/M high, or \overline{IOR} goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7} .

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.



Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

TABLE 1. 8755A PROGRAMMING MODULE CROSS REFERENCE

MODULE NAME	USE WITH
UPP 955	UPP(4)
UPP UP2(2)	UPP 855
PROMPT 975	PROMPT 80/85(3)
PROMPT 475	PROMPT 48(1)
NOTES:	
1. Described on p. 13-34 of 1978 Data Catalog.	
2. Special adaptor socket.	
3. Described on p. 13-39 of 1978 Data Catalog.	
4. Described on p. 13-71 of 1978 Data Catalog.	

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (\AA). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 \AA range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8755A in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure for the 8755A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (\AA). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μ W/cm² power rating. The 8755A should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755A are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755A can be programmed on the Intel® Universal PROM Programmer (UPP), and the PROMPT™ 80/85 and PROMPT-48™ design aids. The appropriate programming modules and adapters for use in programming both 8755A's and 8755's are shown in Table 1.

The program mode itself consists of programming a single address at a time, giving a single 50 msec pulse for every address. Generally, it is desirable to have a verify cycle after a program cycle for the same address as shown in the attached timing diagram. In the verify cycle (i.e., normal memory read cycle) 'V_{DD}' should be at +5V.

Preliminary timing diagrams and parameter values pertaining to the 8755A programming operation are contained in Figure 7.

SYSTEM APPLICATIONS

System Interface with 8085A and 8088

A system using the 8755A can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE₃ and CE₁. By using a combination of unused address lines A₁₁₋₁₅ and the Chip Enable inputs, the 8085A system can use up to 5 each 8755A's without requiring a CE decoder. See Figure 2a and 2b.

If a memory mapped I/O approach is used the 8755A will be selected by the combination of both the Chip Enables and I/O/M using the AD₈₋₁₅ address lines. See Figure 1.

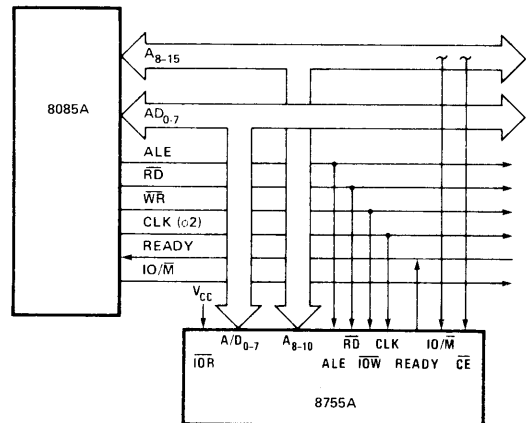
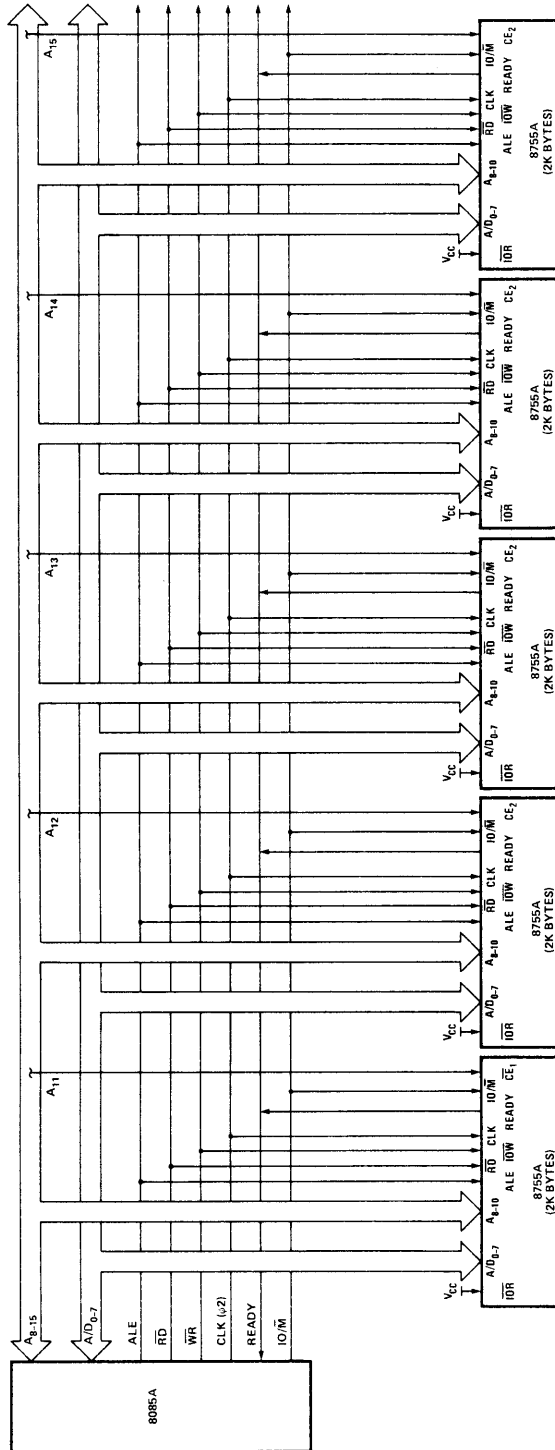


Figure 1. 8755A in 8085A System (Memory-Mapped I/O)



Note: Use \overline{CE}_1 for the first 8755A in the system, and \overline{CE}_2 for the other 8755A's. Permits up to 5 8755A's in a system without CE decoder.

Figure 2b. 8755A in 8085A System (Standard I/O)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5V \pm 5\%$)

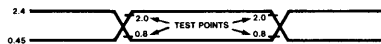
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	V	$V_{CC} = 5.0V$
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2mA$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\mu A$
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$ to 0V
I_{LO}	Output Leakage Current		± 10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	8755A		8755A-2 (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	320		200		ns
T_1	CLK Pulse Width	80		40		ns
T_2	CLK Pulse Width	120		70		ns
$t_{f, tr}$	CLK Rise and Fall Time		30		30	ns
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		45		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		450		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to Write Set Up Time	150		150		ns
t_{WD}	Data In Hold Time After WRITE	30		10		ns
t_{WP}	WRITE to Port Output		400		400	ns
t_{PR}	Port Input Set Up Time	50		50		ns
t_{RP}	Port Input Hold Time	50		50		ns
t_{RYH}	READY HOLD Time	0	160	0	160	ns
t_{ARY}	ADDRESS (CE) to READY		160		160	ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{RDE}	READ Control to Data Bus Enable	10		10		ns
t_{LD}	ALE to Data Out Valid		350		270	ns

Note: $C_{LOAD} = 150pF$

Input Waveform for A.C. Tests:



WAVEFORMS

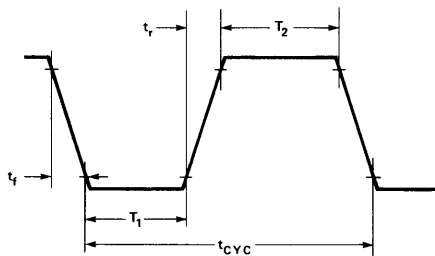


Figure 3. Clock Specification for 8755A

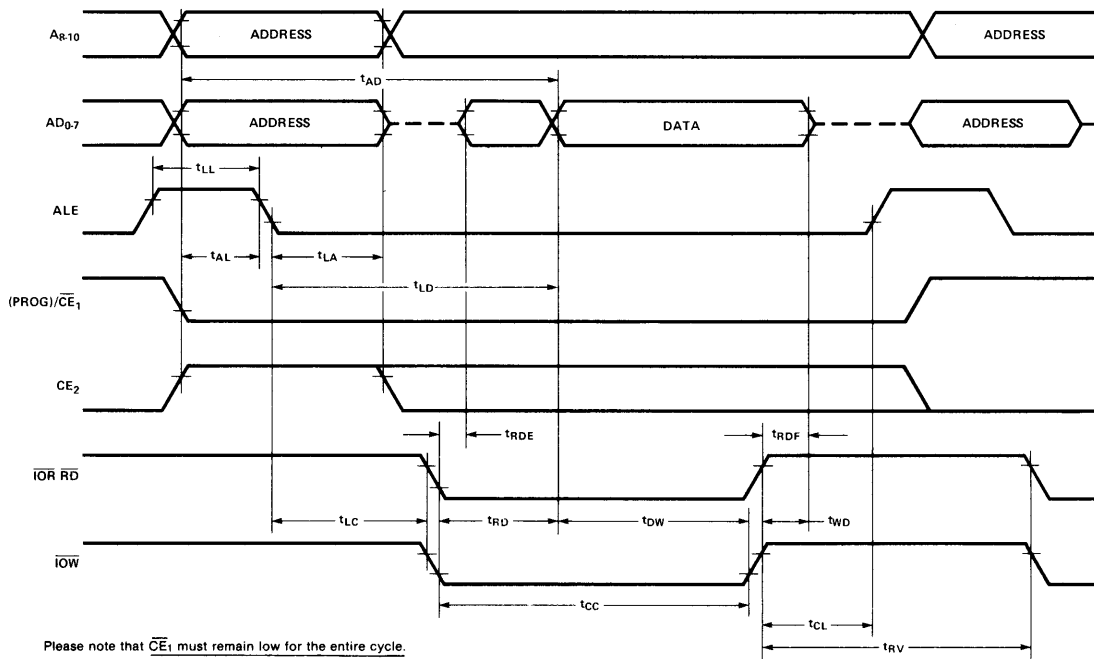


Figure 4. PROM Read, I/O Read and Write Timing

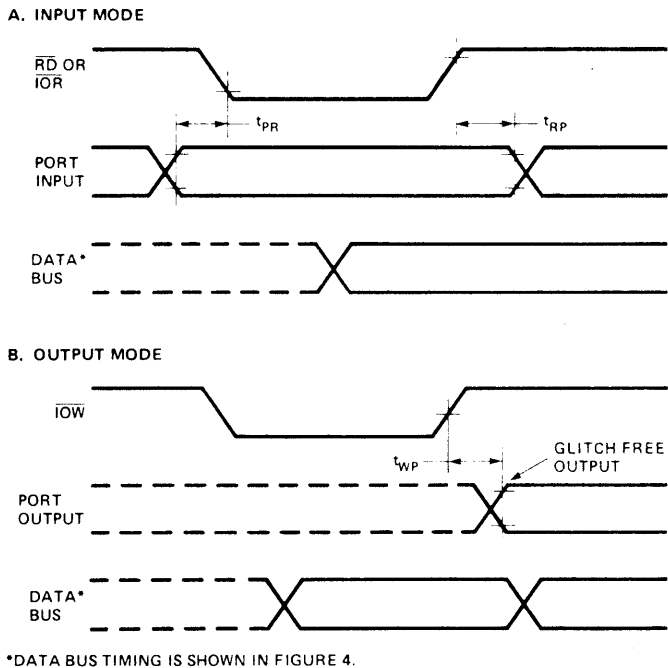


Figure 5. I/O Port Timing

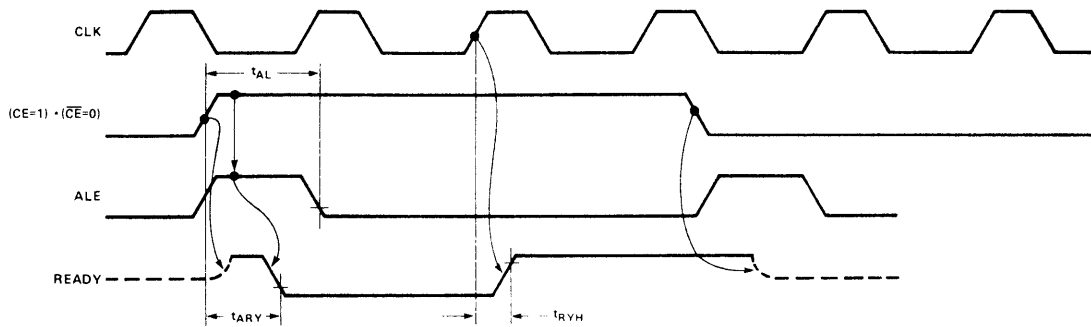


Figure 6. Wait State Timing (READY = 0)

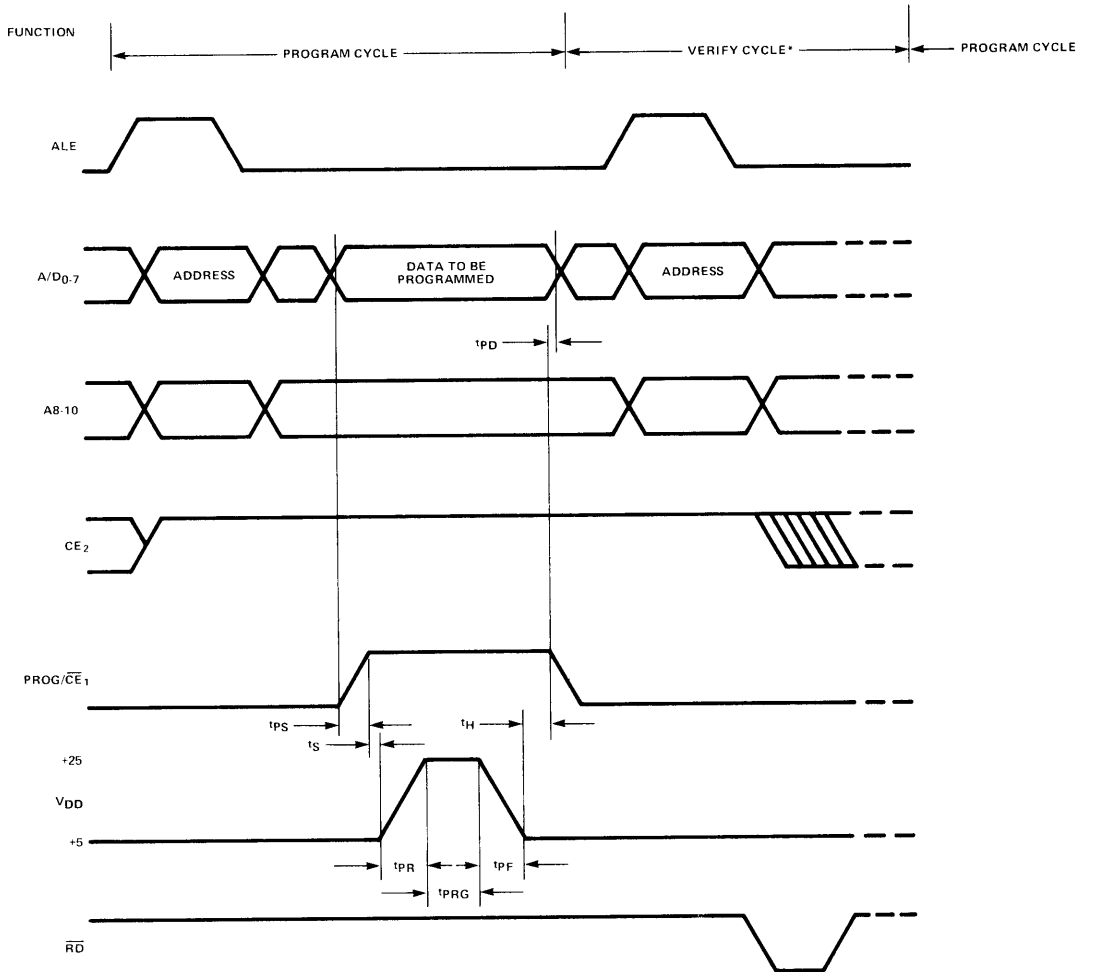
D.C. SPECIFICATION PROGRAMMING(T_A = 0°C to 70°C; V_{CC} = 5V ± 5%; V_{SS} = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Programming Voltage (during Write to EPROM)	24	25	26	V
I _{DD}	Prog Supply Current		15	30	mA

A.C. SPECIFICATION FOR PROGRAMMING(T_A = 0°C to 70°C; V_{CC} = 5V ± 5%; V_{SS} = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t _{PS}	Data Setup Time	10			ns
t _{PD}	Data Hold Time	0			ns
t _S	Prog Pulse Setup Time	2			μs
t _H	Prog Pulse Hold Time	2			μs
t _{PR}	Prog Pulse Rise Time	0.01	2		μs
t _{PF}	Prog Pulse Fall Time	0.01	2		μs
t _{PRG}	Prog Pulse Width	45	50		msec

WAVEFORMS



*VERIFY CYCLE IS A REGULAR MEMORY READ CYCLE (WITH V_{DD} = +5V FOR 8755A)

Figure 7. 8755A Program Mode Timing Diagram

