

## SUMMARY OF 8259A INSTRUCTION SET

Inst. #	Mnemonic	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description		
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	} Format = 4, single, edge triggered Format = 4, single, level triggered Format = 4, not single, edge triggered Format = 4, not single, level triggered No ICW4 Required Format = 8, single, edge triggered Format = 8, single, level triggered Format = 8, not single, edge triggered Format = 8, not single, level triggered		
2	ICW1 B	0	A7	A6	A5	1	1	1	1	0			
3	ICW1 C	0	A7	A6	A5	1	0	1	0	0			
4	ICW1 D	0	A7	A6	A5	1	1	1	0	0			
5	ICW1 E	0	A7	A6	0	1	0	0	1	0			
6	ICW1 F	0	A7	A6	0	1	1	0	1	0			
7	ICW1 G	0	A7	A6	0	1	0	0	0	0			
8	ICW1 H	0	A7	A6	0	1	1	0	0	0			
9	ICW1 I	0	A7	A6	A5	1	0	1	1	1	} Format = 4, single, edge triggered Format = 4, single, level triggered Format = 4, not single, edge triggered Format = 4, not single, level triggered ICW4 Required Format = 8, single, edge triggered Format = 8, single, level triggered Format = 8, not single, edge triggered Format = 8, not single, level triggered		
10	ICW1 J	0	A7	A6	A5	1	1	1	1	1			
11	ICW1 K	0	A7	A6	A5	1	0	1	0	1			
12	ICW1 L	0	A7	A6	A5	1	1	1	0	1			
13	ICW1 M	0	A7	A6	0	1	0	0	1	1			
14	ICW1 N	0	A7	A6	0	1	1	0	1	1			
15	ICW1 O	0	A7	A6	0	1	0	0	0	1			
16	ICW1 P	0	A7	A6	0	1	1	0	0	1			
17	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization		
18	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master		
19	ICW3 S	1	0	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave	
20	ICW4 A	1	0	0	0	0	0	0	0	0	No action, redundant		
21	ICW4 B	1	0	0	0	0	0	0	0	0	1	0	Non-buffered mode, no AEOL, 8086/8088
22	ICW4 C	1	0	0	0	0	0	0	0	1	0	Non-buffered mode, AEOL, MCS-80/85	
23	ICW4 D	1	0	0	0	0	0	0	0	1	1	Non-buffered mode, AEOL, 8086/8088	
24	ICW4 E	1	0	0	0	0	0	0	1	0	0	No action, redundant	
25	ICW4 F	1	0	0	0	0	0	0	1	0	1	Non-buffered mode, no AEOL, 8086/8088	
26	ICW4 G	1	0	0	0	0	0	0	1	1	0	Non-buffered mode, AEOL, MCS-80/85	
27	ICW4 H	1	0	0	0	0	0	0	1	1	1	Non-buffered mode, AEOL, 8086/8088	
28	ICW4 I	1	0	0	0	0	0	1	0	0	0	Buffered mode, slave, no AEOL, MCS-80/85	
29	ICW4 J	1	0	0	0	0	0	1	0	0	1	Buffered mode, slave, no AEOL, 8086/8088	
30	ICW4 K	1	0	0	0	0	0	1	0	1	0	Buffered mode, slave, AEOL, MCS-80/85	
31	ICW4 L	1	0	0	0	0	0	1	0	1	1	Buffered mode, slave, AEOL, 8086/8088	
32	ICW4 M	1	0	0	0	0	0	1	1	0	0	Buffered mode, master, no AEOL, MCS-80/85	
33	ICW4 N	1	0	0	0	0	0	1	1	0	1	Buffered mode, master, no AEOL, 8086/8088	
34	ICW4 O	1	0	0	0	0	0	1	1	1	0	Buffered mode, master, AEOL, MCS-80/85	
35	ICW4 P	1	0	0	0	0	0	1	1	1	1	Buffered mode, master AEOL, 8086, 8088	
36	ICW4 NA	1	0	0	0	0	1	0	0	0	0	Fully nested mode, MCS-80, non buffered, no AEOL	
37	ICW4 NB	1	0	0	0	0	1	0	0	0	1	} ICW4 NB through ICW4 ND are identical to ICW4 B through ICW4 D with the addition of Fully Nested Mode	
38	ICW4 NC	1	0	0	0	0	1	0	0	1	0		
39	ICW4 ND	1	0	0	0	0	1	0	0	1	1		
40	ICW4 NE	1	0	0	0	0	1	0	1	0	0		Fully Nested Mode, MCS-80/85, non-buffered, no AEOL
41	ICW4 NF	1	0	0	0	0	1	0	1	0	1	} ICW4 NF through ICW4 NP are identical to ICW4 F through ICW4 P with the addition of Fully Nested Mode	
42	ICW4 NG	1	0	0	0	0	1	0	1	1	0		
43	ICW4 NH	1	0	0	0	0	1	0	1	1	1		
44	ICW4 NI	1	0	0	0	0	1	1	0	0	0		
45	ICW4 NJ	1	0	0	0	0	1	1	0	0	1		
46	ICW4 NK	1	0	0	0	0	1	1	0	1	0		
47	ICW4 NL	1	0	0	0	0	1	1	0	1	1		
48	ICW4 NM	1	0	0	0	0	1	1	1	0	0		
49	ICW4 NN	1	0	0	0	0	1	1	1	0	1		
50	ICW4 NO	1	0	0	0	0	1	1	1	1	0		
51	ICW4 NP	1	0	0	0	0	1	1	1	1	1		
52	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask register, read mask register		
53	OCW2 E	0	0	0	1	0	0	0	0	0	0	Non-specific EOI	
54	OCW2 SE	0	0	0	1	1	0	0	L2	L1	L0	Specific EOI, LO-L2 code of IS FF to be reset	
55	OCW2 RE	0	1	0	1	0	0	0	0	0	0	Rotate on Non-Specific EOI	
56	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate on Specific EOI LO-L2 code of line		
57	OCW2 R	0	1	0	0	0	0	0	0	0	0	Rotate in Auto EOI (set)	
58	OCW2 CR	0	0	0	0	0	0	0	0	0	0	Rotate in Auto EOI (clear)	
59	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	Set Priority Command		
60	OCW3 P	0	0	0	0	0	0	1	1	0	0	Poll mode	
61	OCW3 RIS	0	0	0	0	0	0	1	0	1	1	Read IS register	

SUMMARY OF 8259A INSTRUCTION SET (Cont.)

Inst. #	Mnemonic	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description	
46	OCW3 RR	0	0	0	0	0	0	1	0	1	0	Read request register
47	OCW3 SM	0	0	1	1	0	1	0	0	0	0	Set special mask mode
48	OCW3 RSM	0	0	1	0	0	1	0	0	0	0	Reset special mask mode

Note: 1. In the master mode  $\overline{SP}$  pin = 1, in slave mode  $\overline{SP}$  = 0

Cascading

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

A typical MCS-80/85 system is shown in Figure 2. The master controls, through the 3 line cascade bus, which one of the slaves will release the corresponding address.

As shown in Figure 2, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave

to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. It is obvious that each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ( $\overline{CS}$ ) input of each 8259A.

The cascade lines of the Master 8259A are activated for any interrupt input, even if no slave is connected to that input.

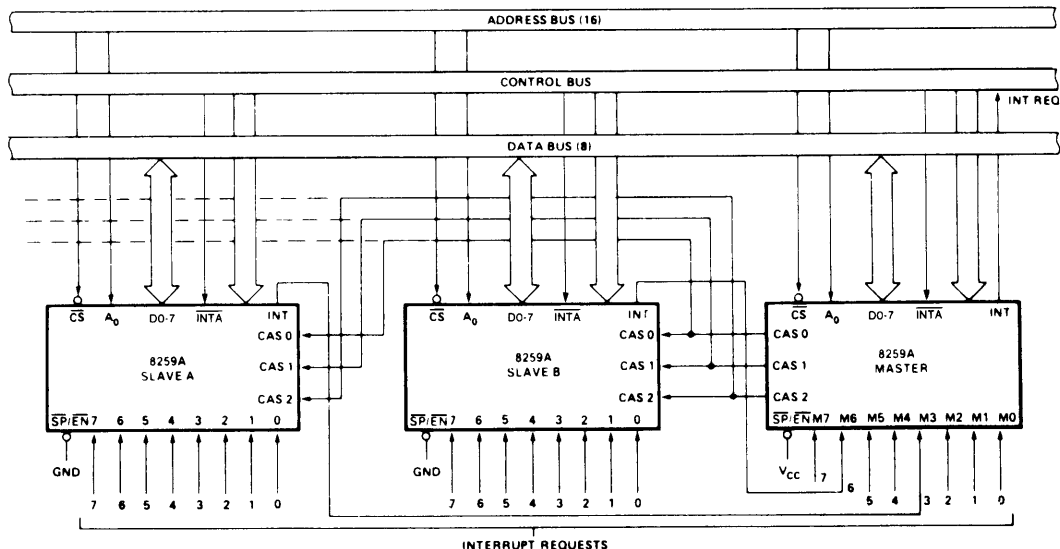


Figure 2. Cascading the 8259A

## PIN FUNCTIONS

NAME	I/O	PIN#	FUNCTION				
V <sub>CC</sub>	I	28	+5v supply	INT	0	17	Interrupt: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
GND	I	14	Ground				
$\overline{CS}$	I	1	Chip Select A low on this pin enables RD and WR communication between the CPU and the 8259A. INTA functions are independent of CS.	IR <sub>0</sub> -IR <sub>7</sub>	I	18-25	Interrupt Requests: Asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{WR}$	I	2	Write: A low on this pin when CS is low, enables the 8259A to accept command words from the CPU.				
$\overline{RD}$	I	3	Read: A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.	$\overline{INTA}$	I	26	Interrupt Acknowledge: This pin is used to enable 8259A interrupt-vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
D <sub>7</sub> -D <sub>0</sub>	I/O	4-11	Bidirectional Data Bus: Control, status and interrupt-vector information is transferred via this bus.	A <sub>0</sub>	I	27	A0 Address Line: This pin acts in conjunction with the $\overline{CS}$ , $\overline{WR}$ , and $\overline{RD}$ pins. It is used by the 8259A to decipher between various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086/8088).
CAS <sub>0</sub> -CAS <sub>2</sub>	I/O	12,13,15	Cascade Lines: The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.				
$\overline{SP}/\overline{EN}$	I/O	16	Slave Program/Enable Buffer: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).				

## ABSOLUTE MAXIMUM RATINGS\*

Ambient Temperature Under Bias . . . . . - 40°C to 85°C  
Storage Temperature . . . . . - 65°C to + 150°C  
Voltage On Any Pin

With Respect to Ground . . . . . - 0.5V to + 7V  
Power Dissipation . . . . . 1 Watt

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## D.C. CHARACTERISTICS

T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ± 10% (8259-A), V<sub>CC</sub> = 5V ± 10% (8259A)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-.5	V		
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + .5V	V	
V <sub>OL</sub>	Output Low Voltage		.45	V	I <sub>OL</sub> = 2.2 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = - 400 μA
V <sub>OH(INT)</sub>	Interrupt Output High Voltage	3.5 2.4		C V	I <sub>OH</sub> = - 100 μA I <sub>OH</sub> = - 400 μA
I <sub>LI</sub>	Input Load Current		10	μA	V <sub>IN</sub> = V <sub>CC</sub> to 0V
I <sub>LOL</sub>	Output Leakage Current		-10	μA	V <sub>OUT</sub> = 0.45V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current		85	mA	
I <sub>LIR</sub>	IR Input Load Current		-300 10	μA μA	V <sub>IN</sub> = 0 V <sub>IN</sub> = V <sub>CC</sub>

**8259A A.C. CHARACTERISTICS**
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$   $V_{CC} = 5V \pm 5\%$  (8259A-8)  $V_{CC} = 5V \pm 10\%$  (8259A)
**TIMING REQUIREMENTS**

Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TAHRL	AO/ $\overline{\text{CS}}$ Setup to $\overline{\text{RD}}$ / $\overline{\text{INTA}}$	50		0		0		ns	
TRHAX	AO/ $\overline{\text{CS}}$ Hold after $\overline{\text{RD}}$ / $\overline{\text{INTA}}$	5		0		0		ns	
TRLRH	$\overline{\text{RD}}$ Pulse Width	420		235		160		ns	
TAHWL	AO/ $\overline{\text{CS}}$ Setup to $\overline{\text{WR}}$	50		0		0		ns	
TWHAX	AO/ $\overline{\text{CS}}$ Hold after $\overline{\text{WR}}$	20		0		0		ns	
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		290		190		ns	
TDVWH	Data Setup to $\overline{\text{WR}}$	300		240		160		ns	
TWHDX	Data Hold after $\overline{\text{WR}}$	40		0		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{\text{INTA}}$ (Slave Only)	55		55		40		ns	
TRHRL	End of $\overline{\text{RD}}$ to Next Command	160		160		160		ns	
TWHRL	End of $\overline{\text{WR}}$ to Next Command	190		190		190		ns	

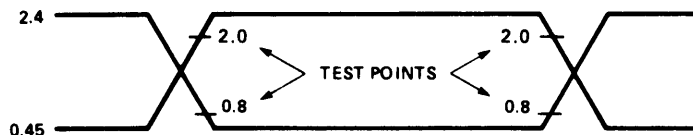
Note: This is the low time required to clear the input latch in the edge triggered mode.

**TIMING RESPONSES**

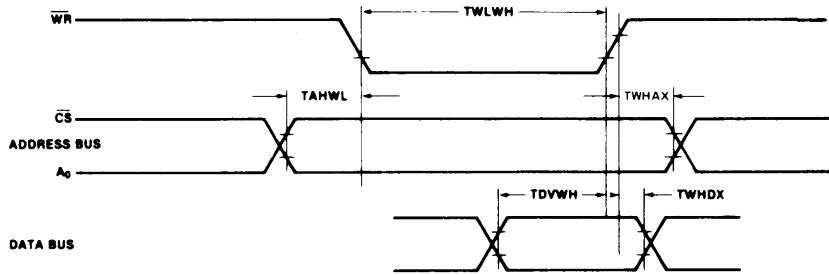
Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TRLDV	Data Valid from $\overline{\text{RD}}$ / $\overline{\text{INTA}}$		300		200		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{\text{RD}}$ / $\overline{\text{INTA}}$	10	200		100		85	ns	C of Data Bus Max test C = 100 pF Min. test C = 15 pF
TJHIH	Interrupt Output Delay		400		350		300	ns	Min. test C = 15 pF
TIAHCV	Cascade Valid from First $\overline{\text{INTA}}$ (Master Only)		565		565		360	ns	$C_{\text{INT}} = 100$ pF
TRLEL	Enable Active from $\overline{\text{RD}}$ or $\overline{\text{INTA}}$		160		125		100	ns	$C_{\text{CASCADE}} = 100$ pF
TRHEH	Enable Inactive from $\overline{\text{RD}}$ or $\overline{\text{INTA}}$		325		150		d150	ns	
TAHDV	Data Valid from Stable Address		350		200		200	ns	
TCVDV	Cascade Valid to Valid Data		300		300		200	ns	

**CAPACITANCE**
 $T_A = 25^\circ\text{C}$ ;  $V_{CC} = \text{GND} = 0V$ 

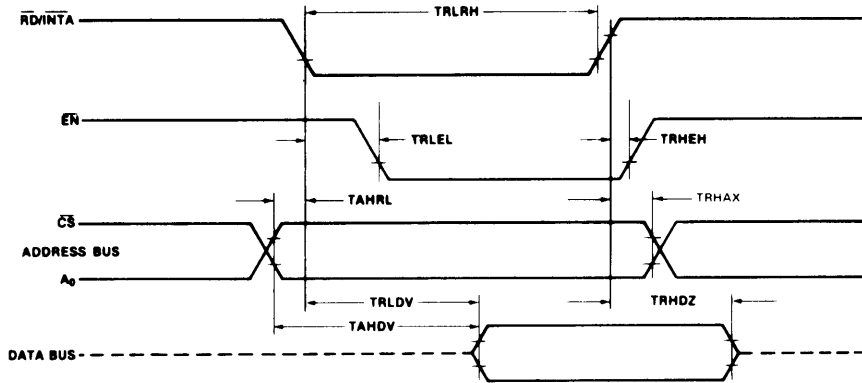
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{\text{IN}}$	Input Capacitance			10	pF	$f_c = 1$ MHz
$C_{\text{I/O}}$	I/O Capacitance			20	pF	Unmeasured pins returned to $V_{SS}$

**Input and Output Waveforms for A.C. Tests**

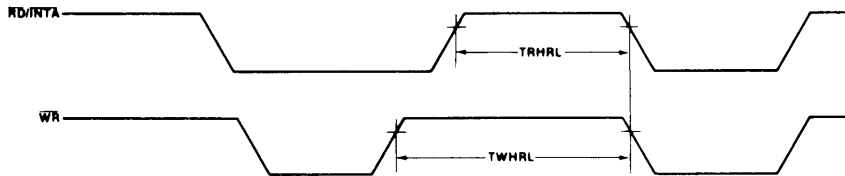
**WRITE MODE**



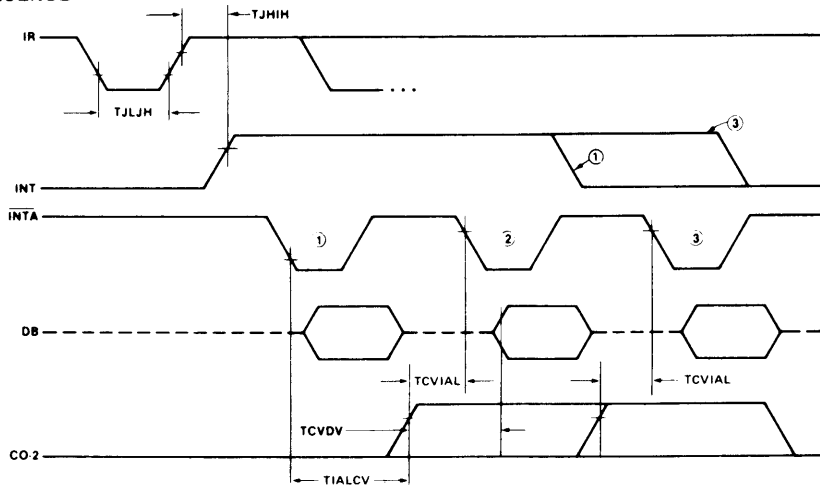
**READ/INTA MODE**



**OTHER TIMING**



**INTA SEQUENCE**

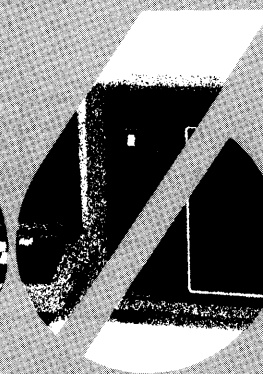
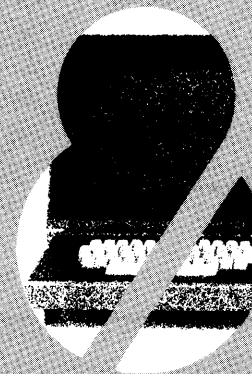
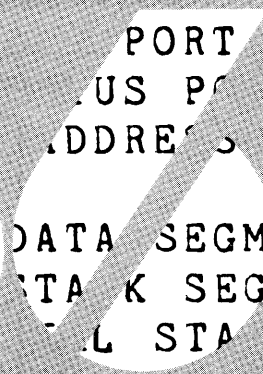
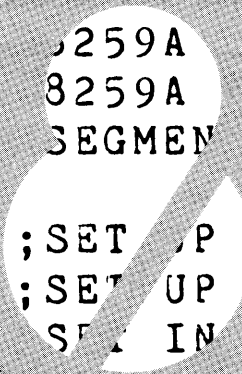
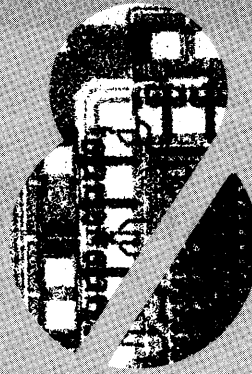


NOTE: Interrupt output must remain HIGH until leading edge of first INTA.  
 ② MCS 8259 Systems only.  
 ③ Cycle 1 in MCS 88 Systems the Data Bus is not active.



## Appendix B Device Specifications

- 8086 Family
- **8085 Peripherals\***
- Standard Peripherals\*\*
- RAM Memories\*\*\*
- EPROM Memories\*\*\*
- Development Tools





# 8155/8156/8155-2/8156-2

## 2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

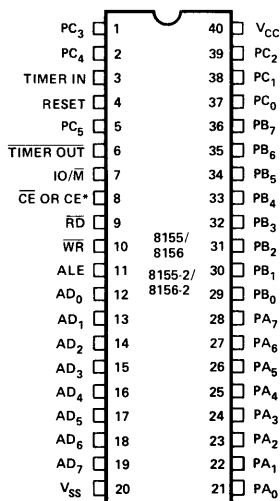
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 89156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

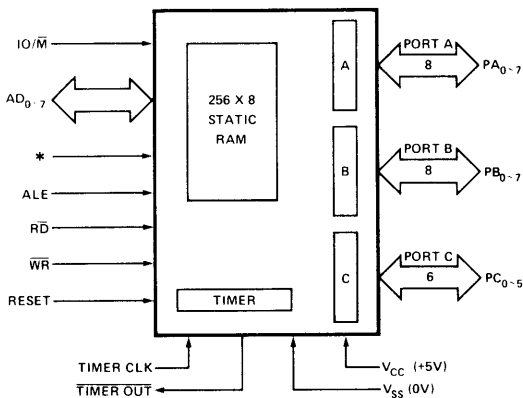
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

### PIN CONFIGURATION



### BLOCK DIAGRAM



\*: 8155/8155-2 =  $\overline{CE}$ , 8156/8156-2 = CE



**PRELIMINARY**  
 Notice: This is not a final specification. Some parametric limits are subject to change.

# 8185/8185-2

## 1024 x 8-BIT STATIC RAM FOR MCS-85™

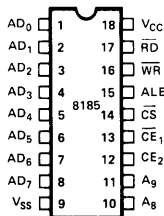
- Multiplexed Address and Data Bus
- Low Standby Power Dissipation
- Directly Compatible with 8085A and 8088 Microprocessors
- Single +5V Supply
- Low Operating Power Dissipation
- High Density 18-Pin Package

The Intel® 8185 is an 8192-bit static random access memory (RAM) organized as 1024 words by 8-bits using N-channel Silicon-Gate MOS technology. The multiplexed address and data bus allows the 8185 to interface directly to the 8085A and 8088 microprocessors to provide a maximum level of system integration.

The low standby power dissipation minimizes system power requirements when the 8185 is disabled.

The 8185-2 is a high-speed selected version of the 8185 that is compatible with the 5 MHz 8085A-2 and the full speed 5 MHz 8088.

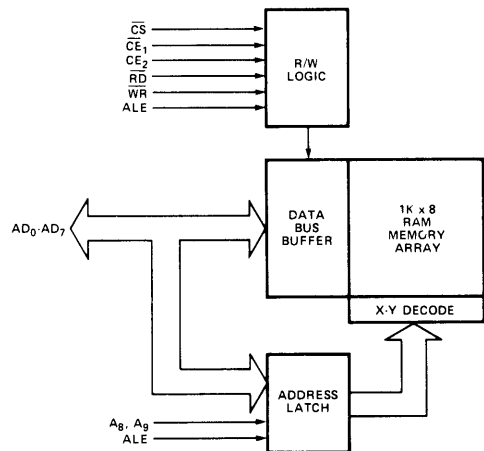
### PIN CONFIGURATION



### PIN NAMES

AD <sub>0</sub> -AD <sub>7</sub>	ADDRESS/DATA LINES
A <sub>8</sub> , A <sub>9</sub>	ADDRESS LINES
CS	CHIP SELECT
CE <sub>1</sub>	CHIP ENABLE (IO/M)
CE <sub>2</sub>	CHIP ENABLE
ALE	ADDRESS LATCH ENABLE
RD	READ ENABLE
WR	WRITE ENABLE

### BLOCK DIAGRAM





## 8355/8355-2 16,384-BIT ROM WITH I/O

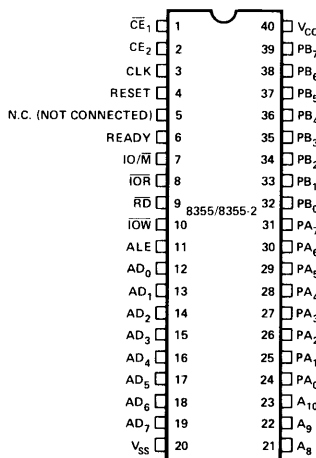
- 2048 Words x 8 Bits
- Single +5V Power Supply
- Directly compatible with 8085A and 8088 Microprocessors
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- Internal Address Latch
- 40-Pin DIP

The Intel® 8355 is a ROM and I/O chip to be used in the 8085A and 8088 microprocessor systems. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 400 ns to permit use with no wait states in the 8085A CPU.

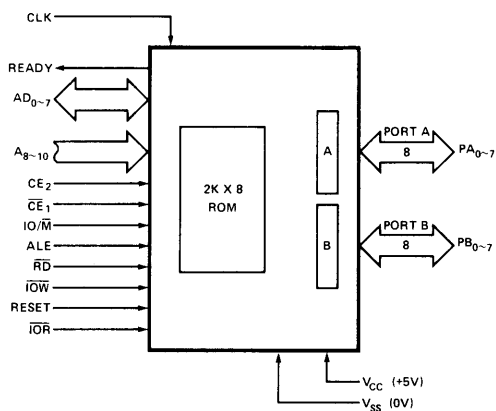
The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines and each I/O port line is individually programmable as input or output.

The 8355-2 has a 300ns access time for compatibility with the 8085A-2 and full speed 5 MHz 8088 microprocessors.

### PIN CONFIGURATION



### BLOCK DIAGRAM





## 8755A / 8755A-2 16,384-BIT EPROM WITH I/O

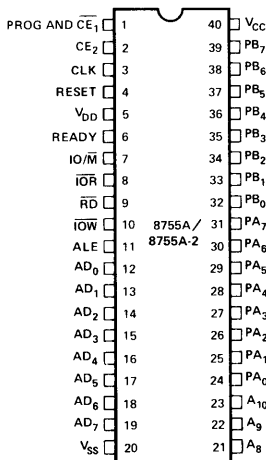
- 2048 Words × 8 Bits
- Single +5V Power Supply ( $V_{CC}$ )
- Directly Compatible with 8085A and 8088 Microprocessors
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP

The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085A and 8088 microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A CPU.

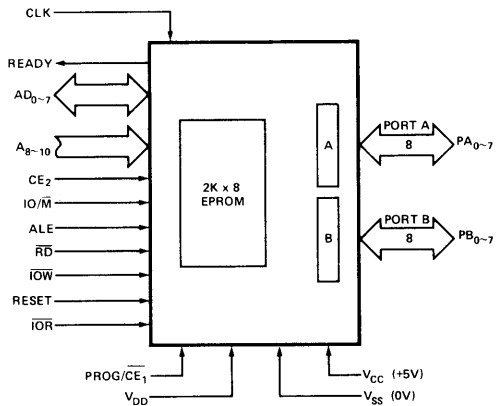
The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

The 8755A-2 is a high speed selected version of the 8755A compatible with the 5 MHz 8085A-2 and the full speed 5 MHz 8088.

PIN CONFIGURATION



BLOCK DIAGRAM





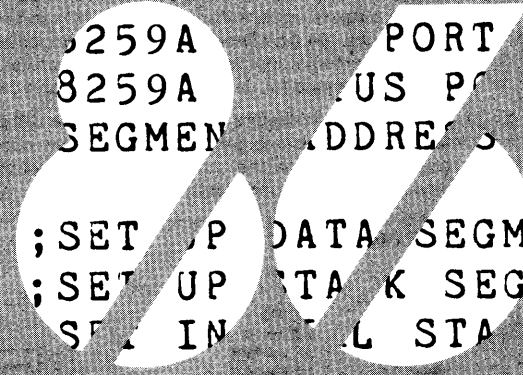
## Appendix B Device Specifications

- 8086 Family
- 8085 Peripherals\*
- **Standard Peripherals\*\***
- RAM Memories\*\*\*
- EPROM Memories\*\*\*
- Development Tools

\*For complete specifications refer to the Intel MCS-85 User's Manual.

\*\*For complete specifications refer to the Intel Peripheral Design Handbook.

\*\*\*For complete specifications refer to the 1979 Intel Component Data Catalog.





# 8041A/8641A/8741A UNIVERSAL PERIPHERAL INTERFACE 8-BIT MICROCOMPUTER

- 8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package
- One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- DMA, Interrupt, or Polled Operation Supported
- 1024 x 8 ROM/EPROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins
- Fully Compatible with MCS-48™, MCS-80™, MCS-85™, and MCS-86™ Microprocessor Families
- Interchangeable ROM and EPROM Versions
- 3.6 MHz 8741A-8 Available
- Expandable I/O
- RAM Power-Down Capability
- Over 90 Instructions: 70% Single Byte
- Single 5V Supply

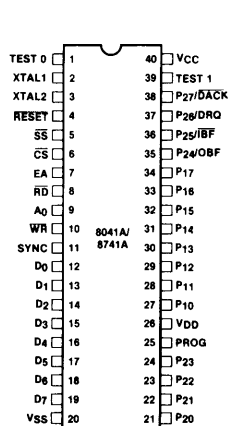
The Intel® 8041A/8741A is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-48™, MCS-80™, MCS-85™, MCS-86™, and other 8-bit systems.

The UPI-41A™ has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041A version or as UV-erasable EPROM in the 8741A version. The 8741A and the 8041A are fully pin compatible for easy transition from prototype to production level designs. The 8641A is a one-time programmable (at the factory) 8741A which can be ordered as the first 25 pieces of a new 8041A order. The substitution of 8641A's for 8041A's allows for very fast turnaround for initial code verification and evaluation results.

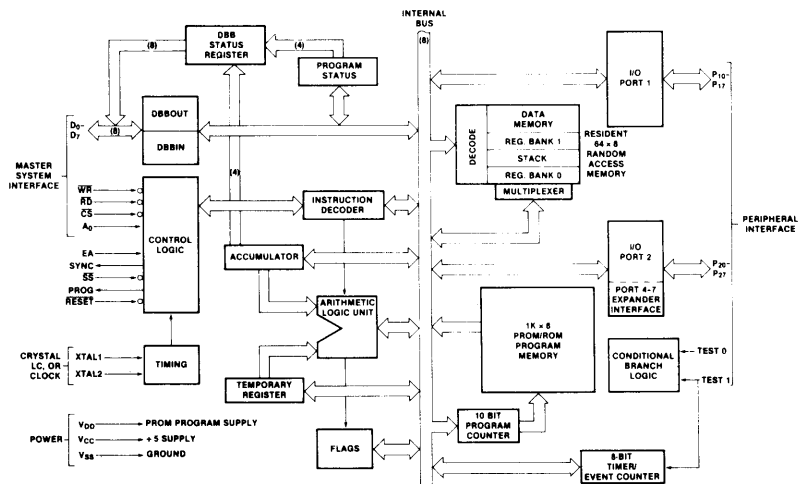
The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041A), single-step mode for debug (in the 8741A), and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

## PIN CONFIGURATION



## BLOCK DIAGRAM





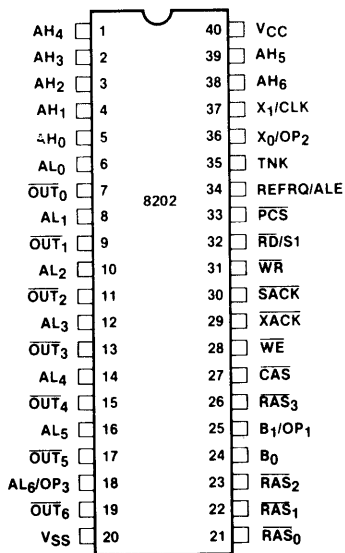
**PRELIMINARY**  
Notice: This is not a final specification. Some parametric limits are subject to change.

# 8202 DYNAMIC RAM CONTROLLER

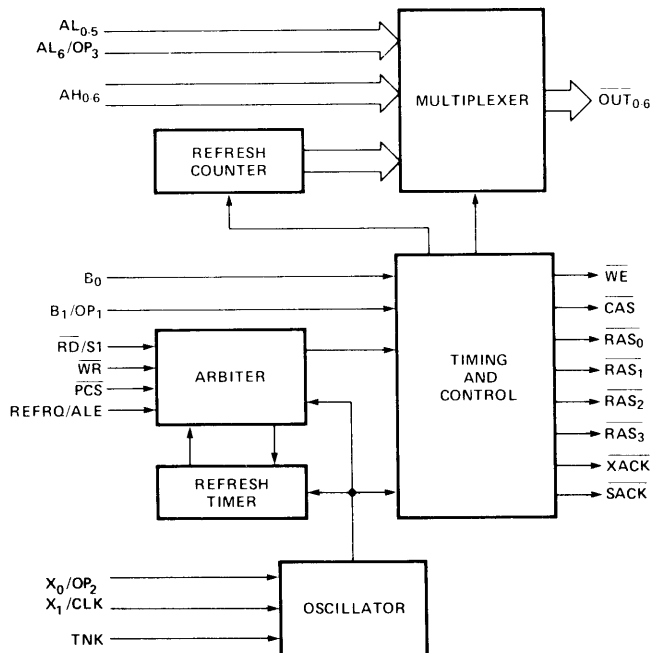
- Provides All Signals Necessary to Control 2104A, 2117, or 2118 Dynamic Memories
- Directly Addresses and Drives Up to 128K Bytes Without External Drivers
- Provides Address Multiplexing and Strobes
- Provides a Refresh Timer and a Refresh Counter
- Refresh Cycles May be Internally or Externally Requested
- Provides Transparent Refresh Capability
- Fully Compatible with Intel® 8080A, 8085A and 8086 Microprocessors
- Decodes 8085A Status for Advanced Read Capability
- Provides System Acknowledge and Transfer Acknowledge Signals
- Internal or External Clock Capability

The 8202 is a Dynamic RAM System Controller designed to provide all signals necessary to use 2104A, 2117, or 2118 Dynamic RAMs in microcomputer systems. The 8202 provides multiplexed addresses and address strobes, as well as refresh/access arbitration. Refresh cycles can be started internally or externally.

PIN CONFIGURATION



8202 BLOCK DIAGRAM





# 8205

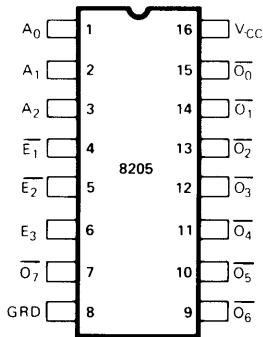
## HIGH SPEED 1 OUT OF 8 BINARY DECODER

- I/O Port or Memory Selector
- Simple Expansion — Enable Inputs
- High Speed Schottky Bipolar Technology — 18ns Max. Delay
- Directly Compatible with TTL Logic Circuits
- Low Input Load Current — .25 mA max., 1/6 Standard TTL Input Load
- Minimum Line Reflection — Low Voltage Diode Input Clamp
- Outputs Sink 10 mA min.
- 16-Pin Dual-In-Line Ceramic or Plastic Package

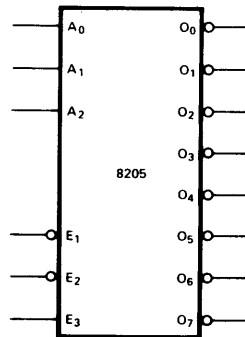
The 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive eight other decoders for arbitrary memory expansions.

The Intel<sup>®</sup> 8205 is packaged in a standard 16 pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A <sub>0</sub> , A <sub>2</sub>	ADDRESS INPUTS
E <sub>1</sub> , E <sub>2</sub>	ENABLE INPUTS
O <sub>0</sub> , O <sub>7</sub>	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	E <sub>1</sub>	E <sub>2</sub>	E <sub>3</sub>	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H



# 8251A

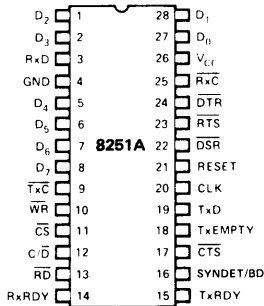
## PROGRAMMABLE COMMUNICATION INTERFACE

**PRELIMINARY**  
 Notice: This is not a final specification. Some parametric limits are subject to change.

- Synchronous and Asynchronous Operation
- Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion
- Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling.
- Synchronous Baud Rate — DC to 64K Baud
- Asynchronous Baud Rate — DC to 19.2K Baud
- Full Duplex, Double Buffered, Transmitter and Receiver
- Error Detection — Parity, Overrun and Framing
- Fully Compatible with 8080/8085 CPU
- 28-Pin DIP Package
- All Inputs and Outputs are TTL Compatible
- Single +5V Supply
- Single TTL Clock

The Intel® 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

### PIN CONFIGURATION

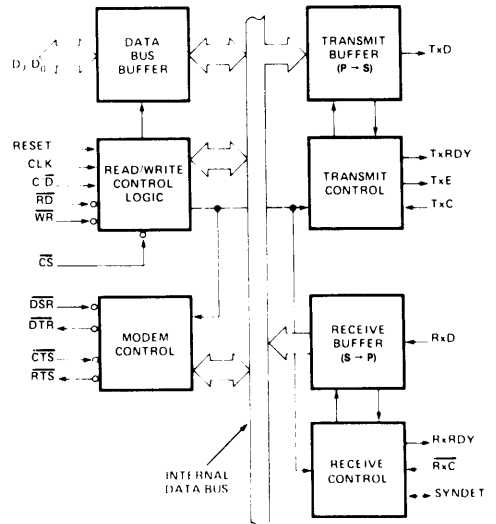


### PIN NAMES

D <sub>7</sub> D <sub>0</sub>	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V <sub>CC</sub>	+5 Volt Supply
GND	Ground

### BLOCK DIAGRAM





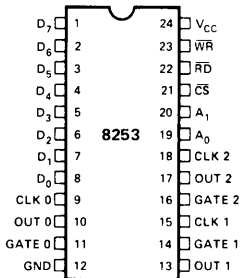
# 8253/8253-5 PROGRAMMABLE INTERVAL TIMER

- MCS—85™ Compatible 8253-5
  - 3 Independent 16-Bit Counters
  - DC to 2 MHz
  - Programmable Counter Modes
- Count Binary or BCD
  - Single +5V Supply
  - 24-Pin Dual In-Line Package

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

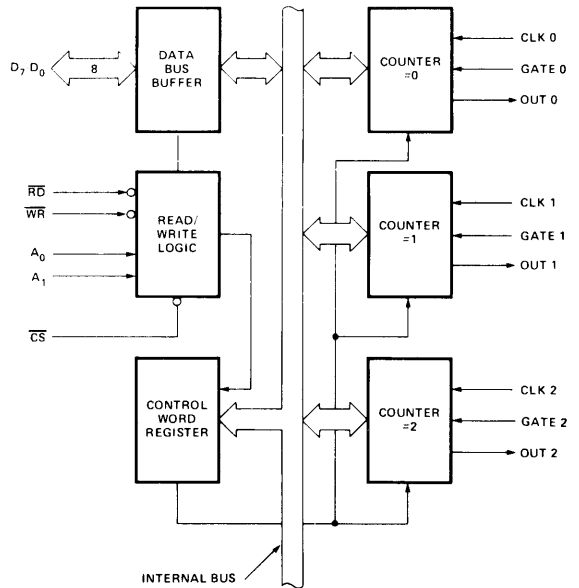
### PIN CONFIGURATION



### PIN NAMES

D <sub>7</sub> , D <sub>0</sub>	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
RD	READ COUNTER
WR	WRITE COMMAND OR DATA
CS	CHIP SELECT
A <sub>0</sub> , A <sub>1</sub>	COUNTER SELECT
V <sub>CC</sub>	+5 VOLTS
GND	GROUND

### BLOCK DIAGRAM



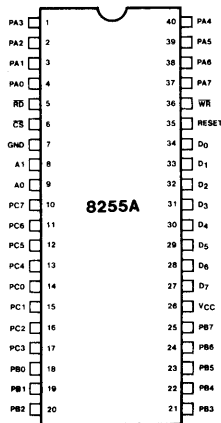


# 8255A/8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

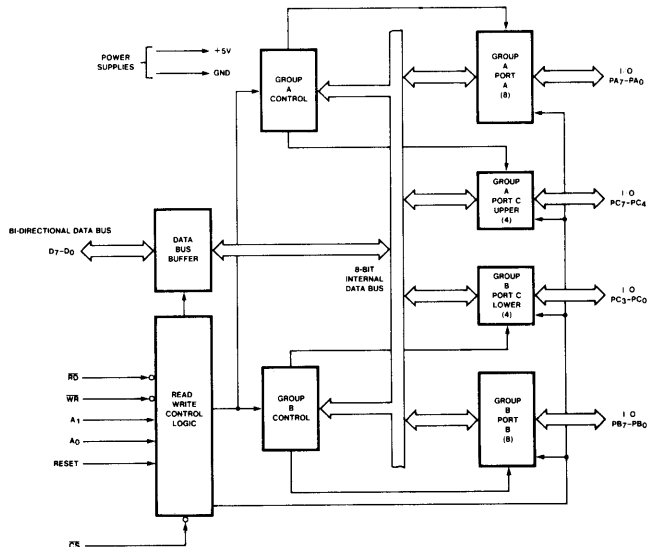
### PIN CONFIGURATION



### PIN NAMES

D <sub>7</sub> -D <sub>0</sub>	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A <sub>0</sub> , A <sub>1</sub>	PORT ADDRESS
PA <sub>7</sub> -PA <sub>0</sub>	PORT A (BIT)
PB <sub>7</sub> -PB <sub>0</sub>	PORT B (BIT)
PC <sub>7</sub> -PC <sub>0</sub>	PORT C (BIT)
V <sub>CC</sub>	+5 VOLTS
GND	0 VOLTS

### 8255A BLOCK DIAGRAM



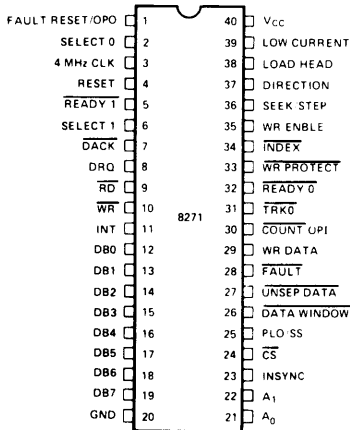


# 8271/8271-6/8271-8 PROGRAMMABLE FLOPPY DISK CONTROLLER

- IBM 3740 Soft Sected Format Compatible
- Programmable Record Lengths
- Multi-Sector Capability
- Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives
- Automatic Read/Write Head Positioning and Verification
- Internal CRC Generation and Checking
- Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count
- Fully MCS-80™ and MCS-85™ Compatible
- Single +5V Supply
- 40-Pin Package

The Intel® 8271 Programmable Floppy Disk Controller (FDC) is an LSI component designed to interface one to 4 floppy disk drives to an 8-bit microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk controllers.

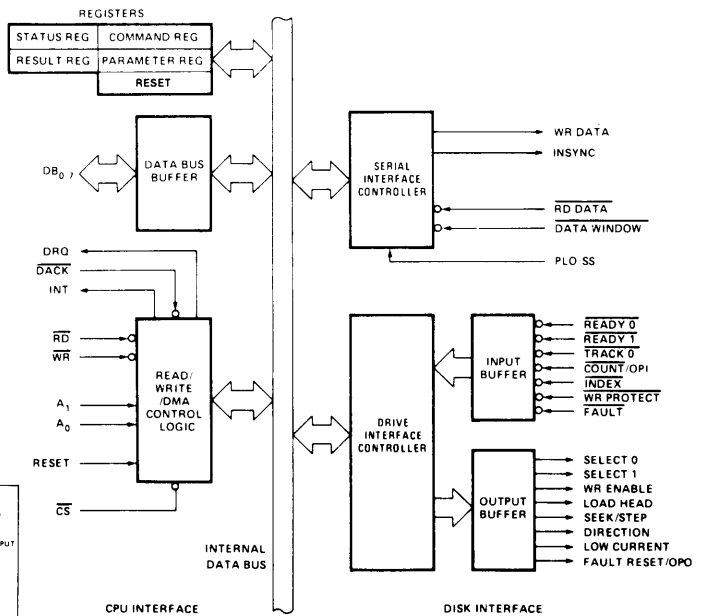
## PIN CONFIGURATION



## PIN NAMES

DB <sub>7</sub> - DB <sub>0</sub>	DATA BUS (BI DIRECTIONAL): CLOCK INPUT (ITL)	PLO/SS DATA WINDOW	PLO/SINGLE SHOT DATA WINDOW
SELECT 1, 0	SELECT 1, 0	UNSEP DATA	UNSEPARATED DATA
FAULT RESET/OPO	CHIP RESET	FAULT	FAULT
RESET	READY 1, 0	WR DATA	WRITE DATA
READY 1, 0	CPU READ INPUT	COUNT/OPI	COUNT/OPTIONAL INPUT
DACK	DMA ACKNOWLEDGE	TRK 0	TRACK 0
DRQ	DMA REQUEST	WR PROTECT	WRITE PROTECT
WR	CPU WRITE INPUT	INDEX	INDEX
RD	INTERRUPT	WR ENBLE	WRITE ENBLE
INT	REGISTER SELECT	SEEK STEP	SEEK STEP
A <sub>1</sub> , 0	READ DATA INSYNC	DIRECTION	DIRECTION
INSYNC	CHIP SELECT	LOAD HEAD	LOAD HEAD
CS		LOW CURRENT	LOW CURRENT

## BLOCK DIAGRAM





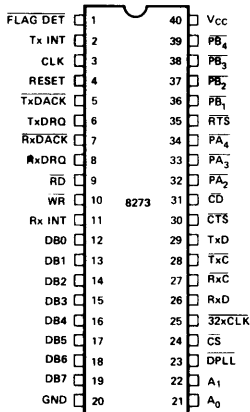
**PRELIMINARY**  
 Notice: This is not a final specification. Some parametric limits are subject to change.

# 8273 PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

- HDLC/SDLC Compatible
- Frame Level Commands
- Full Duplex, Half Duplex, or Loop SDLC Operation
- Up to 64K Baud Transfers
- Two User Programmable Modem Control Ports
- Automatic FCS (CRC) Generation and Checking
- Programmable NRZI Encode/Decode
- N-Bit Reception Capability
- Digital Phase Locked Loop Clock Recovery
- Minimum CPU Overhead
- Fully Compatible with 8080/8085 CPUs
- Single +5V Supply
- 40-Pin Package

The Intel® 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/CITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS-85™. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.

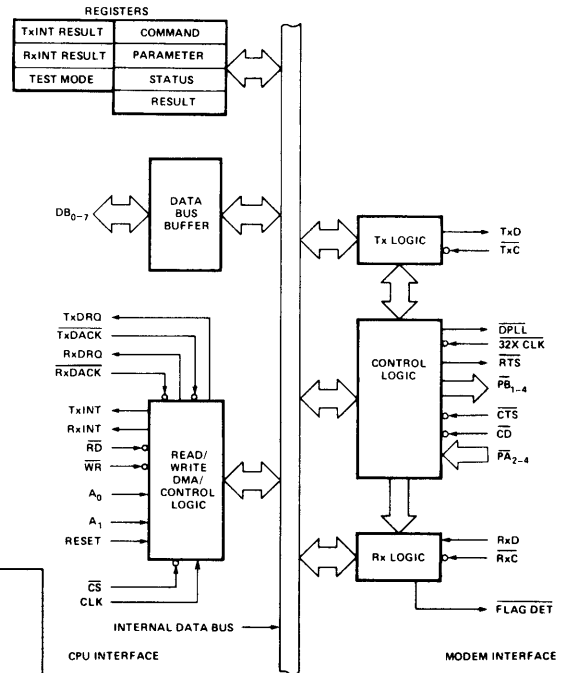
### PIN CONFIGURATION



### PIN NAMES

DB0-DB7	DATA BUS (8 BITS)	CS	CHIP SELECT
FLAG DET	FLAG DETECT	32xCLK	32 TIMES CLOCK
TxINT	TRANSMITTER INTERRUPT	RxD	RECEIVER DATA
CLK	CLOCK INPUT	RxC	RECEIVER CLOCK
RESET	RESET	TxC	TRANSMITTER CLOCK
TxDACK	TRANSMITTER DMA ACKNOWLEDGE	TxD	TRANSMITTER DATA
TxDRQ	TRANSMITTER DMA REQUEST	CTS	CLEAR TO SEND
RD	READ INPUT	CD	CARRIER DETECT
WR	WRITE INPUT	PA2-PA4	GP INPUT PORTS
RxDACK	RECEIVER DMA ACKNOWLEDGE	PB1-PB4	GP OUTPUT PORTS
RxDRQ	RECEIVER DMA REQUEST	RTS	REQUEST TO SEND
RxINT	RECEIVER INTERRUPT	Vcc	+5 VOLT SUPPLY
AD-A1	COMMAND REGISTER SELECT ADDRESS	GND	GROUND
DPLL	DIGITAL PHASE LOCKED LOOP		

### BLOCK DIAGRAM



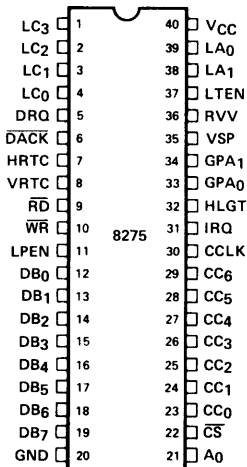


# 8275 PROGRAMMABLE CRT CONTROLLER

- Programmable Screen and Character Format
- 6 Independent Visual Field Attributes
- 11 Visual Character Attributes (Graphic Capability)
- Cursor Control (4 Types)
- Light Pen Detection and Registers
- Fully MCS-80™ and MCS-85™ Compatible
- Dual Row Buffers
- Programmable DMA Burst Mode
- Single +5V Supply
- 40-Pin Package

The Intel® 8275 Programmable CRT Controller is a single chip device to interface CRT raster scan displays with Intel® microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

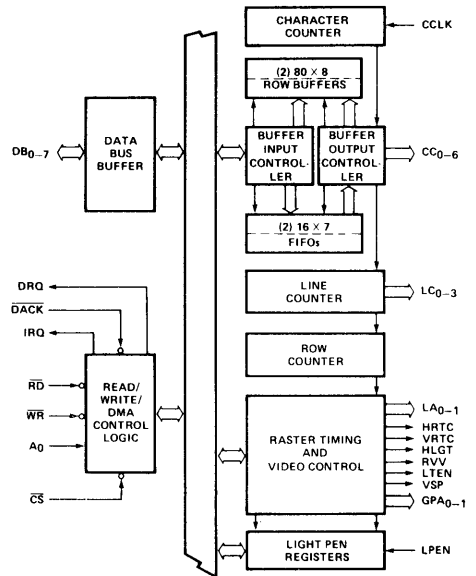
### PIN CONFIGURATION



### PIN NAMES

DB <sub>0-1</sub>	B1- DIRECTIONAL DATA BUS	LC <sub>0-3</sub>	LINE COUNTER OUTPUTS
DRQ	DMA REQUEST OUTPUT	LA <sub>0-1</sub>	LINE ATTRIBUTE OUTPUTS
DACK	DMA ACKNOWLEDGE INPUT	HRTC	HORIZONTAL RETRACE OUTPUT
IRQ	INTERRUPT REQUEST OUTPUT	VRTC	VERTICAL RETRACE OUTPUT
RD	READ STROBE INPUT	HLGT	HIGHLIGHT OUTPUT
WR	WRITE STROBE INPUT	RVV	REVERSE VIDEO OUTPUT
A <sub>0</sub>	REGISTER ADDRESS INPUT	LTEN	LIGHT ENABLE OUTPUT
CS	CHIP SELECT INPUT	VSP	VIDEO SUPPRESS OUTPUT
CCLK	CHARACTER CLOCK INPUT	GPA <sub>0-1</sub>	GENERAL PURPOSE ATTRIBUTE OUTPUTS
CC <sub>0-6</sub>	CHARACTER CODE OUTPUTS	LPEN	LIGHT PEN INPUT

### BLOCK DIAGRAM



# 8279/8279-5

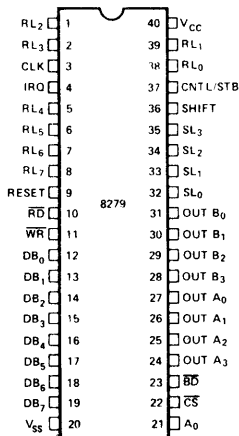
## PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- MCS-85™ Compatible 8279-5
- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8-Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover with Contact Debounce
- Dual 8- or 16-Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

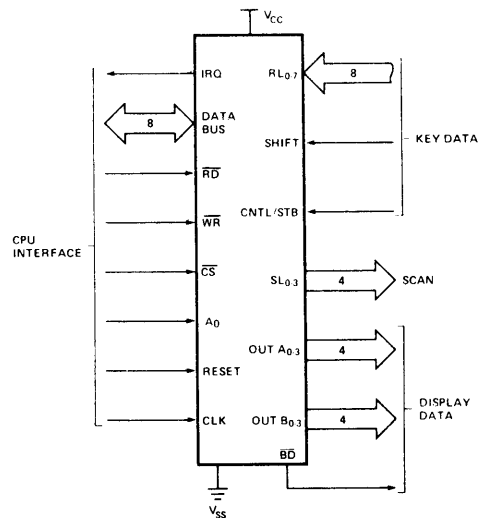
### PIN CONFIGURATION



### PIN NAMES

Symbol	I/O	DATA BUS (BI DIRECTIONAL)
DB <sub>0-7</sub>	I/O	DATA BUS (BI DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
CS	I	CHIP SELECT
RD	I	READ INPUT
WR	I	WRITE INPUT
A <sub>0</sub>	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL <sub>0-3</sub>	O	SCAN LINES
RL <sub>0-7</sub>	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL STROBE INPUT
OUT A <sub>0-3</sub>	O	DISPLAY (A) OUTPUTS
OUT B <sub>0-3</sub>	O	DISPLAY (B) OUTPUTS
BD	O	BLANK DISPLAY OUTPUT

### LOGIC SYMBOL

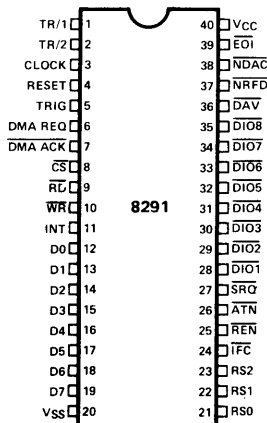


# 8291 GPIB TALKER/LISTENER

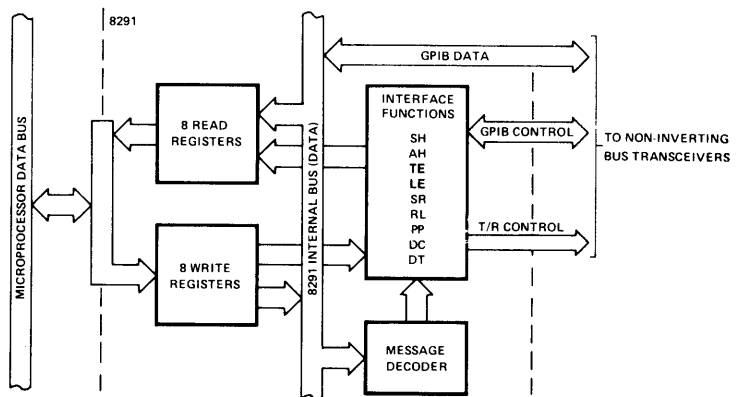
- Designed to Interface Microprocessors (e.g., 8080, 8085, 8086, 8048) to an IEEE Standard 488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features
- 1 – 8 MHz Clock Range
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Directly Interfaces to External Non-Inverting Transceivers for Connection to the GPIB
- Provides Three Addressing Modes, Allowing the Chip to be Addressed Either as a Major or a Minor Talker/Listener with Primary or Secondary Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU Intervention
- Trigger Output Pin
- On-Chip EOS (End of Sequence) Message Recognition Facilitates Handling of Multi-Byte Transfers

The 8291 GPIB Talker/Listener is a microprocessor-controlled chip designed to interface microprocessors (e.g., 8048, 8080, 8085, 8086) to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's interface functions except for the controller.

### PIN CONFIGURATION



### BLOCK DIAGRAM





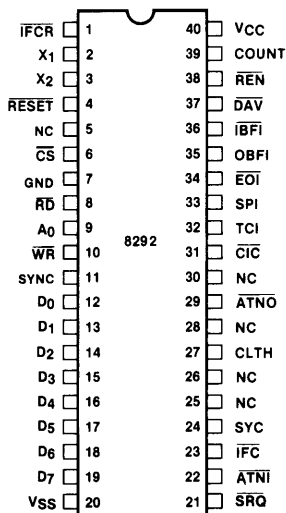
# 8292 GPIB CONTROLLER

## FEATURES:

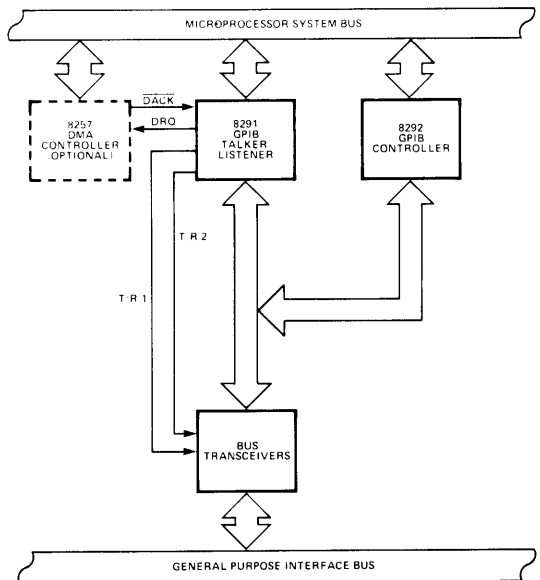
- Complete IEEE Standard 488 Controller Function.
  - Interface Clear (IFC) Sending Capability Allows for Seizure of Control and/or Initialization of the Bus.
  - Responds to Service Requests (SRQ).
  - Sends (REN), Allowing Instruments to Switch to Remote Control.
- Complete Implementation of Transfer Control Protocol.
  - Synchronous Control Seizure Prevents the Destruction of any Data Transmission in Progress.
  - Connects with the 8291 to Form a Complete IEEE Standard 488 Interface Talker/Listener/Controller.

The 8292 GPIB CONTROLLER is a microprocessor-controlled chip designed to connect with the 8291 GPIB TALKER/LISTENER to implement the full IEEE Standard 488 controller function, including transfer control protocol. The 8292 is a pre-programmed UPI-41A™

### PIN CONFIGURATION



### 8291, 8292 SYSTEM DIAGRAM





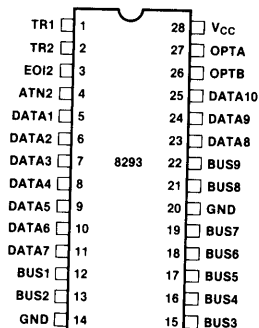
ADVANCE  
INFORMATION  
Characteristics are subject to change without notice

## 8293 GPIO TRANSCEIVER

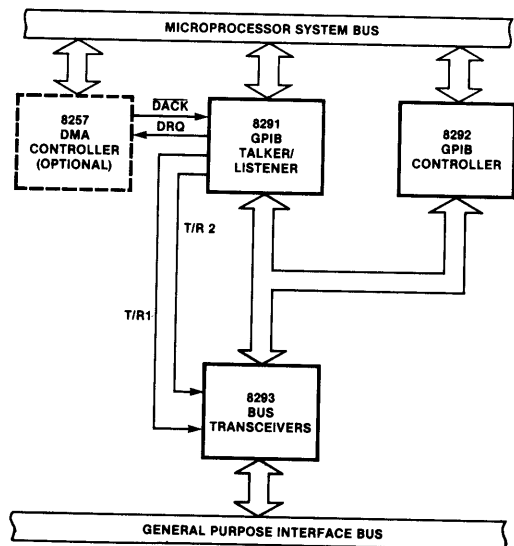
- Nine Open-collector or Three-state Line Drivers
- 48 mA Sink Current Capability on Each Line Driver
- Nine Schmitt-type Line Receivers
- High Capacitance Load Drive Capability
- Single 5V Power Supply
- 28-Pin Package
- Low Power HMOS Design
- On-chip Decoder for Mode Configuration
- Power Up/Power Down Protection to Prevent Disrupting the IEEE Bus
- Connects with the 8291 and 8292 to Form an IEEE Standard 488 Interface Talker/Listener/Controller with no Additional Components
- Only Two 8293's Required per GPIO Interface

The Intel® 8293 GPIO Transceiver is a high current, non-inverting buffer chip designed to interface the 8291 GPIO Talker/Listener or the 8292 GPIO Controller with the 8291 to the IEEE Standard 488-1978 Instrumentation Interface Bus. Each GPIO interface would contain two 8293 Bus Transceivers. In addition, the 8293 can also be used as a general purpose bus driver.

### PIN CONFIGURATION



### 8291, 8292, 8293 SYSTEM DIAGRAM





# 8294 DATA ENCRYPTION UNIT

- Certified by National Bureau of Standards
- 80 Byte/Sec Data Conversion Rate
- 64-Bit Data Encryption Using 56-Bit Key
- DMA Interface
- 3 Interrupt Outputs to Aid in Loading and Unloading Data
- 7-Bit User Output Port
- Single 5V ± 10% Power Supply
- Peripheral to MCS-86™, MCS-85™, MCS-80™ and MCS-48™ Processors
- Implements Federal Information Processing Data Encryption Standard
- Encrypt and Decrypt Modes Available

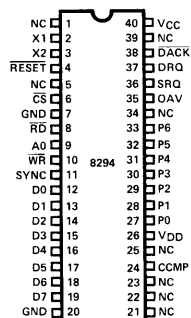
## DESCRIPTION

The Intel® 8294 Data Encryption Unit (DEU) is a microprocessor peripheral device designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard. The DEU operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. The operation is reversible: if the cipher word is operated upon, the original text word is produced. The algorithm itself is permanently contained in the 8294; however, the 56-bit key is user-defined and may be changed at any time.

The 56-bit key and 64-bit message data are transferred to and from the 8294 in 8-bit bytes by way of the system data bus. A DMA interface and three interrupt outputs are available to minimize software overhead associated with data transfer. Also, by using the DMA interface two or more DEUs may be operated in parallel to achieve effective system conversion rates which are virtually any multiple of 80 bytes/second. The 8294 also has a 7-bit TTL compatible output port for user-specified functions.

Because the 8294 implements the NBS encryption algorithm it can be used in a variety of Electronic Funds Transfer applications as well as other electronic banking and data handling applications where data must be encrypted.

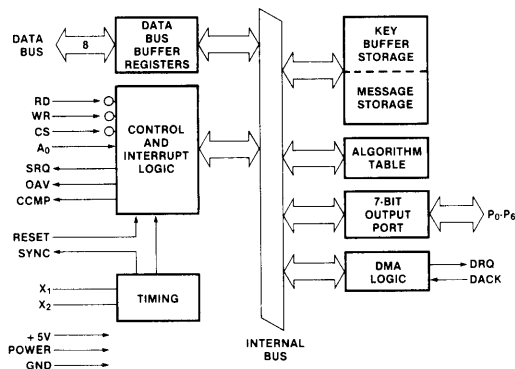
### PIN CONFIGURATION



### PIN NAMES

PIN NAME	FUNCTION
D7-D0	DATA BUS
RD, WR	READ, WRITE STROBES
CS	CHIP SELECT
A0	CONTROL/DATA SELECT
RESET	RESET INPUT
X1, X2	FREQUENCY REFERENCE INPUT
SYNC	HIGH FREQUENCY OUTPUT
DRQ, DACK	DMA REQUEST, DMA ACKNOWLEDGE
SRQ, OAV, CCMP	INTERRUPT REQUEST OUTPUTS
P <sub>7</sub> -P <sub>0</sub>	OUTPUT PORT LINES
V <sub>CC</sub> , V <sub>DD</sub> , GND	+5V POWER, GND
NC	NO CONNECTION

### BLOCK DIAGRAM



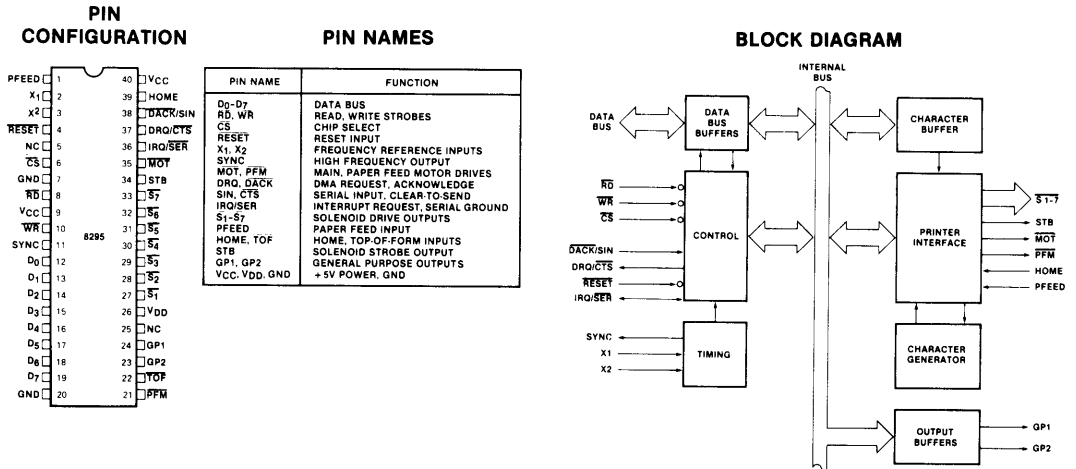


# 8295 DOT MATRIX PRINTER CONTROLLER

- Interfaces Dot Matrix Printers to MCS-48™, MCS-80/85™, MCS-86™ Systems
- 40 Character Buffer On Chip
- Serial or Parallel Communication with Host
- DMA Transfer Capability
- Programmable Character Density (10 or 12 Characters/Inch)
- Programmable Print Intensity
- Single or Double Width Printing
- Programmable Multiple Line Feeds
- 3 Tabulations
- 2 General Purpose Outputs

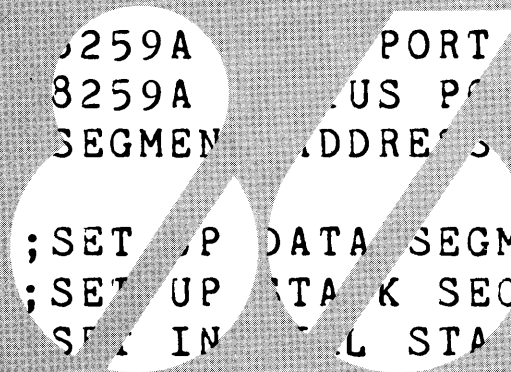
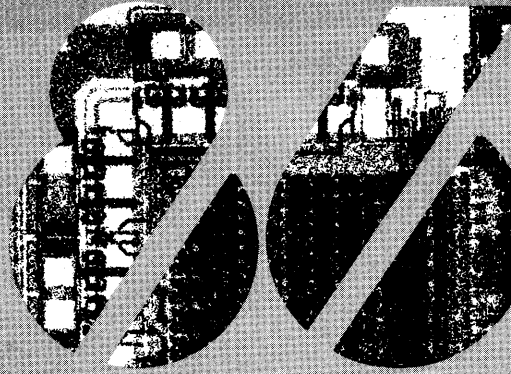
The Intel® 8295 Dot Matrix Printer Controller provides an interface for microprocessors to the LRC 7040 Series dot matrix impact printers. It may also be used as an interface to other similar printers.

The chip may be used in a serial or parallel communication mode with the host processor. In parallel mode, data transfers are based on polling, interrupts, or DMA. Furthermore, it provides internal buffering of up to 40 characters and contains a 7 × 7 matrix character generator accommodating 64 ASCII characters.



## Appendix B Device Specifications

- 8086 Family
- 8085 Peripherals\*
- Standard Peripherals\*\*
- **RAM Memories\*\*\***
- EPROM Memories\*\*\*
- Development Tools



\*For complete specifications refer to the Intel MCS-85 User's Manual.

\*\*For complete specifications refer to the Intel Peripheral Design Handbook.

\*\*\*For complete specifications refer to the 1979 Intel Component Data Catalog.





**PRELIMINARY**  
 Notice: This is not a final specification. Some parametric limits are subject to change.

## 2114A 1024 X 4 BIT STATIC RAM

	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
<b>Max. Access Time (ns)</b>	120	150	200	200	250
<b>Max. Current (mA)</b>	40	40	40	70	70

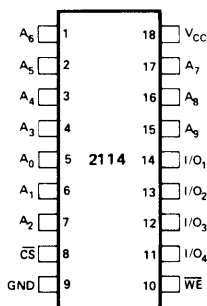
- **HMOS Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply  $\pm 10\%$**
- **High Density 18 Pin Package**
- **Completely Static Memory - No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **2114 Replacement**

The Intel 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

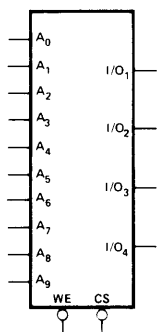
The 2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ( $\overline{CS}$ ) lead allows easy selection of an individual package when outputs are or-tied.

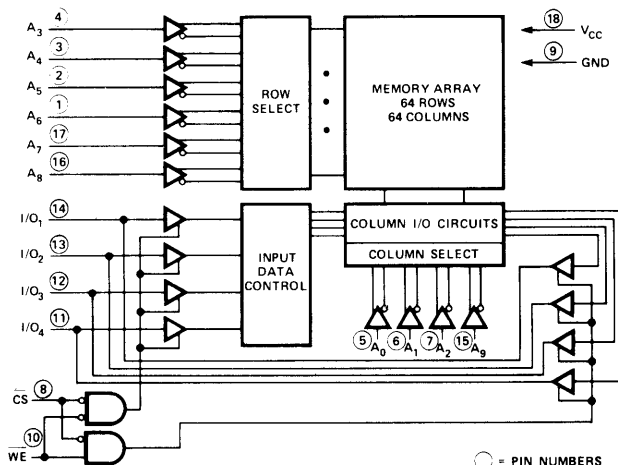
### PIN CONFIGURATION



### LOGIC SYMBOL



### BLOCK DIAGRAM



### PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS	$V_{CC}$ POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
$I/O_1 - I/O_4$	DATA INPUT/OUTPUT	



# 2142

## 1024 X 4 BIT STATIC RAM

	2142-2	2142-3	2142	2142L2	2142L3	2142L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- High Density 20 Pin Package
- Access Time Selections From 200-450ns
- Identical Cycle and Access Times
- Low Operating Power Dissipation  
.1mW/Bit Typical
- Single +5V Supply
- No Clock or Timing Strobe Required
- Completely Static Memory
- Directly TTL Compatible: All Inputs and Outputs
- Common Data Input and Output Using Three-State Outputs

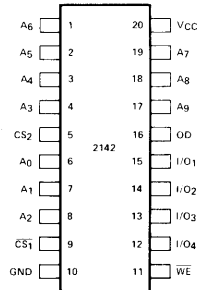
The Intel® 2142 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply.

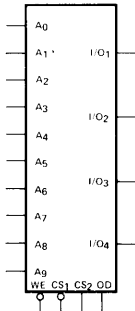
The 2142 is placed in a 20-pin package. Two Chip Selects ( $\overline{CS}_1$  and  $\overline{CS}_2$ ) are provided for easy and flexible selection of individual packages when outputs are OR-tied. An Output Disable is included for direct control of the output buffers.

The 2142 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

### PIN CONFIGURATION



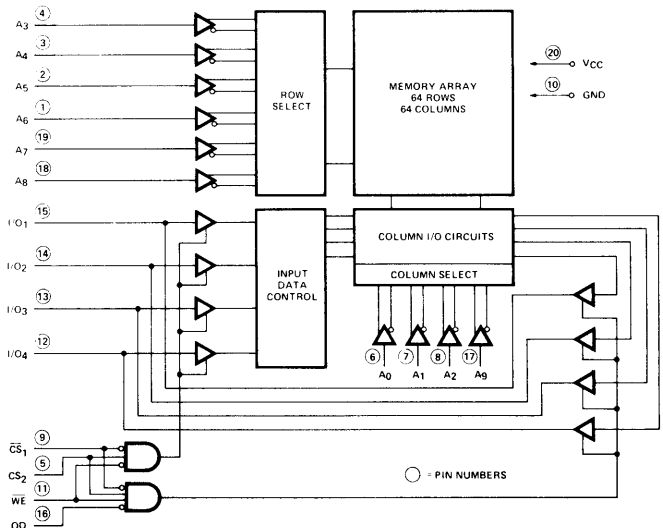
### LOGIC SYMBOL



### PIN NAMES

A <sub>0</sub> -A <sub>9</sub>	ADDRESS INPUTS	OD	OUTPUT DISABLE
WE	WRITE ENABLE	V <sub>CC</sub>	POWER (+5V)
$\overline{CS}_1, \overline{CS}_2$	CHIP SELECT	GND	GROUND
I/O <sub>1</sub> -I/O <sub>4</sub>	DATA INPUT/OUTPUT		

### BLOCK DIAGRAM





**PRELIMINARY**  
 Notice: This is not a final specification. Some parametric limits are subject to change.

# 2148

## 1024 x 4 BIT STATIC RAM

	2148-3	2148	2148-6
Max. Access Time (ns)	55	70	85
Max. Active Current (mA)	125	125	125
Max. Standby Current (mA)	30	30	30

- **HMOS Technology**
- **Automatic Power-Down**
- **Completely Static Memory**  
— No Clock or Timing Strobe Required
- **High Density 18-Pin Package**
- **Equal Access and Cycle Times**
- **Directly TTL Compatible**  
— All Inputs and Outputs
- **Single +5V Supply**
- **Common Data Input and Output**
- **Three-State Output**

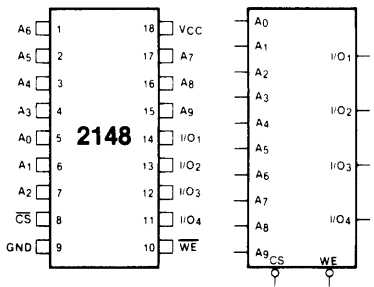
The Intel® 2148 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$  controls the power-down feature. In less than a cycle time after  $\overline{CS}$  goes high — disabling the 2148 — the part automatically reduces its power requirements and remains in this low power standby mode as long as  $\overline{CS}$  remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are disabled.

The 2148 is assembled in an 18-pin package configured with the industry standard 1Kx4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

### PIN CONFIGURATION

### LOGIC SYMBOL



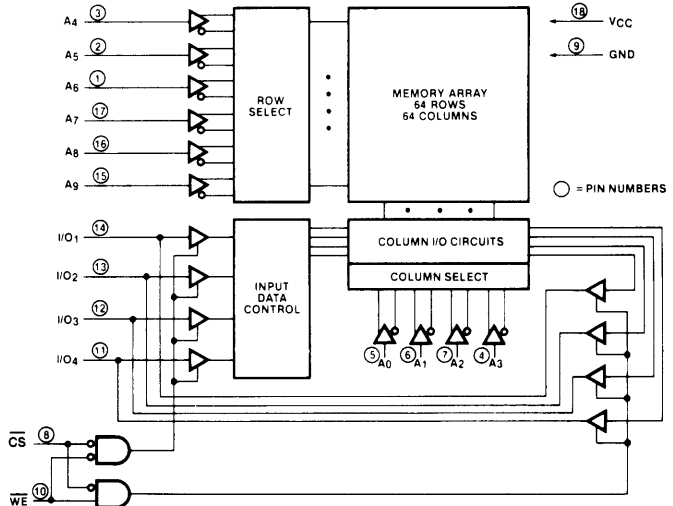
### PIN NAMES

A <sub>0</sub> -A <sub>9</sub>	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
I/O <sub>1</sub> -I/O <sub>4</sub>	DATA INPUT/OUTPUT
V <sub>CC</sub>	POWER (+5V)
GND	GROUND

### TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D <sub>IN</sub>	ACTIVE
L	H	READ	D <sub>OUT</sub>	ACTIVE

### BLOCK DIAGRAM





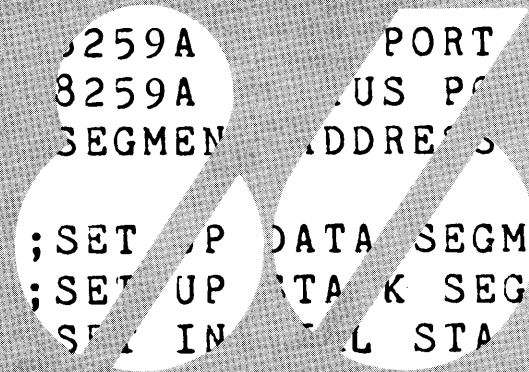
## Appendix B Device Specifications

- 8086 Family
- 8085 Peripherals\*
- Standard Peripherals\*\*
- RAM Memories\*\*\*
- **EPROM Memories\*\*\***
- Development Tools

\*For complete specifications refer to the Intel MCS-85 User's Manual.

\*\*For complete specifications refer to the Intel Peripheral Design Handbook.

\*\*\*For complete specifications refer to the 1979 Intel Component Data Catalog.





# 2716

## 16K (2K × 8) UV ERASABLE PROM

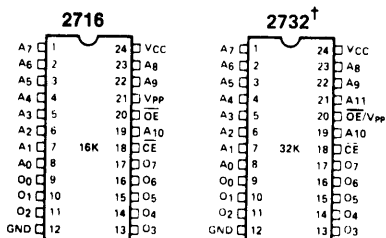
- **Fast Access Time**
  - 350 ns Max. 2716-1
  - 390 ns Max. 2716-2
  - 450 ns Max. 2716
  - 650 ns Max. 2716-6
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power
- **Pin Compatible to Intel® 2732 EPROM**
- **Simple Programming Requirements**
  - Single Location Programming
  - Programs with One 50 ms Pulse
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

### PIN CONFIGURATION



† Refer to 2732 data sheet for specifications

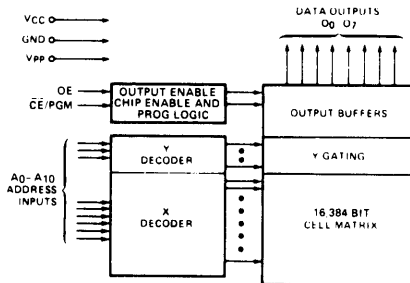
### PIN NAMES

A <sub>0</sub> - A <sub>10</sub>	ADDRESSES
CE/PGM	CHIP ENABLE/PROGRAM
OE	OUTPUT ENABLE
O <sub>0</sub> - O <sub>7</sub>	OUTPUTS

### MODE SELECTION

MODE \ PINS	CE/PGM (18)	OE (20)	V <sub>pp</sub> (21)	V <sub>CC</sub> (24)	OUTPUTS (9-11, 13-17)
Read	V <sub>IL</sub>	V <sub>IL</sub>	+5	+5	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	Don't Care	+5	+5	High Z
Program	Pulsed V <sub>IL</sub> to V <sub>IH</sub>	V <sub>IH</sub>	+25	+5	D <sub>IN</sub>
Program Verify	V <sub>IL</sub>	V <sub>IL</sub>	+25	+5	D <sub>OUT</sub>
Program Inhibit	V <sub>IL</sub>	V <sub>IH</sub>	+25	+5	High Z

### BLOCK DIAGRAM





**PRELIMINARY**  
 Notice: This is not a final specification. Some parametric limits are subject to change.

## 2732 32K (4K x 8) UV ERASABLE PROM

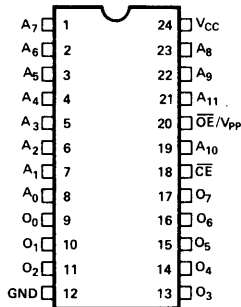
- **Fast Access Time:**
  - 450 ns Max. 2732
  - 550 ns Max. 2732-6
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  - 150mA Max. Active Current
  - 30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - Single Location Programming
  - Programs with One 50ms Pulse
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ( $\overline{OE}$ ), from the Chip Enable control ( $\overline{CE}$ ). The  $\overline{OE}$  control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-30 describes the microprocessor system implementation of the  $\overline{OE}$  and  $\overline{CE}$  controls on Intel's 2716 and 2732 EPROMs. AP-30 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the  $\overline{CE}$  input.

### PIN CONFIGURATION



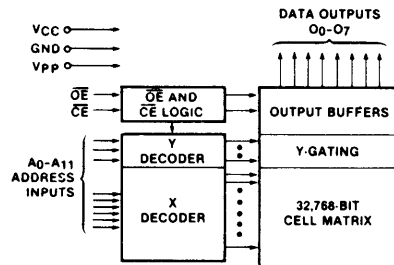
### PIN NAMES

A <sub>0</sub> -A <sub>11</sub>	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O <sub>0</sub> -O <sub>7</sub>	OUTPUTS

### MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V <sub>CC</sub> (24)	OUTPUTS (9-11,13-17)
Read	V <sub>IL</sub>	V <sub>IL</sub>	+5	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	Don't Care	+5	High Z
Program	V <sub>IL</sub>	V <sub>PP</sub>	+5	D <sub>IN</sub>
Program Verify	V <sub>IL</sub>	V <sub>IL</sub>	+5	D <sub>OUT</sub>
Program Inhibit	V <sub>IH</sub>	V <sub>PP</sub>	+5	High Z

### BLOCK DIAGRAM





# 2758

## 8K (1K × 8) UV ERASABLE LOW POWER PROM

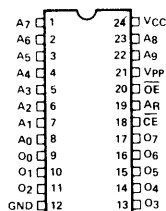
- Single +5V Power Supply
- Simple Programming Requirements
  - Single Location Programming
  - Programs with One 50 ms Pulse
- Low Power Dissipation
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power
- Fast Access Time: 450 ns Max. in Active and Standby Power Modes
- Inputs and Outputs TTL Compatible during Read and Program
- Completely Static
- Three-State Outputs for OR-Ties

The Intel® 2758 is a 8192-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2758 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. The total programming time for all 8192 bits is 50 seconds.

The 2758 has a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW, while the maximum standby power dissipation is only 132 mW, a 75% savings. Power-down is achieved by applying a TTL-high signal to the  $\overline{CE}$  input.

A 2758 system may be designed for total upwards compatibility with Intel's 16K 2716 EPROM (see Applications Note 30). The 2758 maintains the simplest and fastest method yet devised for programming EPROMs — single pulse TTL-level programming. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time — either individually, sequentially, or at random, with the single address location programming.

### PIN CONFIGURATION



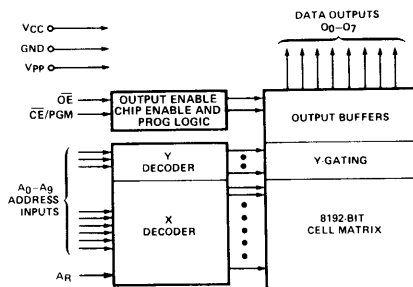
### MODE SELECTION

MODE	PINS					
	$\overline{CE}/\text{PGM}$ (18)	$A_R$ (19)	$\overline{OE}$ (20)	$V_{pp}$ (21)	$V_{cc}$ (24)	OUTPUTS (9-11, 13-17)
Read	$V_{IL}$	$V_{IL}$	$V_{IL}$	+5	+5	$D_{OUT}$
Standby	$V_{IH}$	$V_{IL}$	Don't Care	+5	+5	High Z
Program	Pulsed $V_{IL}$ to $V_{IH}$	$V_{IL}$	$V_{IH}$	+25	+5	$D_{IN}$
Program Verify	$V_{IL}$	$V_{IL}$	$V_{IL}$	+25	+5	$D_{OUT}$
Program Inhibit	$V_{IL}$	$V_{IL}$	$V_{IH}$	+25	+5	High Z

### PIN NAMES

$A_0$ – $A_9$	ADDRESSES
$\overline{CE}/\text{PGM}$	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
$O_0$ – $O_7$	OUTPUTS
$A_R$	SELECT REFERENCE INPUT LEVEL

### BLOCK DIAGRAM



## Appendix B Device Specifications

- 8086 Family
- 8085 Peripherals\*
- Standard Peripherals\*\*
- RAM Memories\*\*\*
- EPROM Memories\*\*\*
- **Development Tools**

\*For complete specifications refer to the Intel MCS-85 User's Manual.

\*\*For complete specifications refer to the Intel Peripheral Design Handbook.

\*\*\*For complete specifications refer to the 1979 Intel Component Data Catalog.

