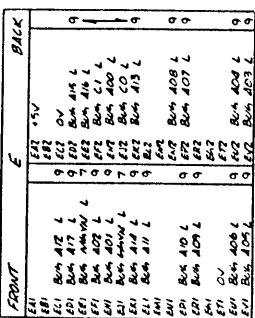
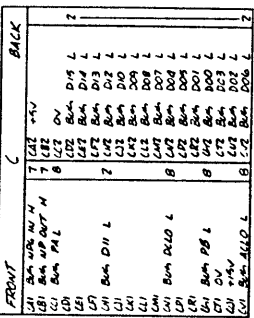
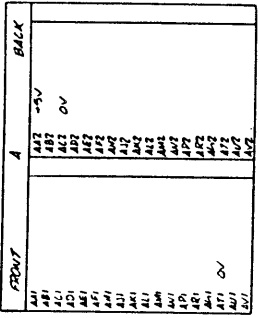
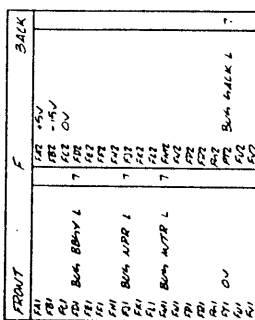
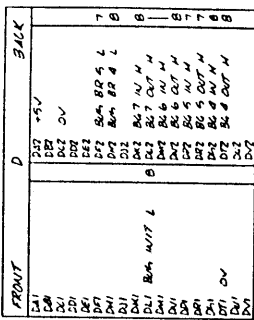
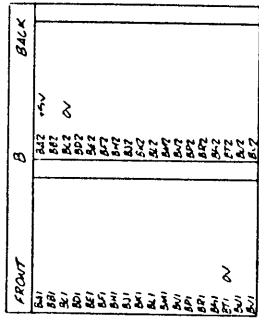
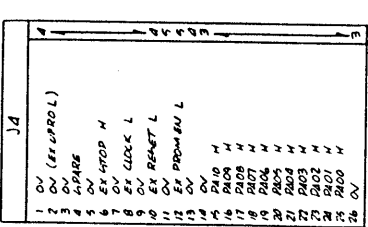
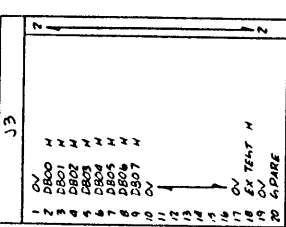


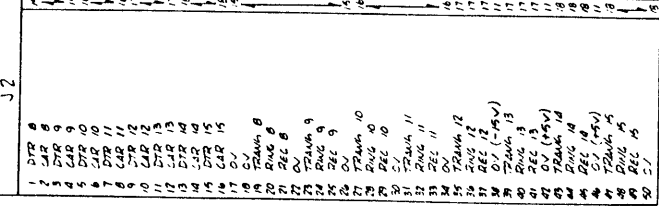
EDGE CONNECTORS



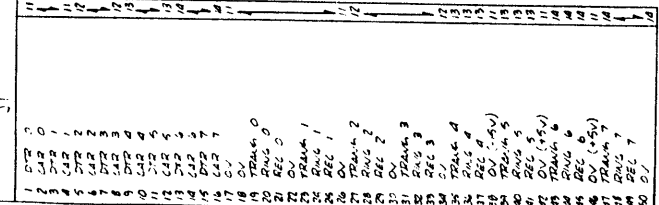
TEST CONNECTORS



INTERFLEX CONNECTOR



INTERFLEX CONNECTOR



NOTES: UNLESS OTHERWISE SPECIFIED
 1. CAPACITANCE VALUES ARE IN MICROFARADS.
 2. RESISTANCE VALUES ARE IN OHMS, UNLESS

JUMPERS LOCATION

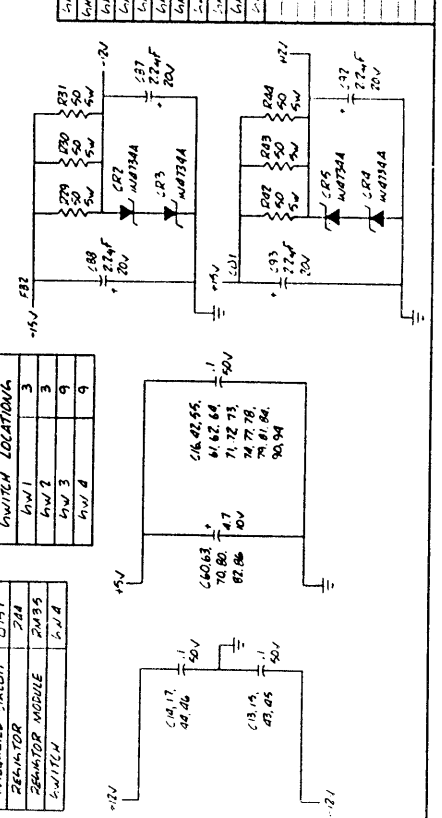
A	B	C

SWITCH LOCATION

SW1	SW2	SW3	SW4

UNIT REFERENCE DESIGNATION AND PART NUMBER

DESIGNATION	QUANTITY	PART NUMBER
CONDENSATOR	33A	74A-00
DIODE	1R5	74A-32
RESISTOR	15T	74A-20
SWITCH	244	74A-00

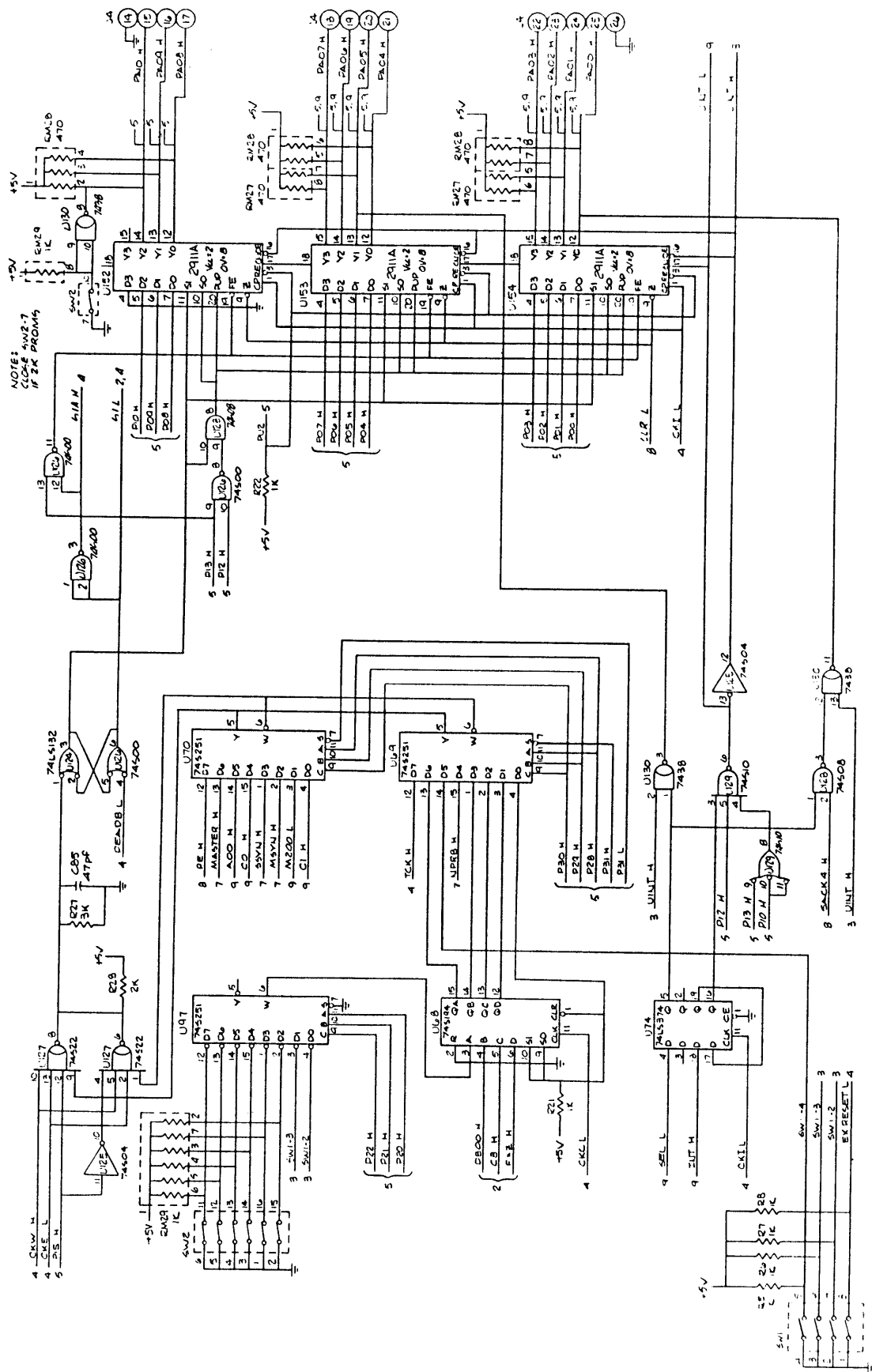


PREFERRED PART NUMBER	QUANTITY	PART NUMBER
C41	2/4	74A-38
C42	2/4	74A-00
C43	3/4	74A-00
C44	2/4	74A-32
C45	3/4	74A-20
C46	2/4	74A-00
C47	1/2	74A-72
C48	5/6	74A-04
C49	3/4	74A-04
C50	3/4	74A-02
C51	3/4	74A-00
C52	2/4	74A-00
C53	2/4	74A-00
C54	3/4	74A-32
C55	3/4	74A-32

SHEET 19 BAND RATE GENERATOR
 SHEET 18 CHANNEL 0 TEST CHANNEL 15
 SHEET 17 BREAK CONTROL REGULATOR TIME DATA REGISTER MEMORY
 SHEET 16 VECTOR INTERRUPT ADDRESS CODE / ADDRESS RANGE PERM.
 SHEET 15 VECT CONTROL
 SHEET 14 UPB CONTROL / BUS Arbitration
 SHEET 13 BUFFER ADDRESS REGISTER / BUFFER
 SHEET 12 LOOK-UP / 25.6 US TIMER
 SHEET 11 TEST AUX
 SHEET 10 JNDY / JLD / DRY / SUBDATA DATA REGISTER
 SHEET 9... SHEET 2...

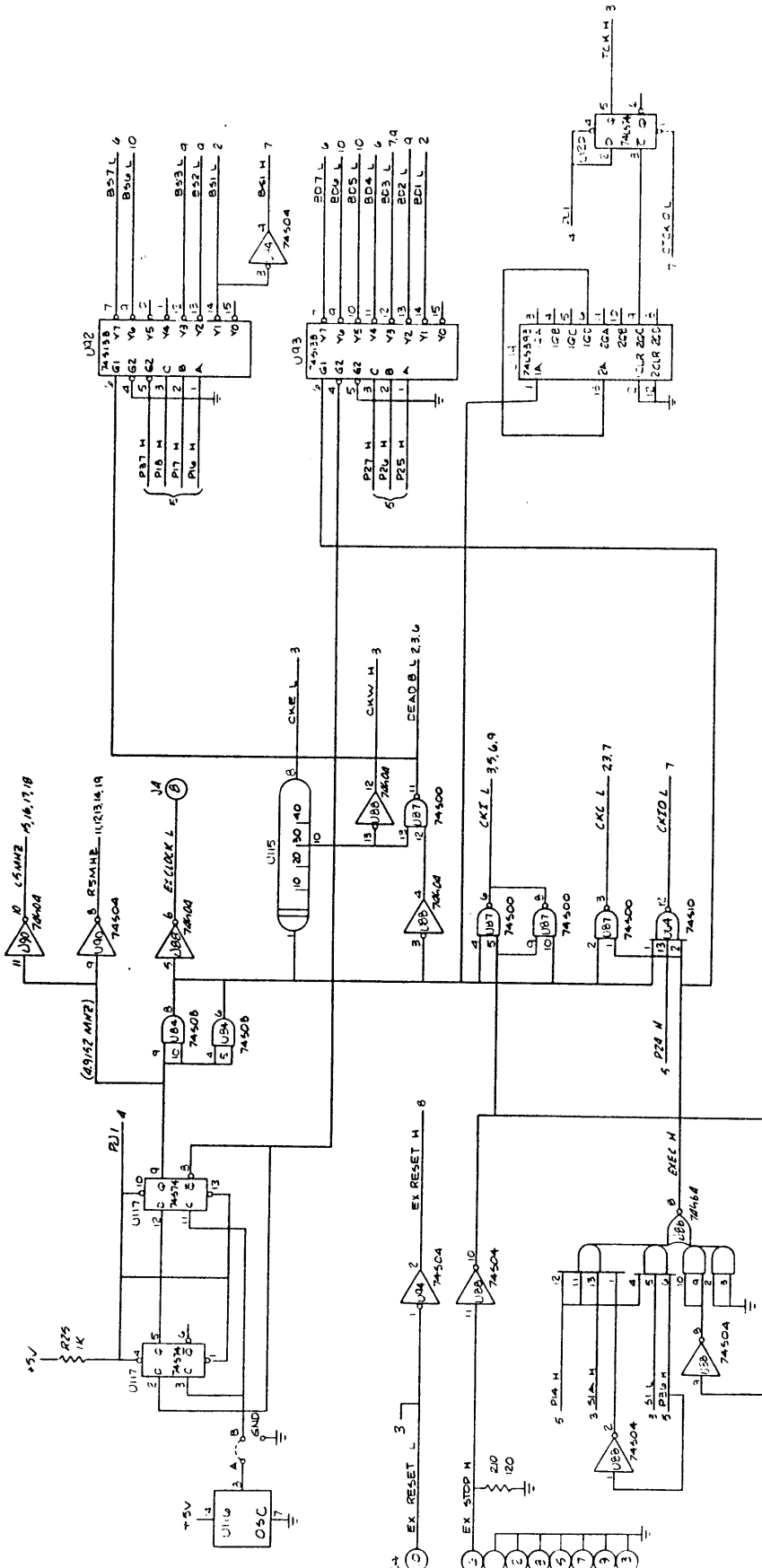
TITLE: SCHEMATIC DIAGRAM - CR3 COMMUNICATIONS FILTER
 DRAWN BY: J.B.P. / J.B.P. / J.B.P.
 CHECKED BY: J.B.P. / J.B.P. / J.B.P.
 APPROVED BY: J.B.P. / J.B.P. / J.B.P.
 DESIGNED BY: J.B.P. / J.B.P. / J.B.P.
 CHECKED BY: J.B.P. / J.B.P. / J.B.P.
 APPROVED BY: J.B.P. / J.B.P. / J.B.P.
 DATE: MAR 1963

EMULTE CORPORATION
 COSTA MESA, CALIF.



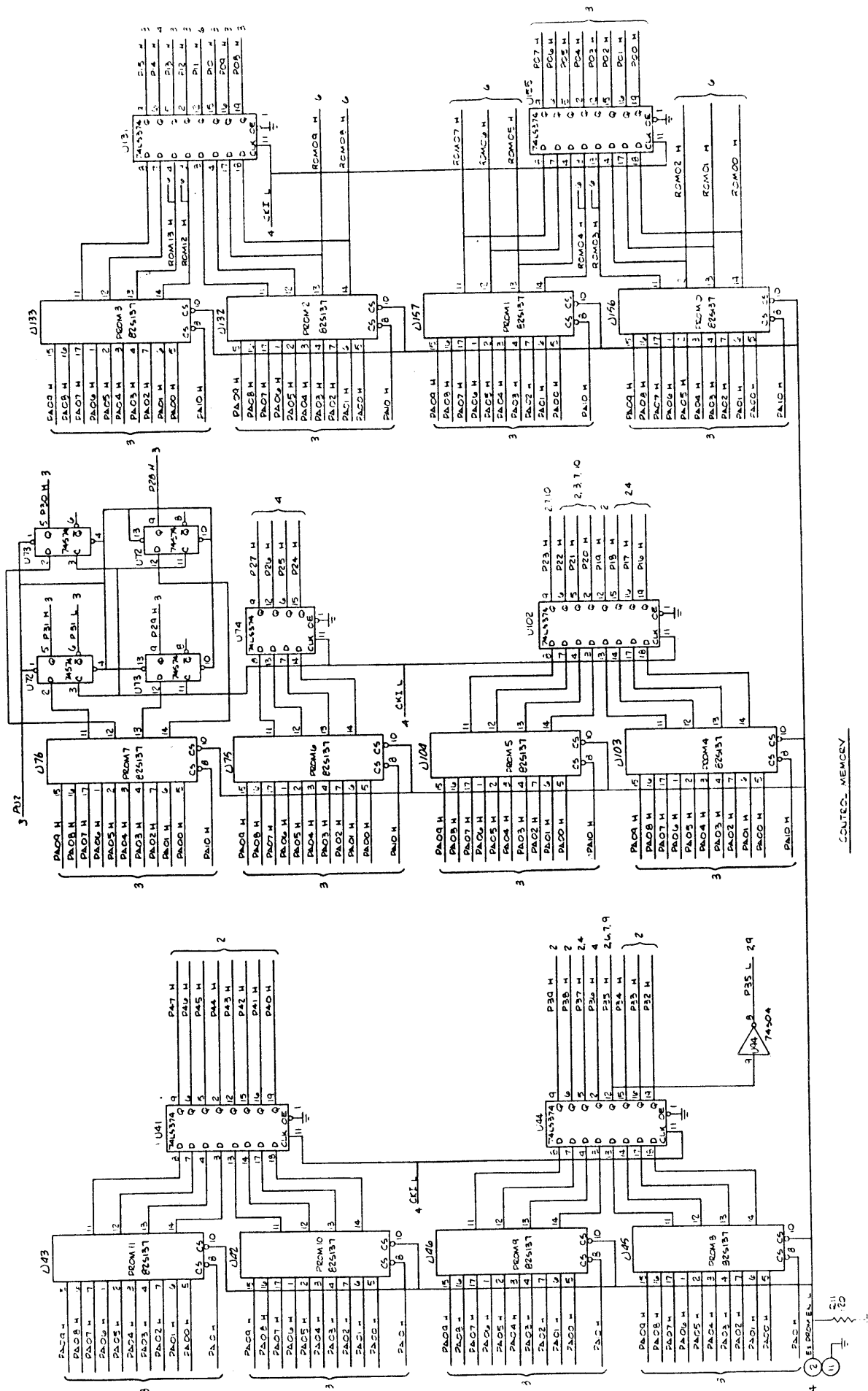
NOTE:
CLOSE SW2-7
IF 2K PROMS

TEST MUX

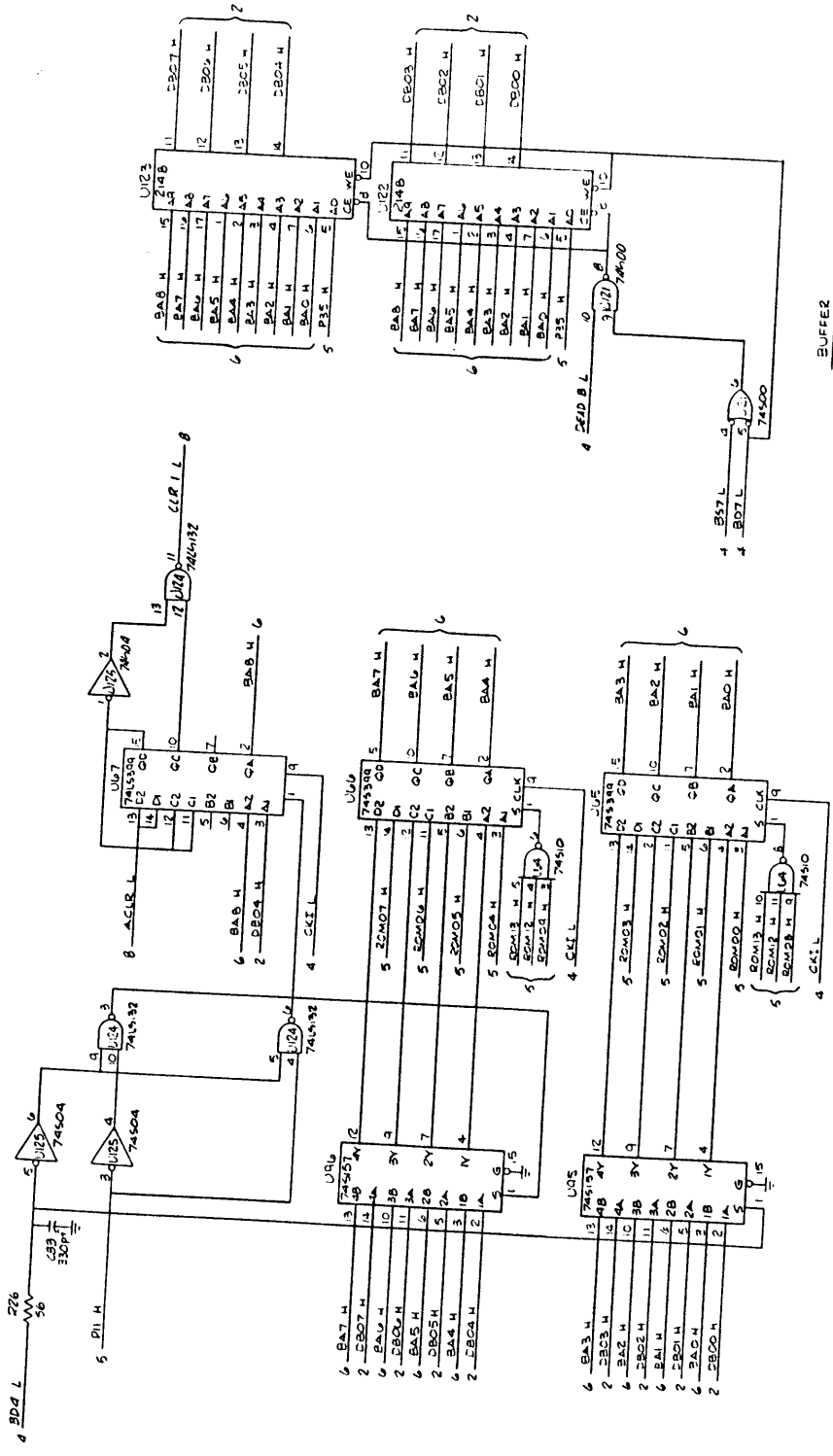


CLOCKING

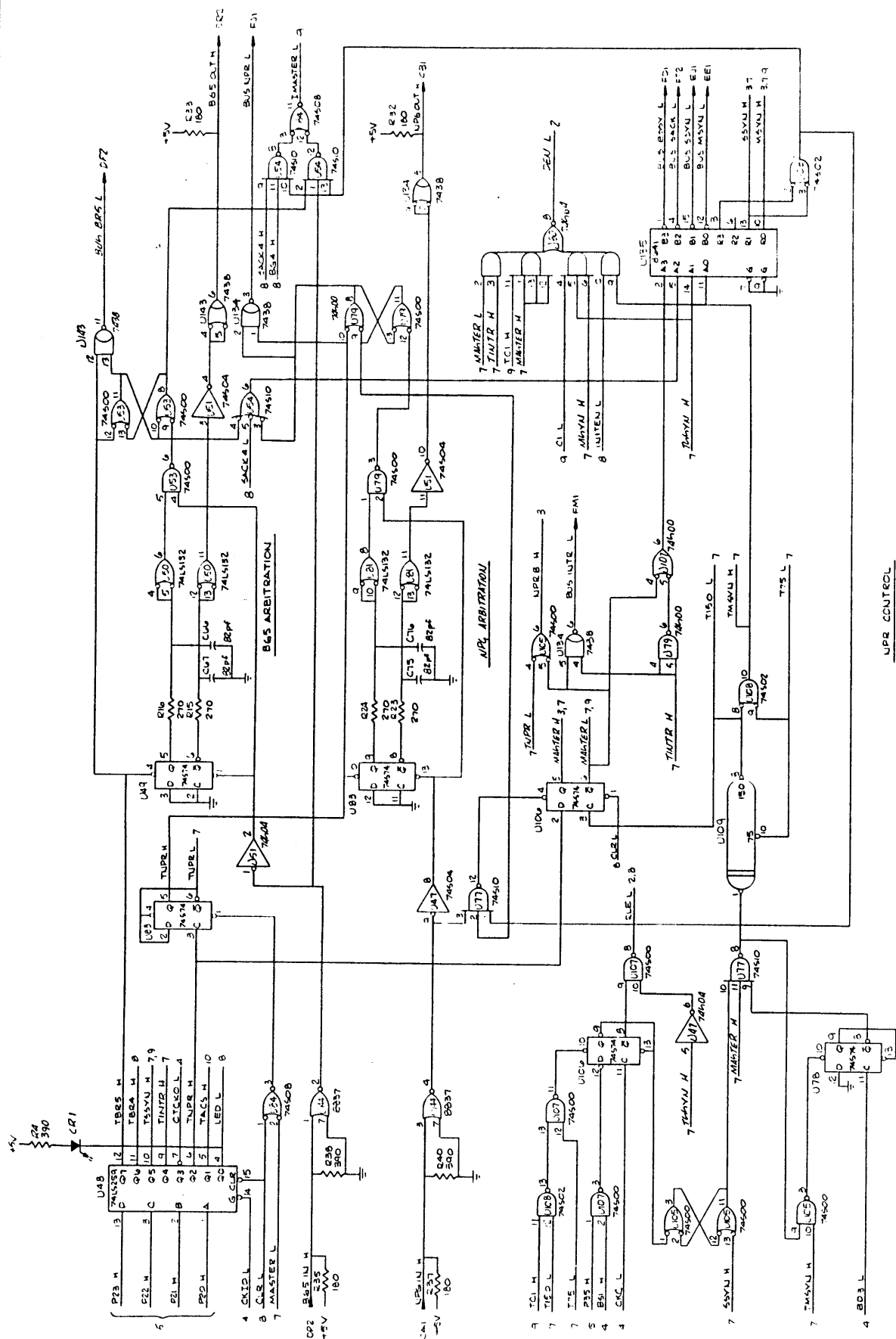
25.0 US TIMER



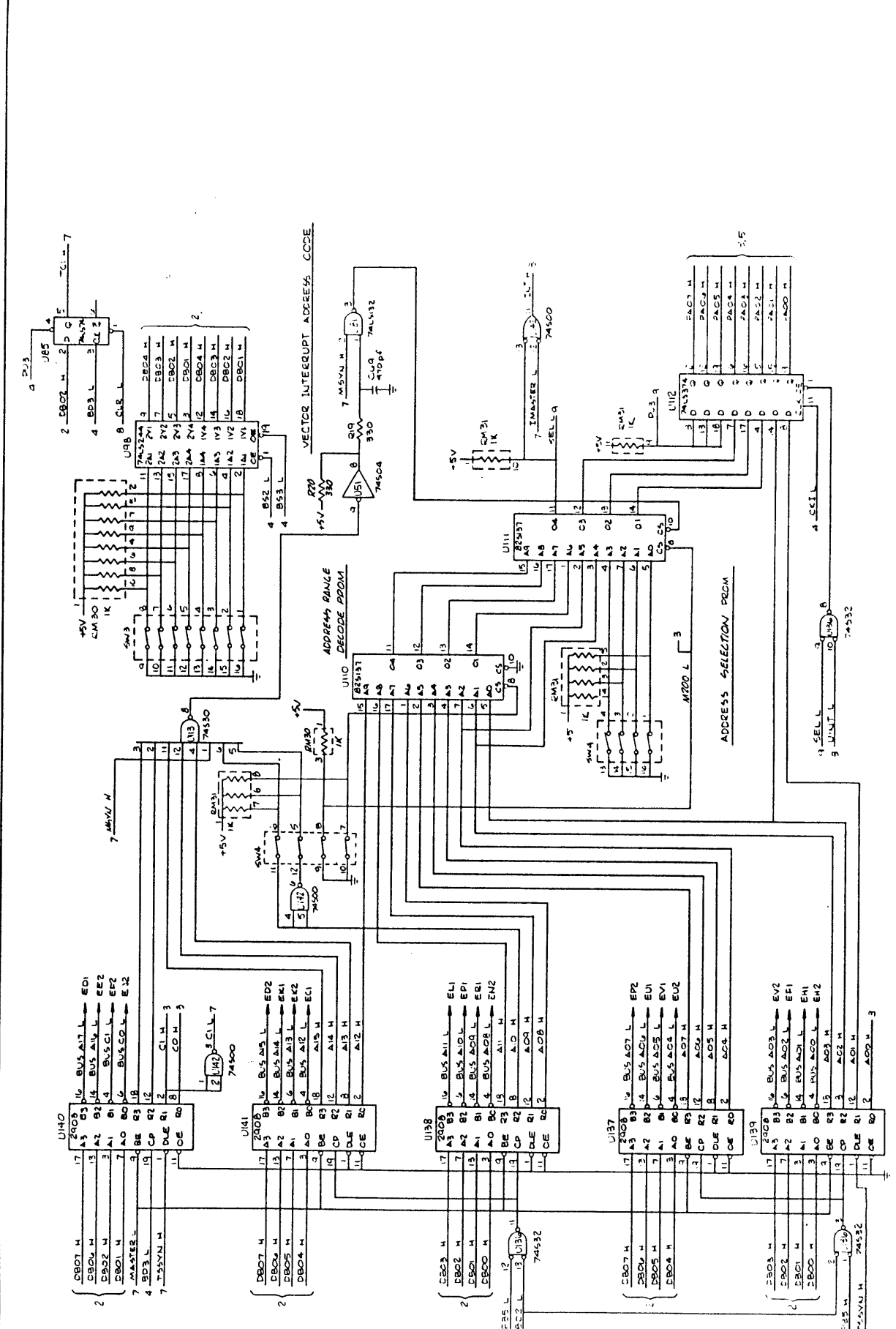
COURTESY - MEMCEY

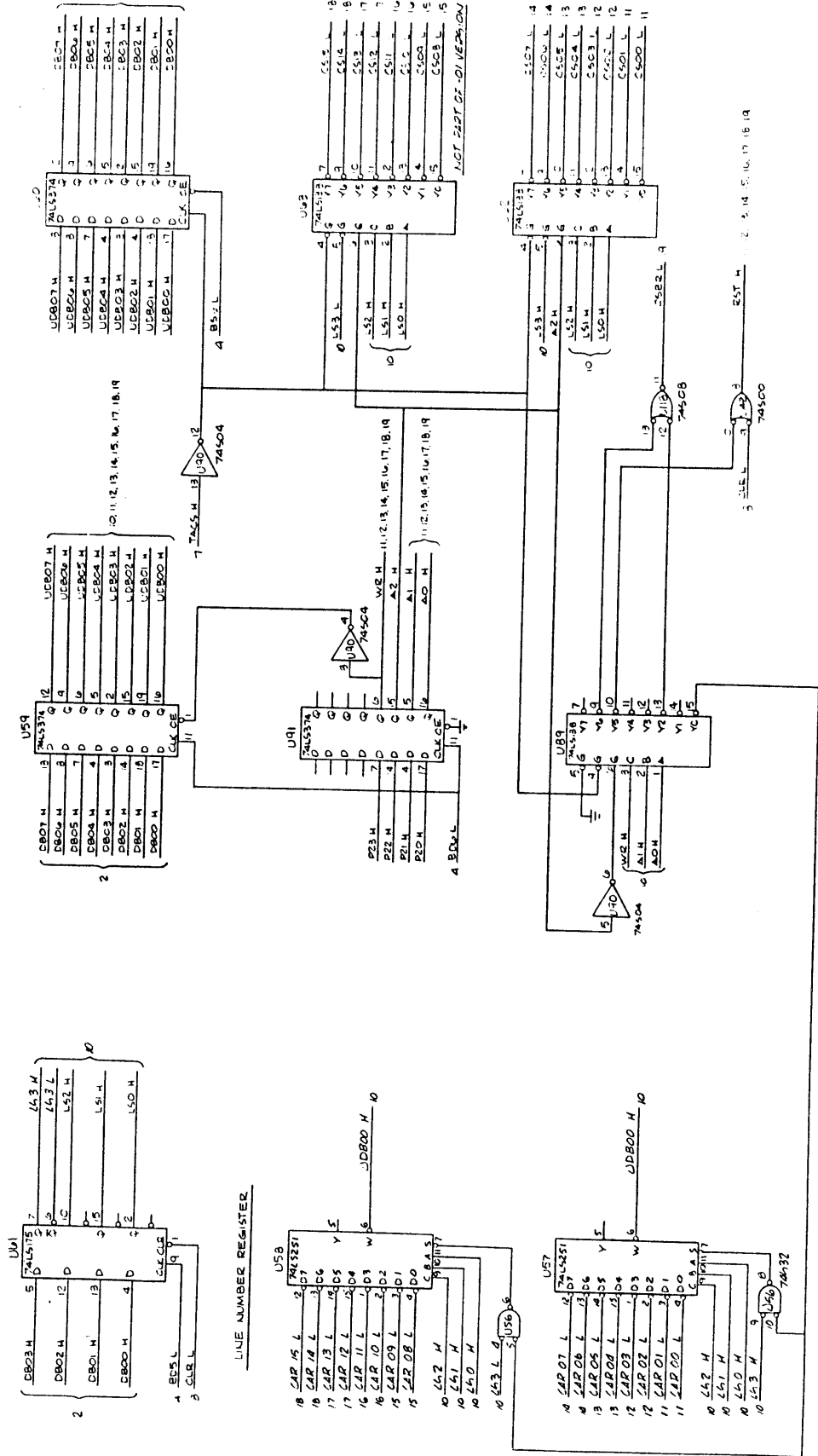


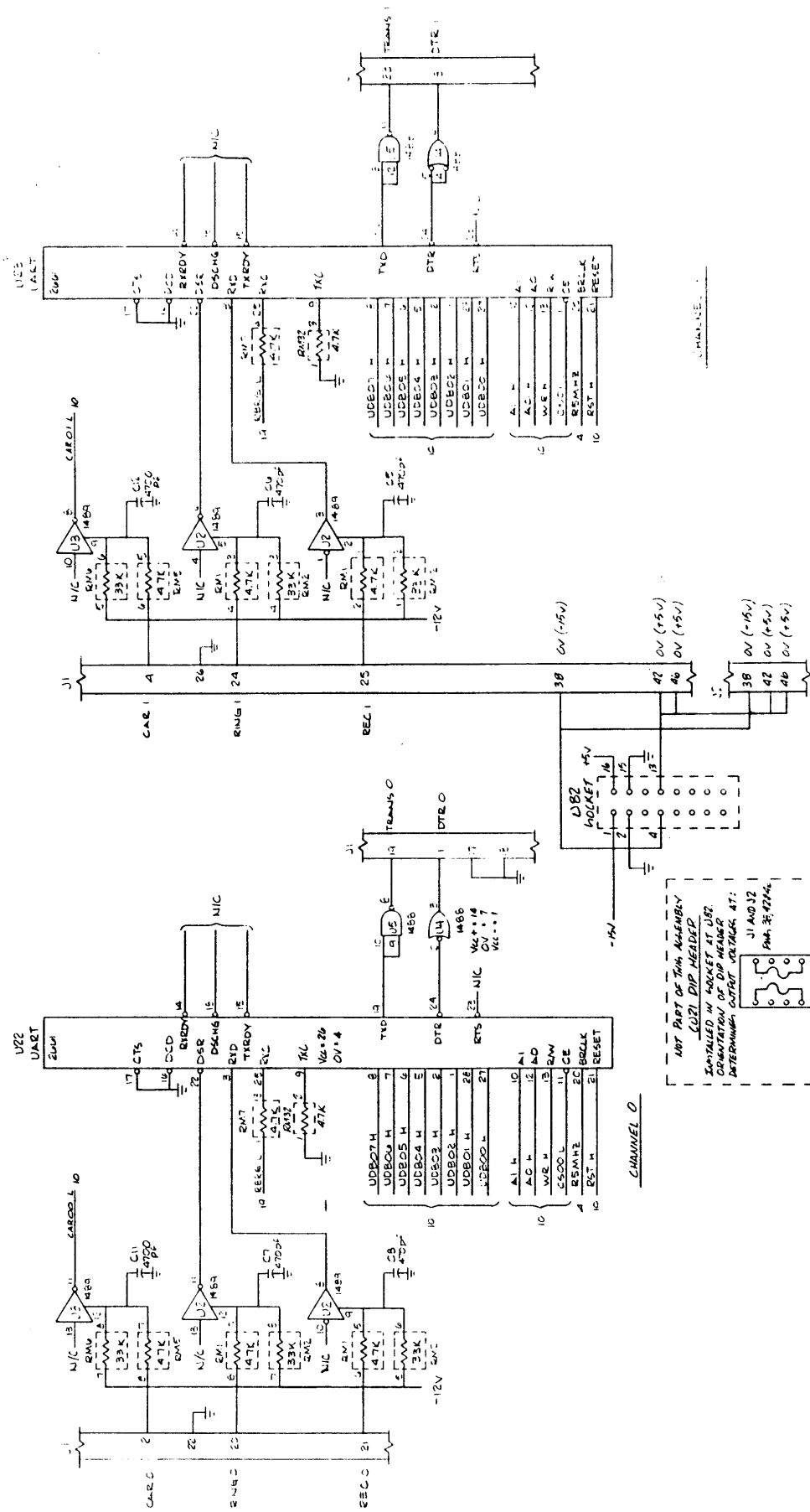
BUFFER ADDRESS REGISTER



UPR CONTROL

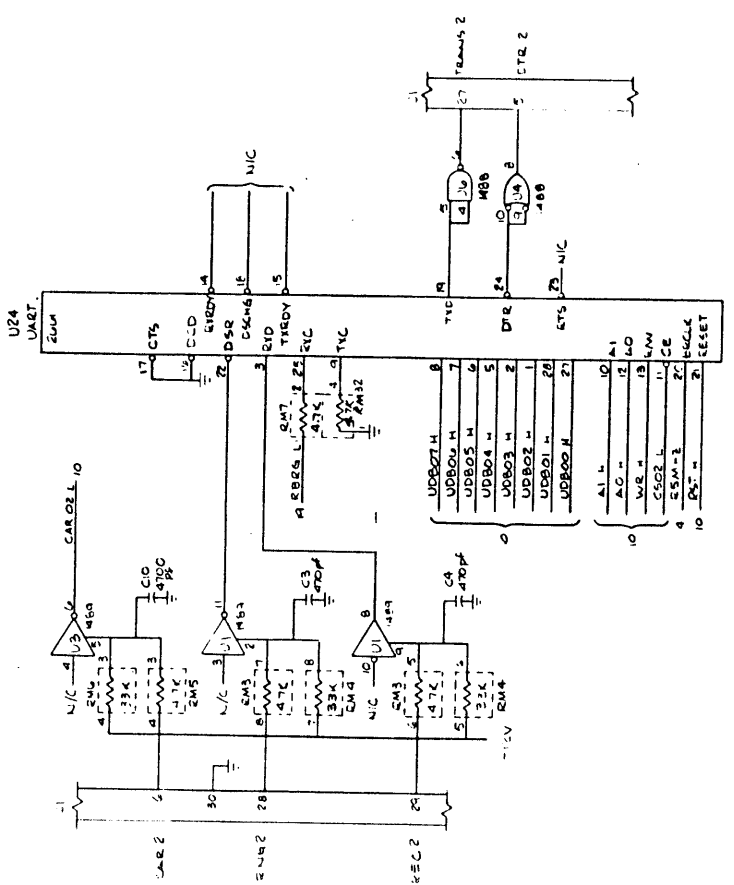
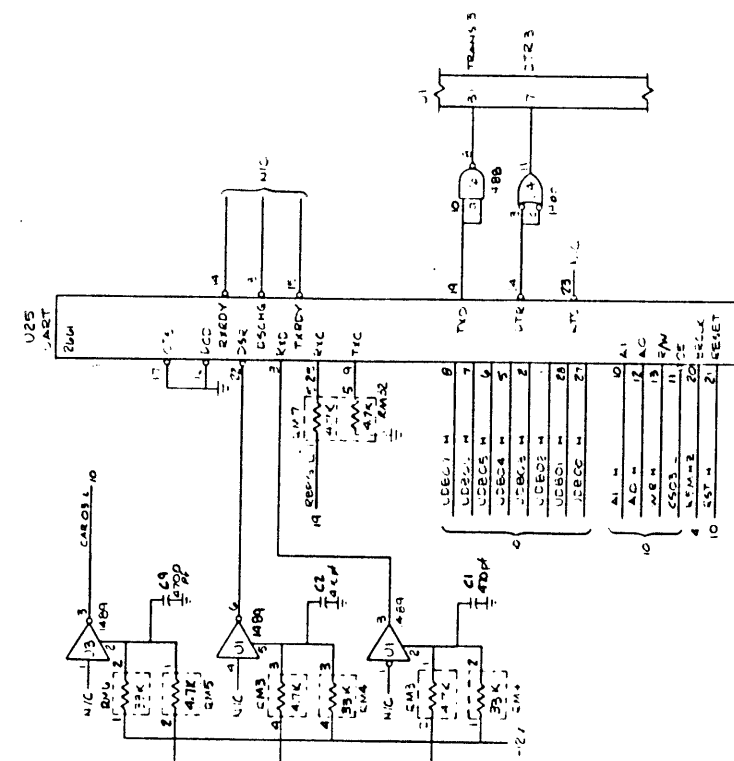






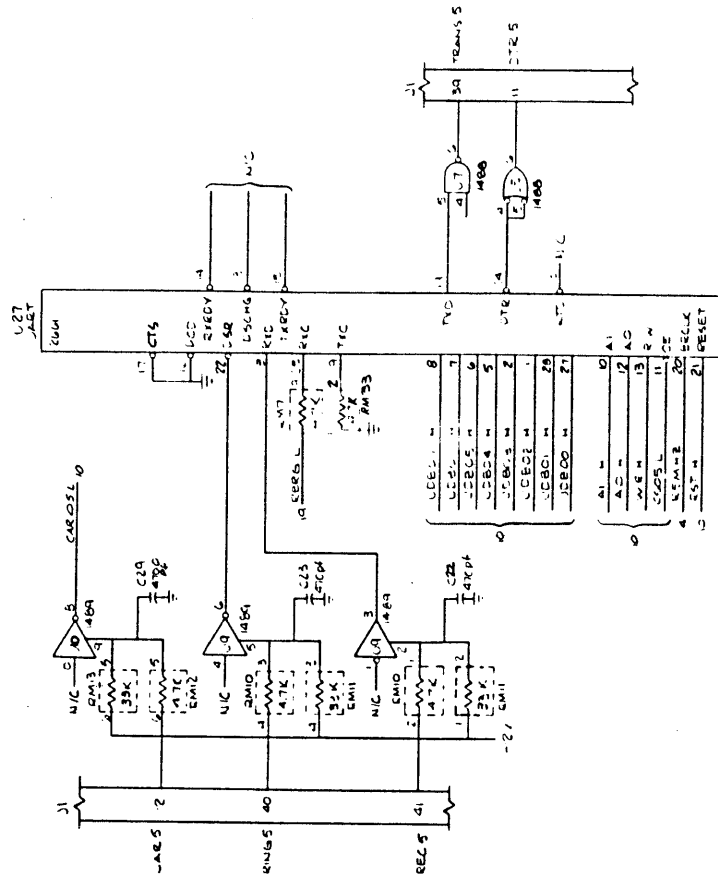
NOT PART OF THIS ASSEMBLY
 U221 DIP HEADER
 INSTALLED IN CHANNEL 0 SET.
 CHANNEL 0 SET HAS TWO
 DETERMINING OUTPUT CHANNELS AT:
 J1 AND J2
 PWA 35-12144

CHANNEL 0

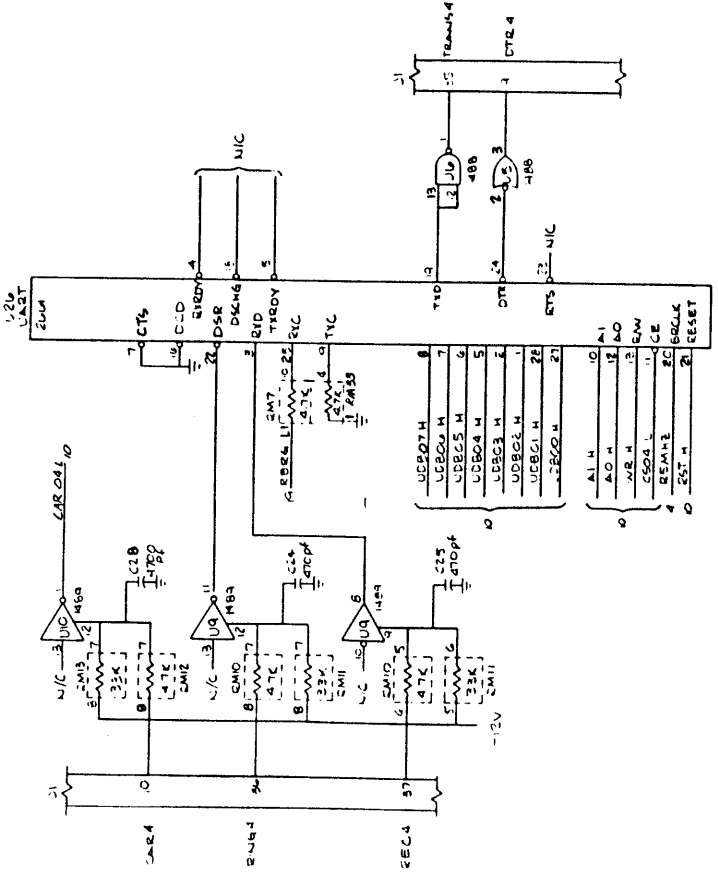


CHANNEL 2

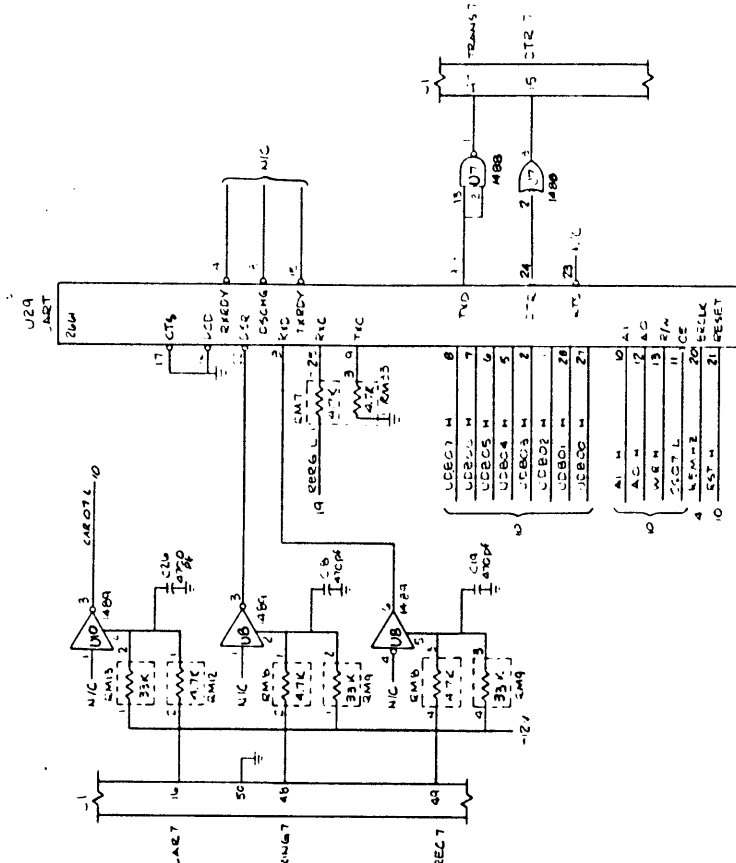
CHANNEL 3



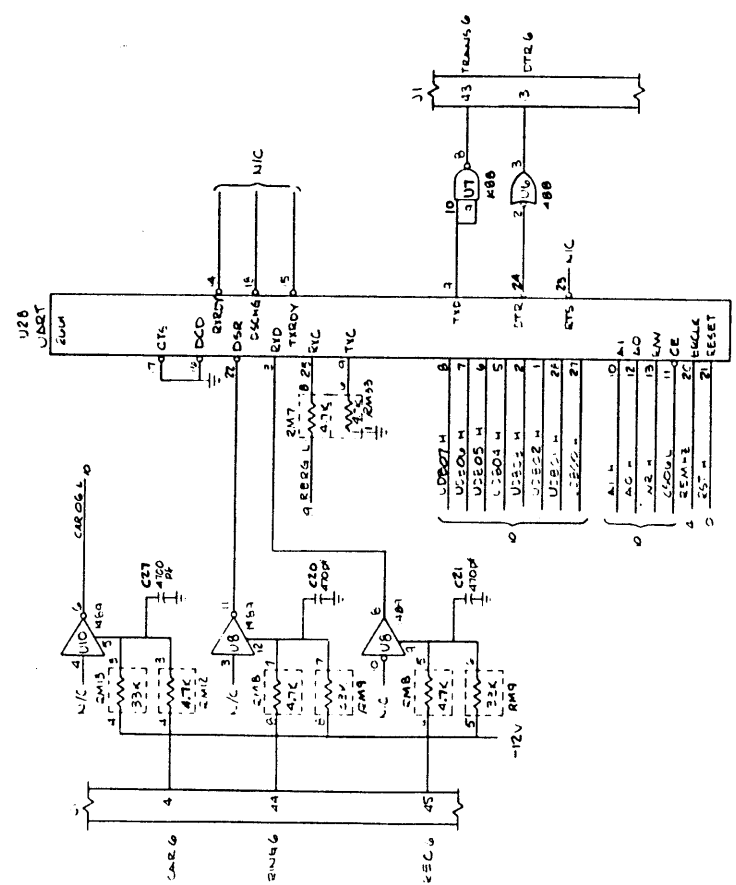
CHANNEL 5



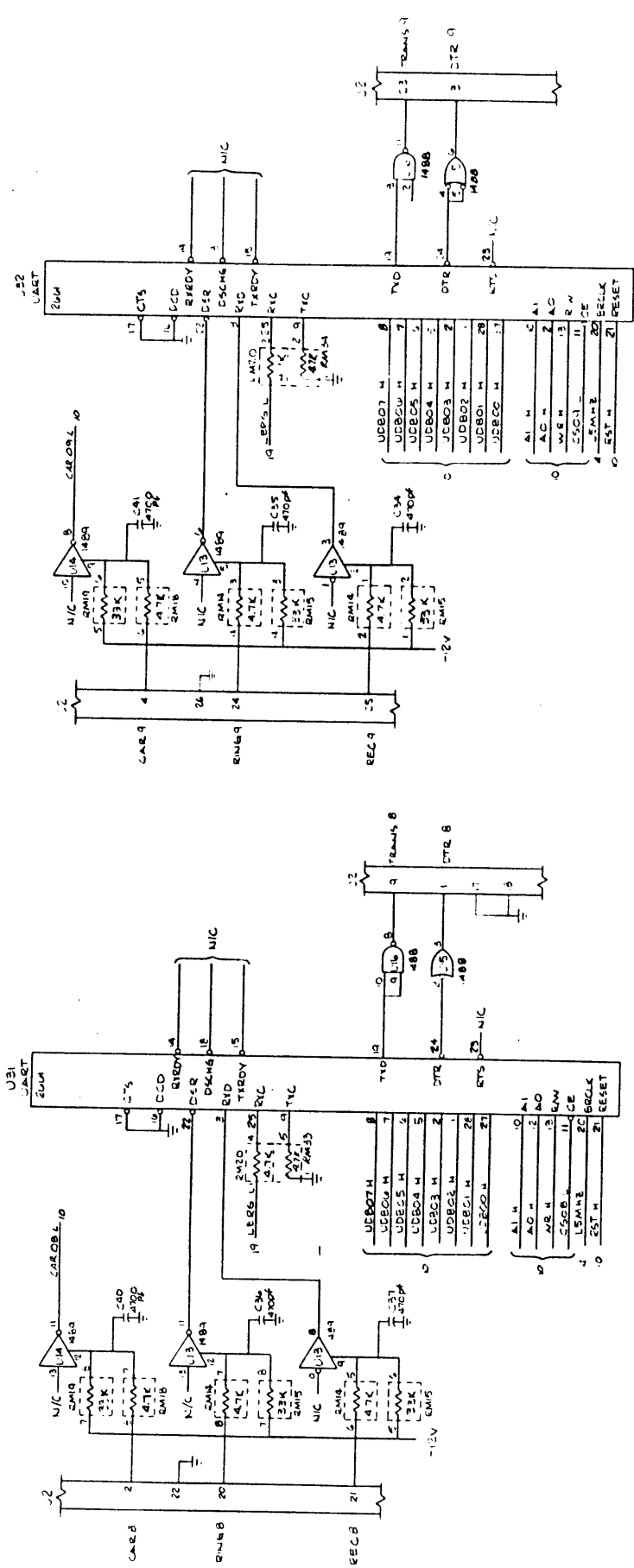
CHANNEL 4



CHANNEL 7

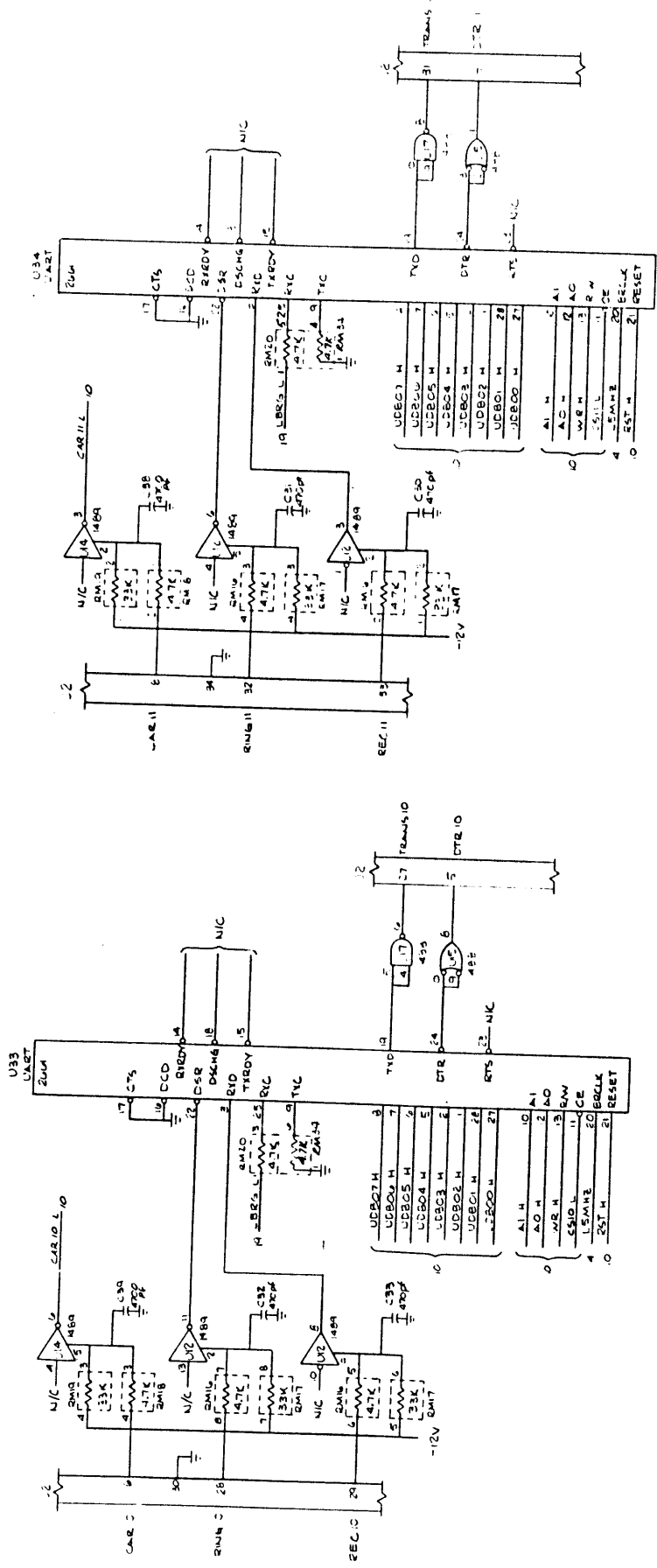


CHANNEL 6



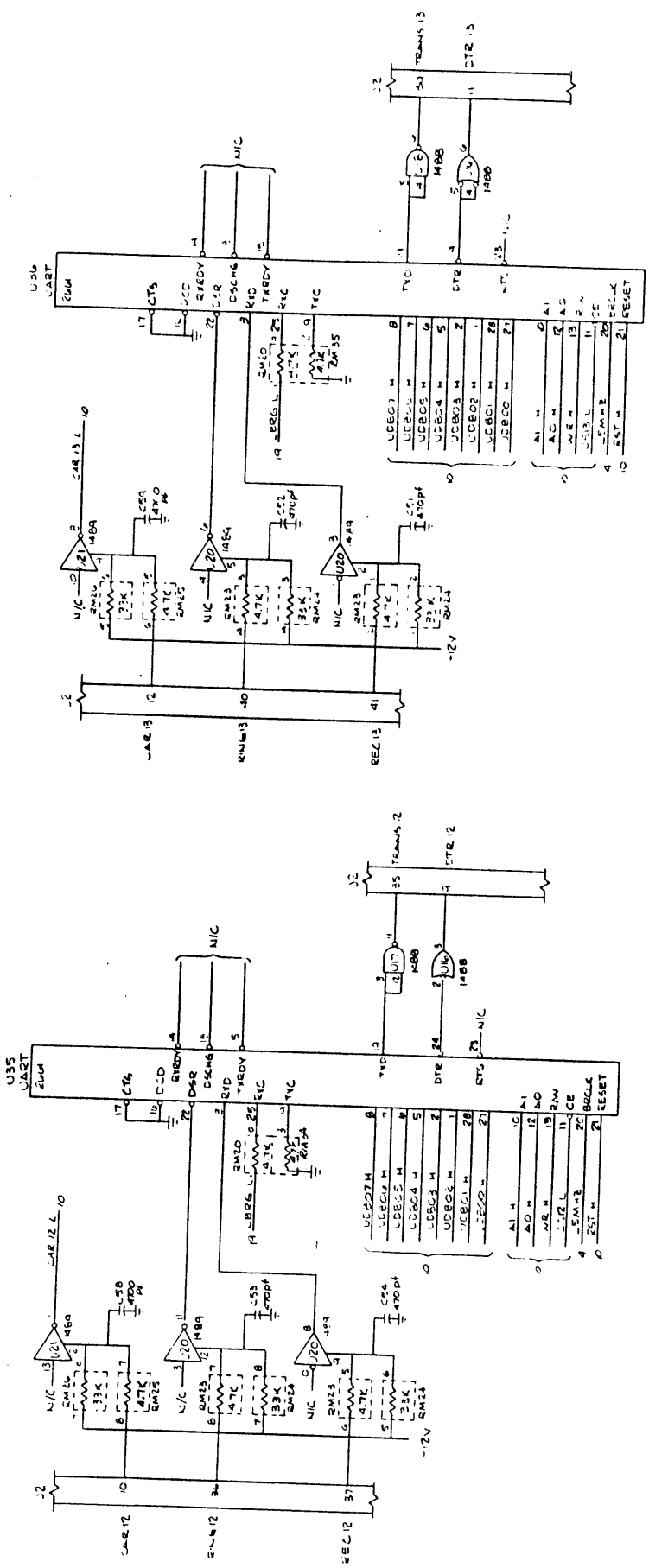
CHANNEL 8

CHANNEL 9



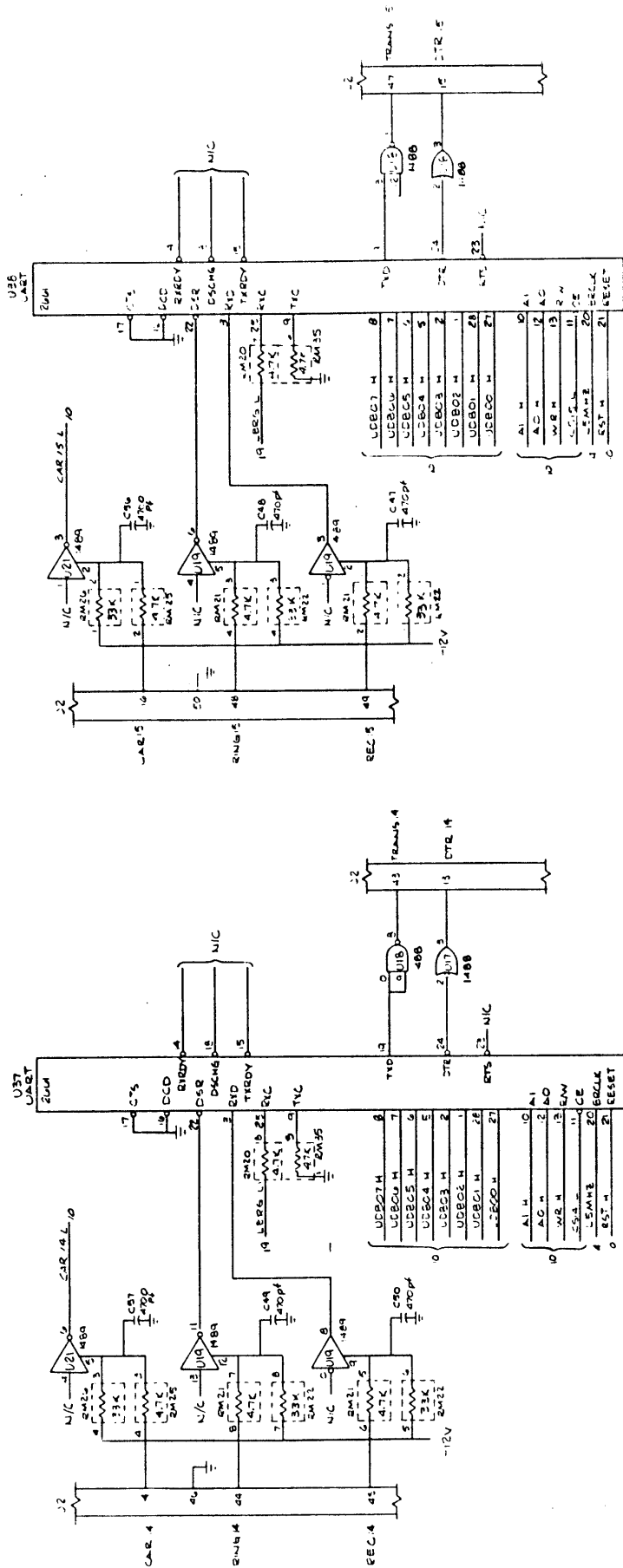
CHANNEL I

CHANNEL II



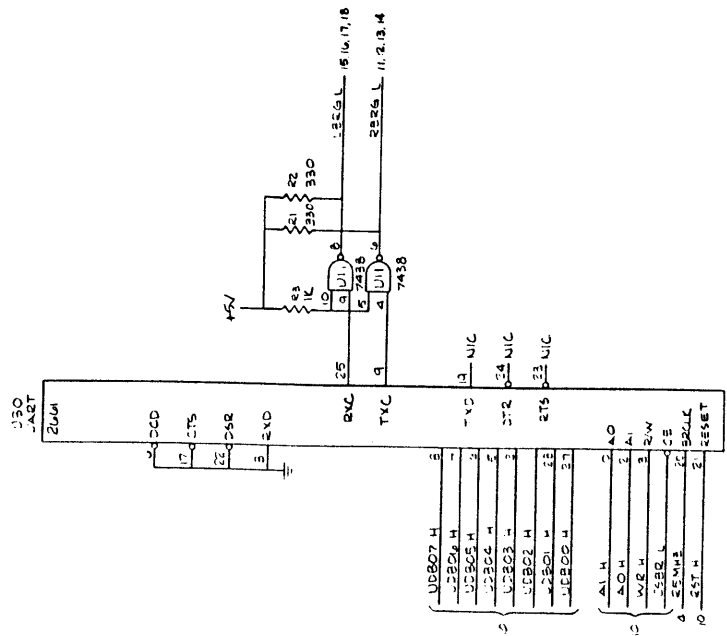
CHANNEL 12

CHANNEL 13



CHANNEL 14

TABLE 14



BAC RATE GENERATOR