

ZONE	LTN	DESCRIPTION	DATE	APPROVED
A	ELO # 0000	INITIAL RELEASE	2/11/82	AD/DA
B	ELO # 0000	INCORPORATED	2/11/82	AD/DA
C	ELO # 0000	INCORPORATED	2/11/82	AD/DA
D	ELO # 0000	INCORPORATED	2/11/82	AD/DA

REF DES.	QIBS USED (PER TOTAL)	PART NUMBER
D13	3/4	74S08
D15	3/4	74S08
D18	2/4	74S08
D19	2/4	74S08
D20	2/3	74S08
D21	2/3	74S08
D22	4/6	74S08
D23	3/4	74S08
D24	1/2	74S08
D25	2/3	74S08
D26	3/4	74S08
D27	1/4	74S08
D28	3/4	74S08
D29	3/4	74S08
D30	1/2	74S08
D31	1/4	74S08
D32	1/4	74S08
D33	1/4	74S08
D34	1/4	74S08
D35	1/4	74S08
D36	1/4	74S08
D37	1/4	74S08
D38	1/4	74S08
D39	1/4	74S08
D40	1/4	74S08
D41	1/4	74S08
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D97	1/4	74S08
D98	1/4	74S08
D99	1/4	74S08
D100	1/4	74S08

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1 INTERRUPT END H
2 INT CHNL L
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PRESENT L
BUS MBA INT B00 H
BUS MBA INT B01 H
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ABO OR L
CHECK RD BIT H
INTERUPT EPO L
MULTI XMIT FEL H
WRITE SEQ FEL H
RD ADDR H
DT READ H
CMD REQ L
PARITY FEL H
SET CORRECT RD L
CLK DIB1 H
ENAB WDZ MUX H
INT COND L
INT DIF T1 CLK L
ENAB H A H
ENAB G A H
ENAB B A H
ENAB INT B10 H
ENAB INT B11 H
ENAB INT B12 H
ENAB INT B13 H
ENAB INT B14 H
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INT DIF T1 CLK L
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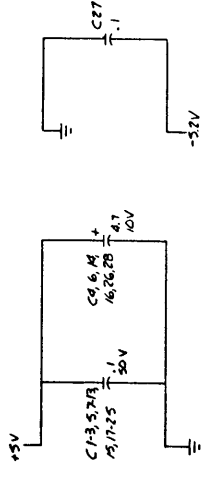
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REFERENCE DESIGNATIONS NOT USED

RESISTOR	R1, 5, 11, 21
RESISTOR MODULE	RM 2

LAST REFERENCE DESIGNATION USED

CAPACITOR	C30
INTEGRATED CIRCUIT	D175
RESISTOR	R54
RESISTOR MODULE	RM 1
SWITCH	SW 1
TRANSFORMER	TS

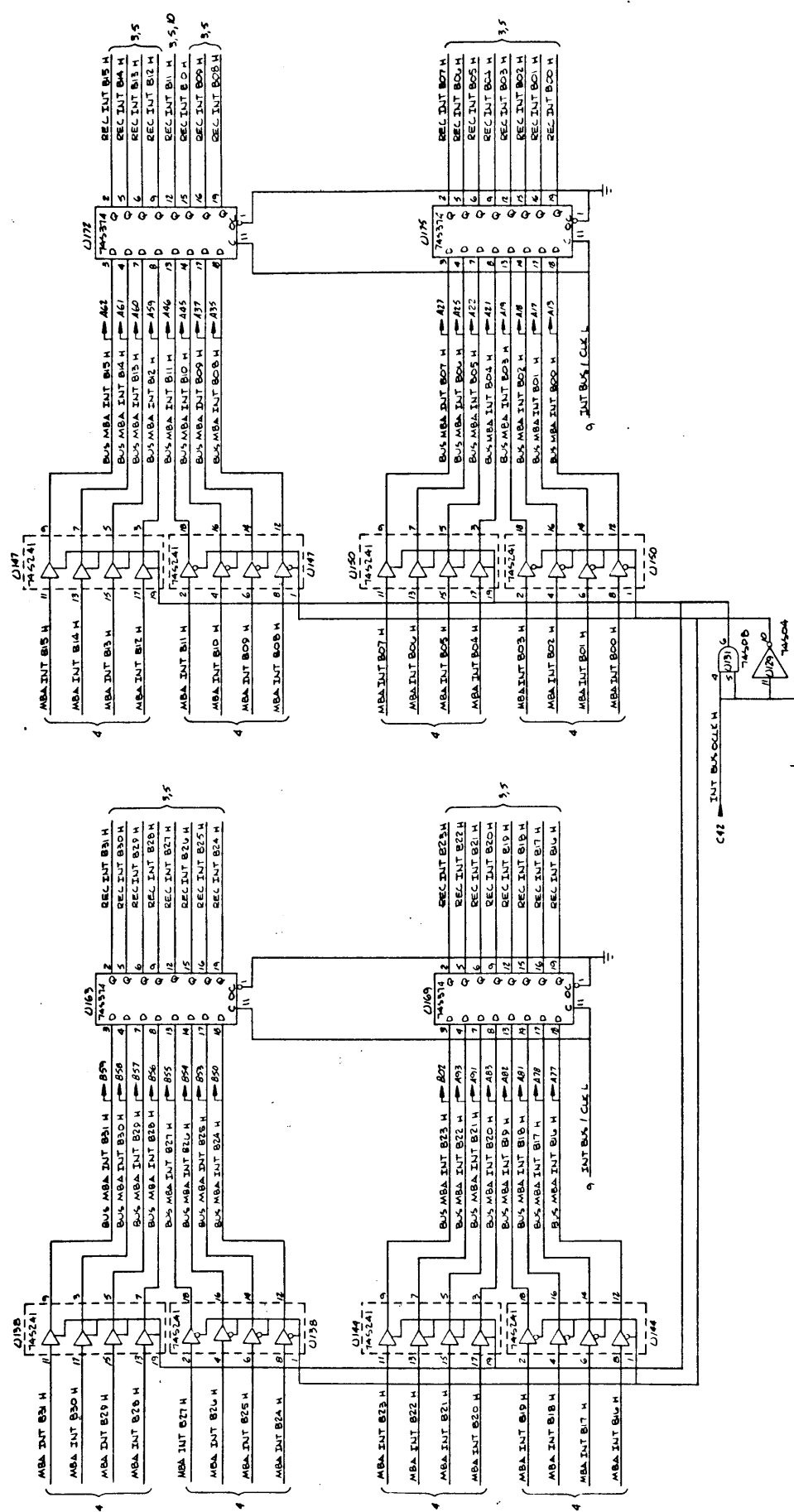


SHEET	NO.	DESCRIPTION	DATE	APPROVED
SHEET 13	TR EARLY CONTROL, CMT BLK W/ITZ			
SHEET 12	4-BIT BUS ARBITRATION CONTROL			
SHEET 11	4-BIT FAULT STATUS, POWER UP/DOWN STATUS			
SHEET 9	DATA DATA CONTROL, POWER CONTROL, DESELECT AND SELECT, 4-BIT DATA REGENERATOR AND CMT CLK GENERATOR			
SHEET 8	4-BIT BUS COMMAND CONTROL			
SHEET 7	FUNCTION CODE AND MASK BIT LOGIC, CMT BUS CONTROL			
SHEET 6	CMT BUS TRANSMITTER			
SHEET 5	4-BIT ADDRESS/CMT DPO READ BUFFER, CMT READ DATA BUFFER			
SHEET 4	4-BIT ADDRESS/CMT DPO WRITE BUFFER, CMT WRITE DATA BUFFER			
SHEET 3	CMT ADDRESS REGISTER, CMT DPO WRITE DATA BUFFER			
SHEET 2	MBA INTERNAL BUS TRANSMITTER			

EMULEX CORPORATION
SANTA ANA, CALIF.

DATE: 2/11/82
DRAWN BY: PLATY
CHECKED BY: []
ENGINEER: []
APPROVED BY: []
TITLE: SCHEMATIC DIAGRAM - 4478 BUS TRANSMITTER BOARD
SHEET NO: 13 OF 13

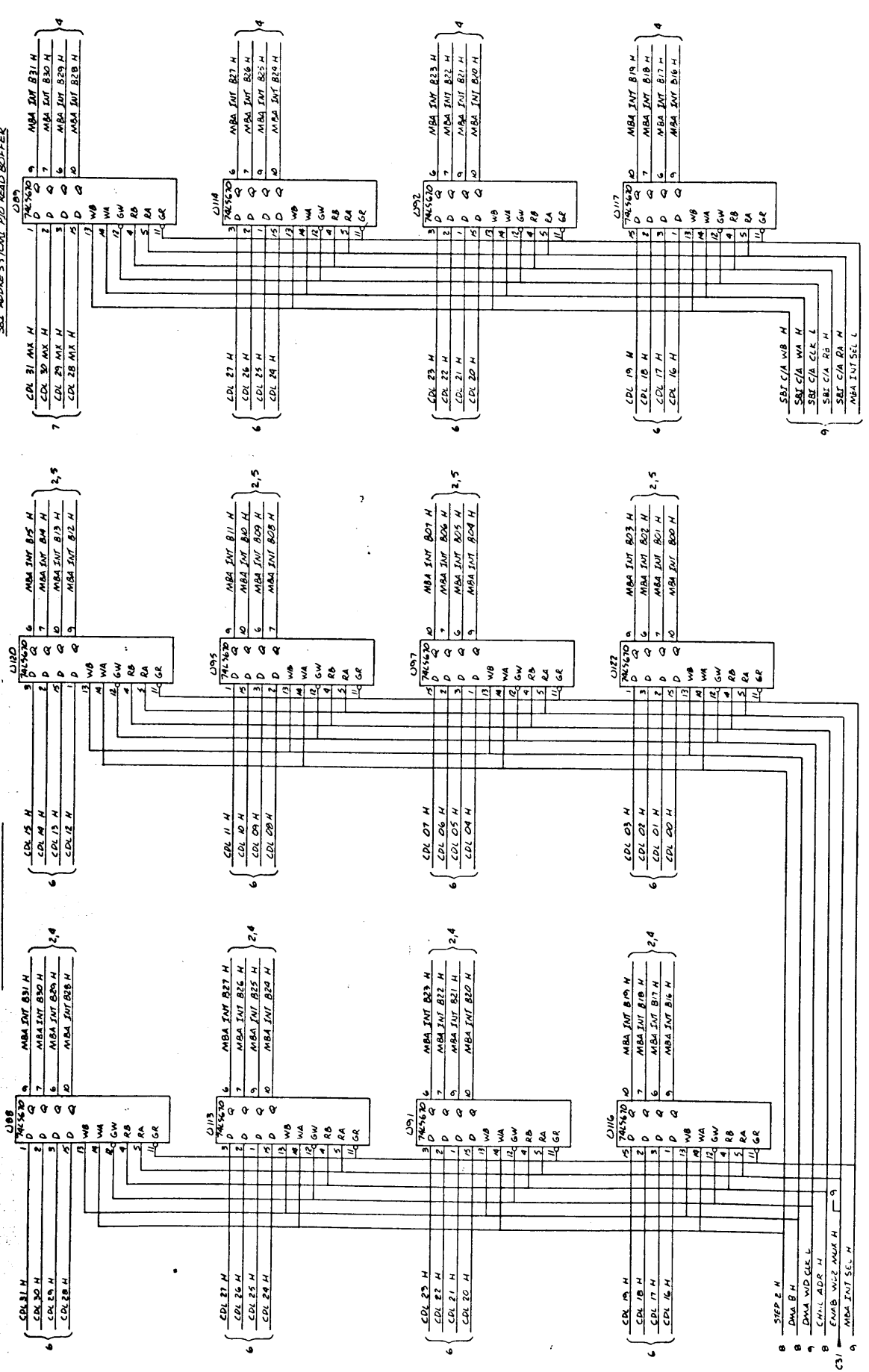
NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS
2. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.



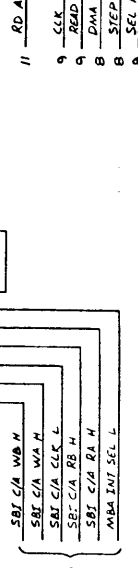
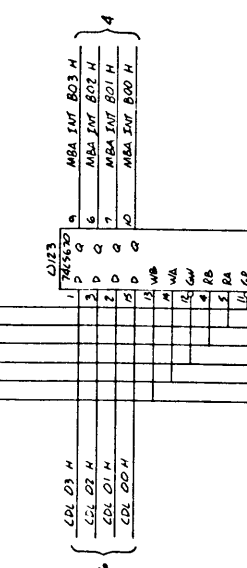
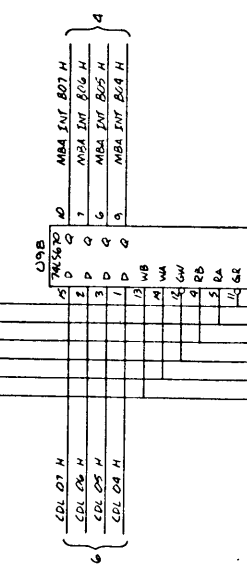
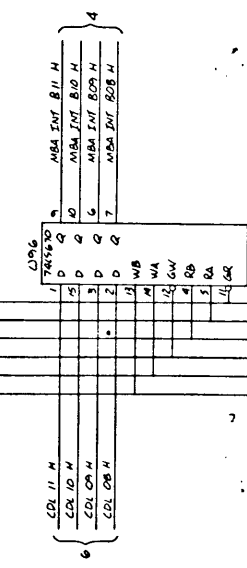
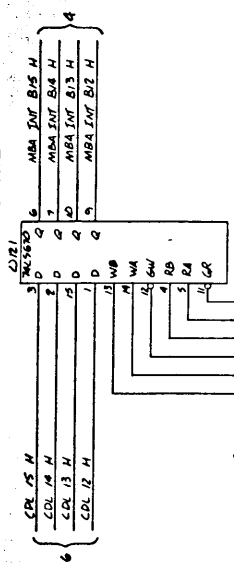
MBA INTERNAL BUS TRANSCEIVERS

SAT WRITE DATA REGISTER

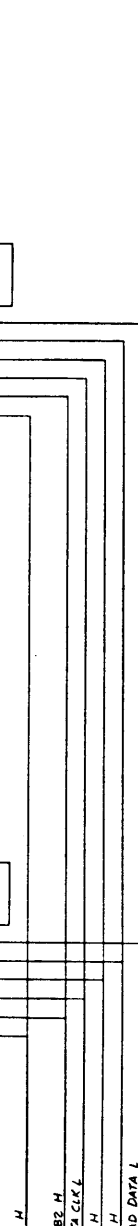
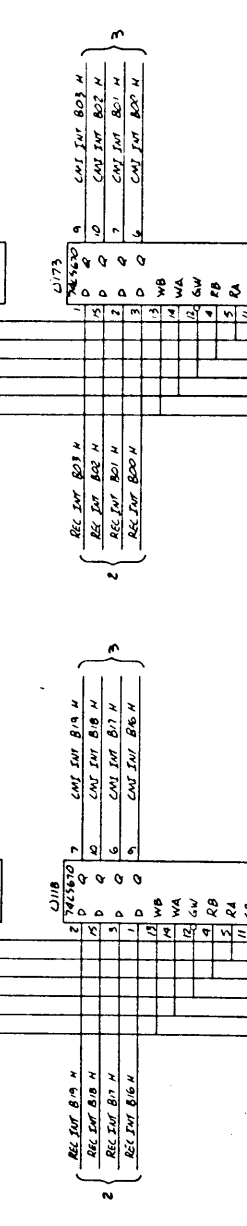
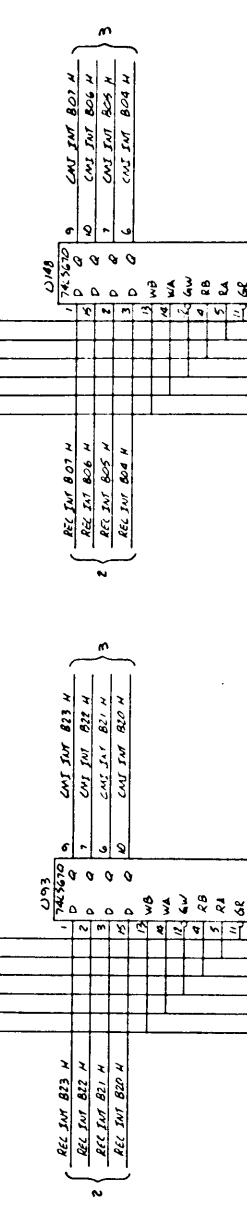
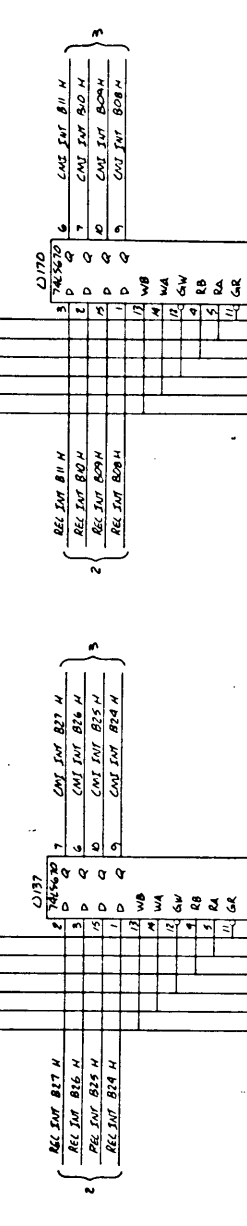
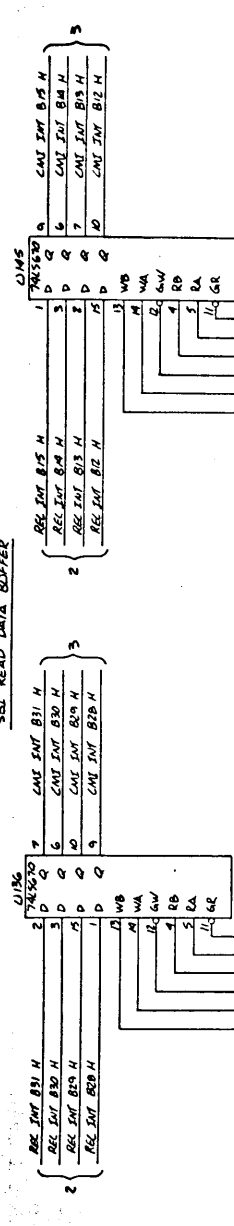
SAT ADDRESS COUNT DTD READ BUFFER

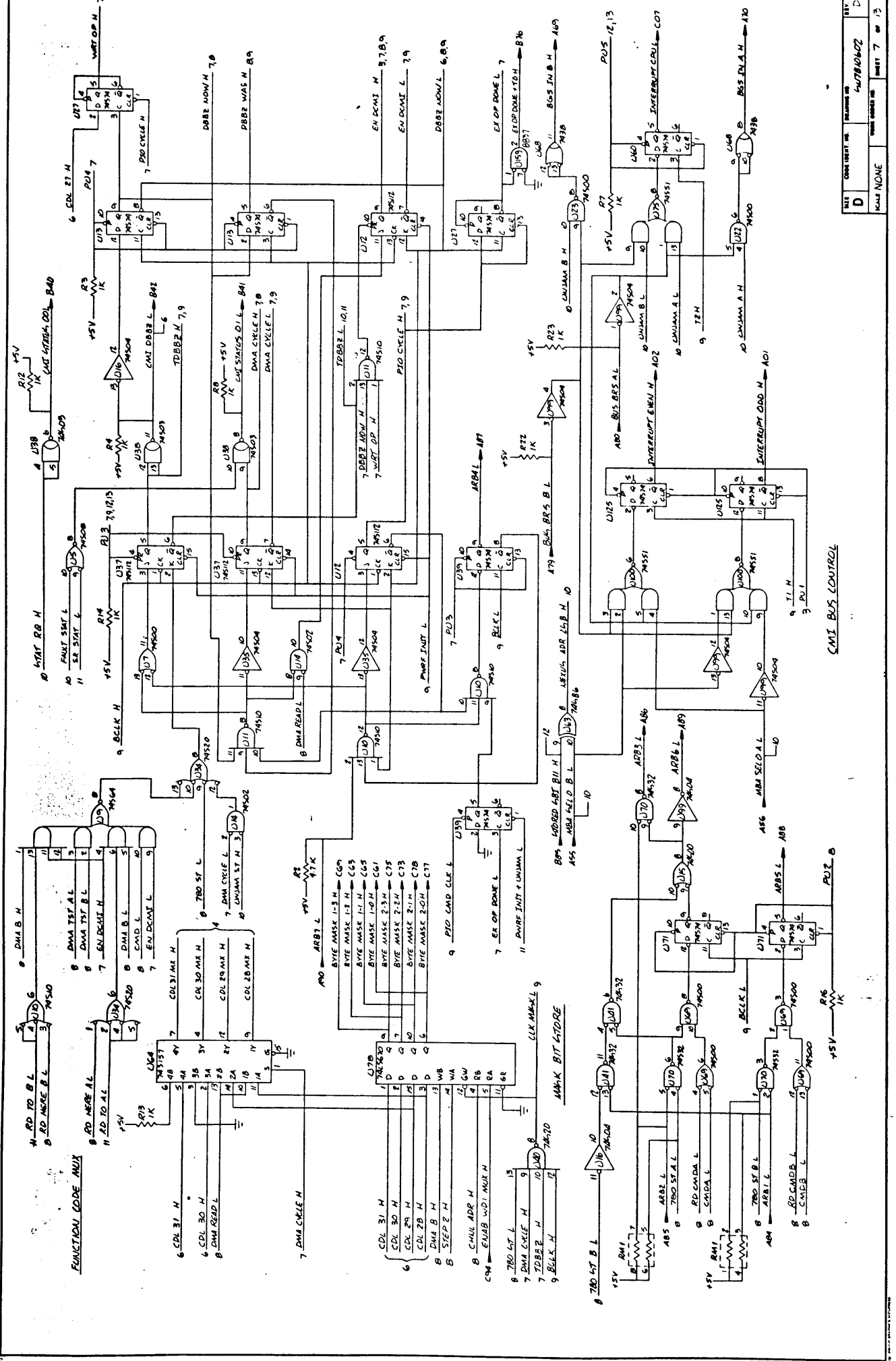


SBI ADDRESS/CMI PID READ BUFFER



SBI READ DATA BUFFER





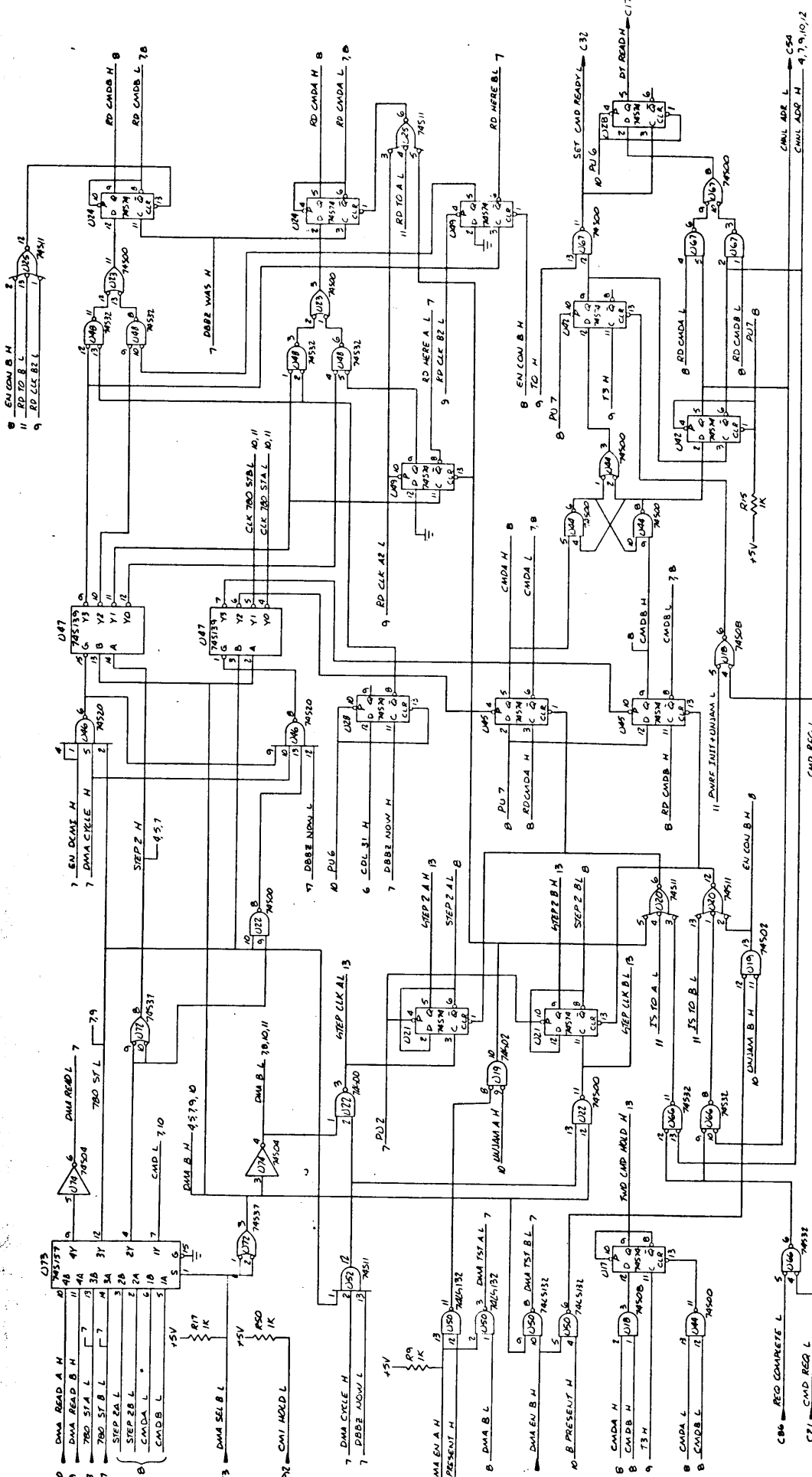
FUNCTIONAL CODE MUX

- 4 RD TO B L
- 5 RD TO B L
- 6 DMA TST A L
- 7 DMA TST B L
- 8 EN DMAS H
- 9 DMAB L
- 10 DMAB L
- 11 EN DMAS L
- 12 CDL ST L
- 13 CDL ST L
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CMI BUS CONTROL



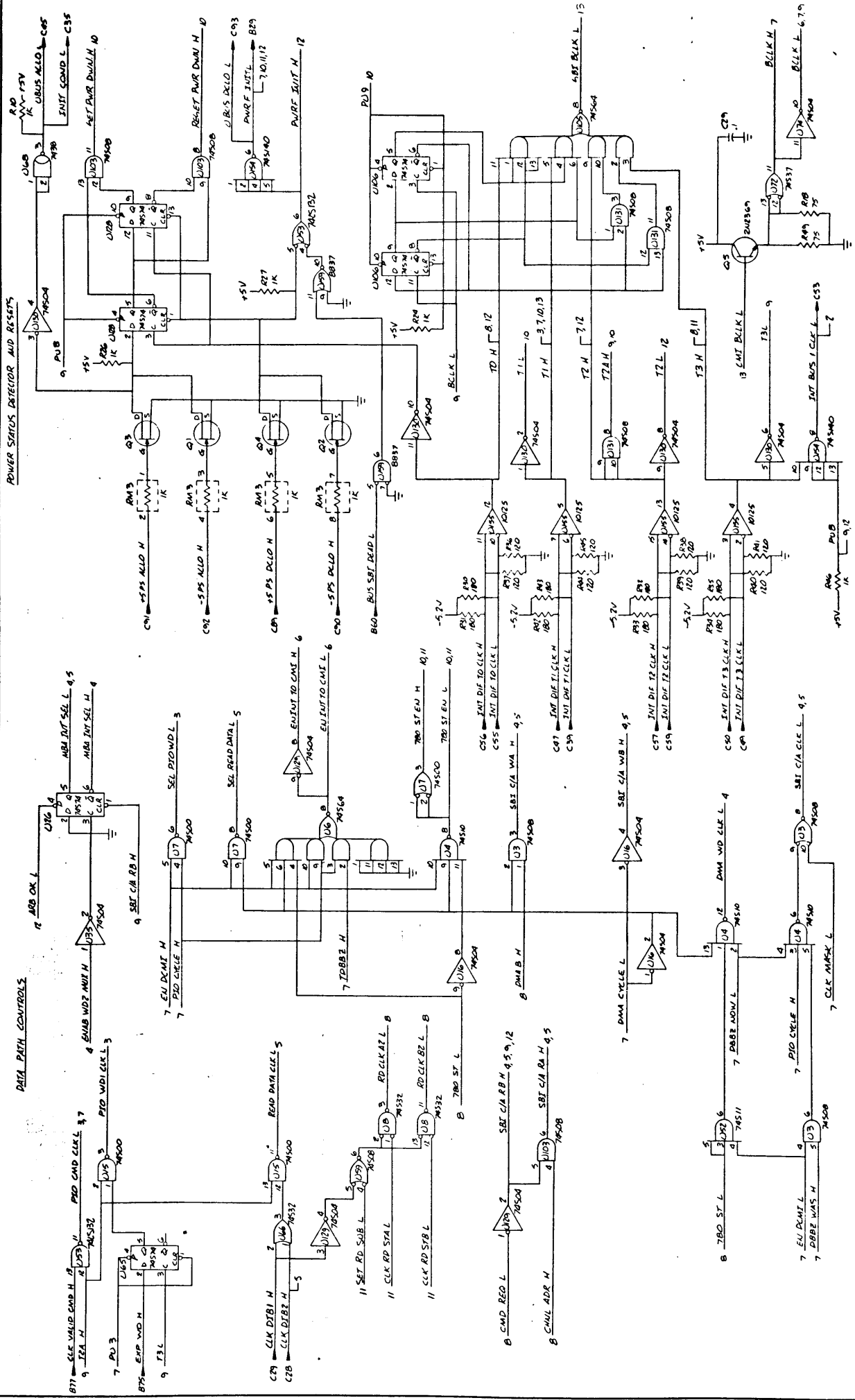
SBI BUS COMMAND CONTROL

REV	DATE	BY
D	5/28/80	WJ
SCALE	NONE	WORK SHEET NO.
		SHEET 6 OF 13

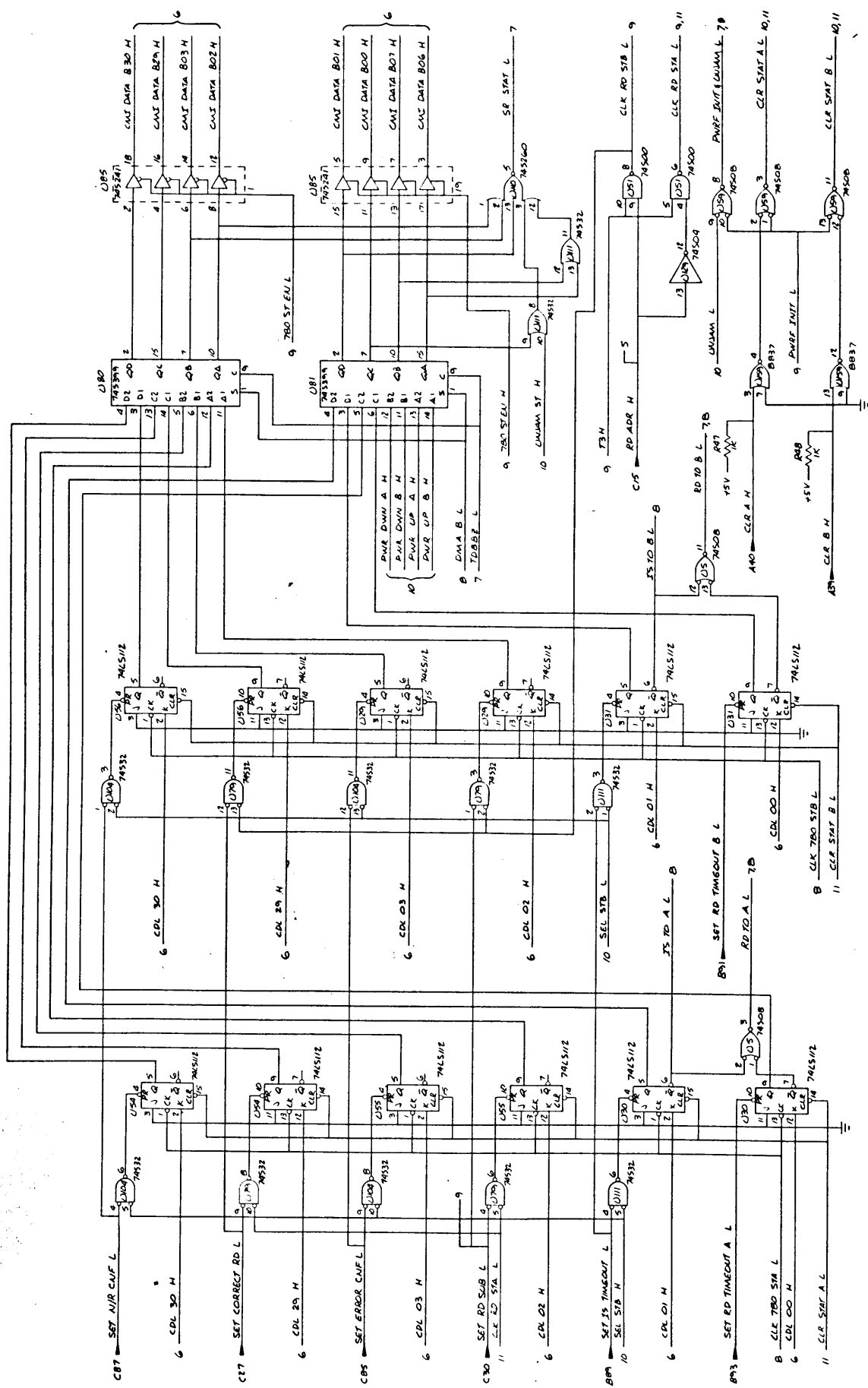
DATA PATH CONTROLS

POWER STATUS DETECTOR AND RESETS

SBT CLOCK RECEIVERS AND CNT CLK GENERATOR



REV	DATE	BY
D	4/28/80	07
CHKD BY	DATE	BY
None	None	None
SHEET 9 OF 13		



CS/SR STATUS

REV	D
SCALE	NONE
DATE	08/10/62
DESIGNED BY	
CHECKED BY	
INSTRUMENT	
SHEET	11 OF 15

