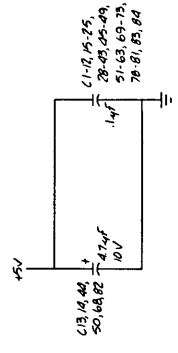


REFERENCE DESIGNATION	VALUES USED PER TOTAL	PART NUMBER
Q19	2/3	74640
Q31	1/2	74649
Q40	1/4	746132
Q49	3/4	74600
Q62	1/4	746408
Q67	3/4	746432
Q68	1/2	746434
Q75	3/4	74600
Q77	2/3	74640
Q78	1/4	746408
Q80	3/4	746400
Q85	3/4	74600
Q92	3/6	74608
Q97	4/6	746414
Q104	3/4	74658
Q112	2/4	746407
Q113	5/6	8837

LAST REFERENCE DESIGNATION USED	
CAPACITOR	C84
CONNECTOR	J3
DIODE	D14
INTEGRATED CIRCUIT	U14
JUMPER	C
REGULATOR	R29
RESISTOR MODULE	RAM5
SWITCH	SW6



TEST CONNECTOR

J3
1 OV
2 1
3 OV
4 4
5 OV
6 EX +50P H
7 OV
8 EXT CLKX L
9 OV
10 EX RESET L
11 OV
12 OV
13 OV
14 PA11 B+H
15 PA10 H
16 PA09 H
17 PA08 H
18 PA07 H
19 PA06 H
20 PA05 H
21 PA04 H
22 PA03 H
23 PA02 H
24 PA01 H
25 PA00 H
26 OV

J2

1 OV
2 1A 1A04 L
3 1A 1A03 L
4 1A 1A02 L
5 1A 1A01 L
6 1A 1A00 L
7 1B DBA4 L
8 1B DBA3 L
9 1B DBA2 L
10 1B DBA1 L
11 1B A2 L
12 1B A1 L
13 1B A0 L
14 1B WR L
15 1B BIT 7 L
16 1B BIT 6 L
17 1B BIT 5 L
18 1B BIT 4 L
19 1B BIT 3 L
20 1B BIT 2 L
21 1B BIT 1 L
22 1B BIT 0 L
23 OV
24
25
26 OV RESET L
27 1B SM CK H
28 1B SM CK H
29 1B SM CK L
30 1B SM CK L
31 OV
32 1B CE L
33 1B CE L
34 OV

TEST CONNECTOR

J1
1 OV
2 0B00 H
3 0B01 H
4 0B02 H
5 0B03 H
6 0B04 H
7 0B05 H
8 0B06 H
9 0B07 H
10 OV
11
12
13
14
15
16
17 OV EX TEST H
18 OV
19 OV
20

SWITCH LOCATIONS

SW1	9
SW2	9
SW3	6
SW4	3, 5, 9
SW5	9
SW6	8

JUMPER LOCATIONS

A, B, C	4
---------	---

1	2
CA1 B04 APR 20V H	B CA2 +5V
CB1 B04 APR 20V H	B CB2 OV
CC1 B04 PA L	B CC2 OV
CD1	B CD2 B04 D15 L
CE1	B CE2 B04 D14 L
CF1	B CF2 B04 D13 L
CG1	B CG2 B04 D12 L
CH1 B04 D11 L	B CH2 B04 D10 L
CI1	B CI2 B04 D09 L
CJ1	B CJ2 B04 D08 L
CK1	B CK2 B04 D07 L
CL1	B CL2 B04 D06 L
CM1 B04 D10 L	B CM2 B04 D05 L
CN1	B CN2 B04 D04 L
CO1	B CO2 B04 D03 L
CP1	B CP2 B04 D02 L
CQ1 B04 PB L	B CQ2 B04 D01 L
CR1	B CR2 B04 D00 L
CS1	B CS2 B04 D00 L
CT1 OV	B CT2 B04 D00 L
CU1	B CU2 B04 D00 L
CV1	B CV2 B04 D00 L

1	2
BA1	B A2 +5V
BB1	B B2 OV
BC1	B BC2 OV
BD1	B BD2 OV
BE1	B BE2 OV
BF1	B BF2 OV
BG1	B BG2 OV
BH1	B BH2 OV
BI1	B BI2 OV
BJ1	B BJ2 OV
BK1	B BK2 OV
BL1	B BL2 OV
BM1	B BM2 OV
BN1	B BN2 OV
BO1	B BO2 OV
BP1	B BP2 OV
BQ1	B BQ2 OV
BR1	B BR2 OV
BS1	B BS2 OV
BT1	B BT2 OV
BV1	B BV2 OV

1	2
AA2 +5V	
AB2 OV	
AC2 OV	
AD2	
AE2	
AF2	
AG2	
AH2	
AI2	
AJ2	
AK2	
AL2	
AM2	
AN2	
AO2	
AP2	
AQ2	
AR2	
AS2	
AT2	
AU2	
AV2	

1	2
FA1	B FA2 +5V
FB1	B FB2 OV
FC1	B FC2 OV
FD1	B FD2 OV
FE1	B FE2 OV
FF1	B FF2 OV
FG1	B FG2 OV
FH1	B FH2 OV
FI1	B FI2 OV
FJ1	B FJ2 OV
FK1	B FK2 OV
FL1	B FL2 OV
FM1	B FM2 OV
FN1	B FN2 OV
FO1	B FO2 OV
FP1	B FP2 OV
FQ1	B FQ2 OV
FR1	B FR2 OV
FS1	B FS2 OV
FT1	B FT2 OV
FV1	B FV2 OV
FW1	B FW2 OV
FX1	B FX2 OV
FY1	B FY2 OV
FZ1	B FZ2 OV

1	2
EA1	B EA2 +5V
EB1	B EB2 OV
EC1	B EC2 OV
ED1	B ED2 OV
EE1	B EE2 OV
EF1	B EF2 OV
EG1	B EG2 OV
EH1	B EH2 OV
EI1	B EI2 OV
EJ1	B EJ2 OV
EK1	B EK2 OV
EL1	B EL2 OV
EM1	B EM2 OV
EN1	B EN2 OV
EO1	B EO2 OV
EP1	B EP2 OV
EQ1	B EQ2 OV
ER1	B ER2 OV
ES1	B ES2 OV
ET1	B ET2 OV
EU1	B EU2 OV
EV1	B EV2 OV
EW1	B EW2 OV
EX1	B EX2 OV
EY1	B EY2 OV
EZ1	B EZ2 OV

1	2
DA1	B DA2 +5V
DB1	B DB2 OV
DC1	B DC2 OV
DD1	B DD2 OV
DE1	B DE2 OV
DF1	B DF2 OV
DG1	B DG2 OV
DH1	B DH2 OV
DI1	B DI2 OV
DJ1	B DJ2 OV
DK1	B DK2 OV
DL1	B DL2 OV
DM1	B DM2 OV
DN1	B DN2 OV
DO1	B DO2 OV
DP1	B DP2 OV
DQ1	B DQ2 OV
DR1	B DR2 OV
DS1	B DS2 OV
DT1	B DT2 OV
DU1	B DU2 OV
DV1	B DV2 OV

SHEET 10 LINK NUMBER REGISTER, LINK DATA REGISTER, LINK CONTROL, LINK INTERFACE
 SHEET 9 ADDRESS OFFSET, ADDRESS DECODE, MAX GROUP NO. OPTION SWITCHES
 SHEET 8 JUMPER INTERFACE CONTROL, 200 MA DECAN
 SHEET 7 JUMPER ADDRESS REGISTER, JUMPER DATA REGISTER
 SHEET 6 JUMPER CONTROL LOGIC
 SHEET 5 TEST CONDITIONS, TEST COMMANDS, TEST CONNECTOR B04 AND D10 VECTOR AND VECTOR PROGRAMMED ADDRESS WIRE 640
 SHEET 4 TEST CONNECTOR A MAX. ALL. DATA. FAULT ON LINE RLM ADDRESS REGISTER
 SHEET 3 TEST CONNECTOR A MAX. ALL. DATA. FAULT ON LINE RLM ADDRESS REGISTER

THIS DRAWING CONTAINS INFORMATION THAT IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE AND IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE. DATE OF DECLASSIFICATION: 1-1-88 BY: 1043

SCALE: 1:1

DATE: 10/27/89

DESIGNED BY: J. P. ...
 CHECKED BY: J. P. ...
 ENGINEER: J. P. ...

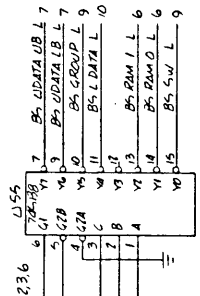
INULEX CORPORATION
 COSTA MESA, CALIF.

TITLE: SCHEMATIC DIAGRAM, U32
 COMMUNICATIONS CONTROLLER

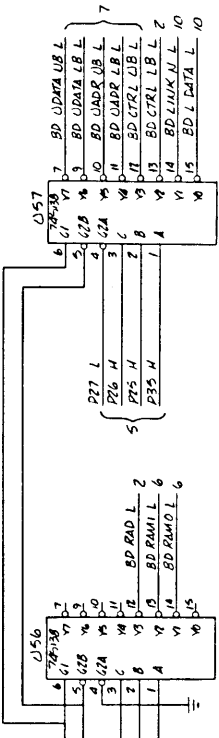
FILE: U3210601
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 SHEET 1 OF 10

NOTES: UNLESS OTHERWISE SPECIFIED,
 1 CAPACITANCE VALUES ARE IN MICROFARADS,
 2 RESISTANCE VALUES ARE IN OHMS, 15% TOL.

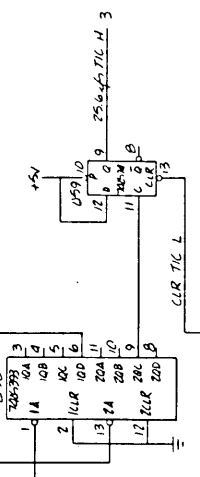
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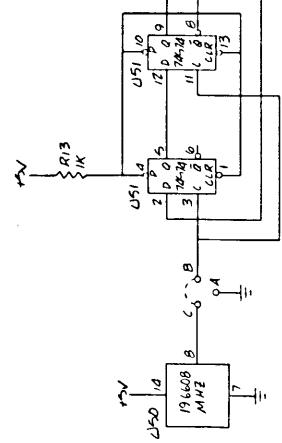
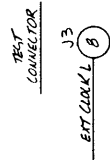
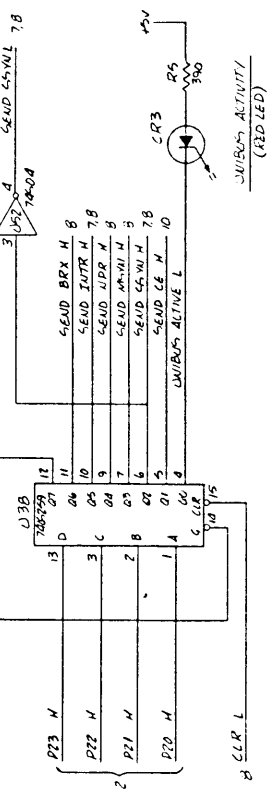
RAM DESTINATION DECODE



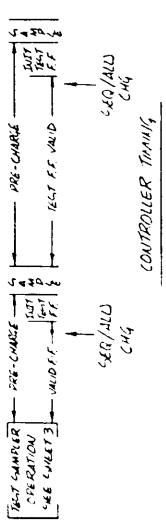
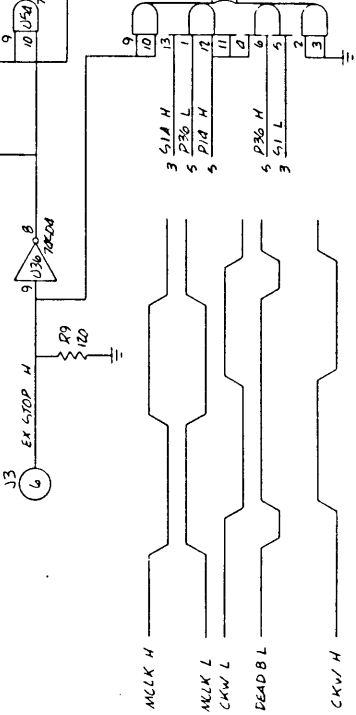
256-45 TIMER



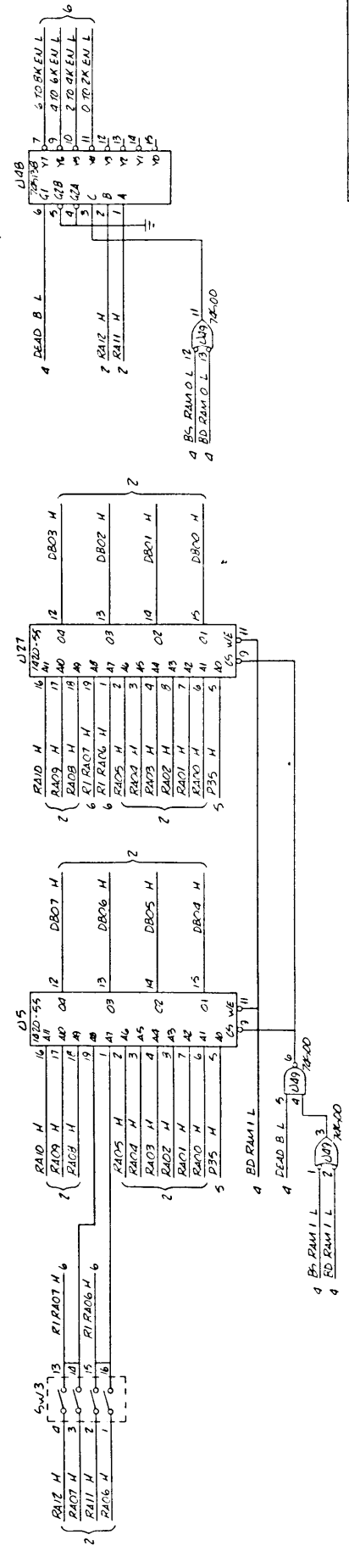
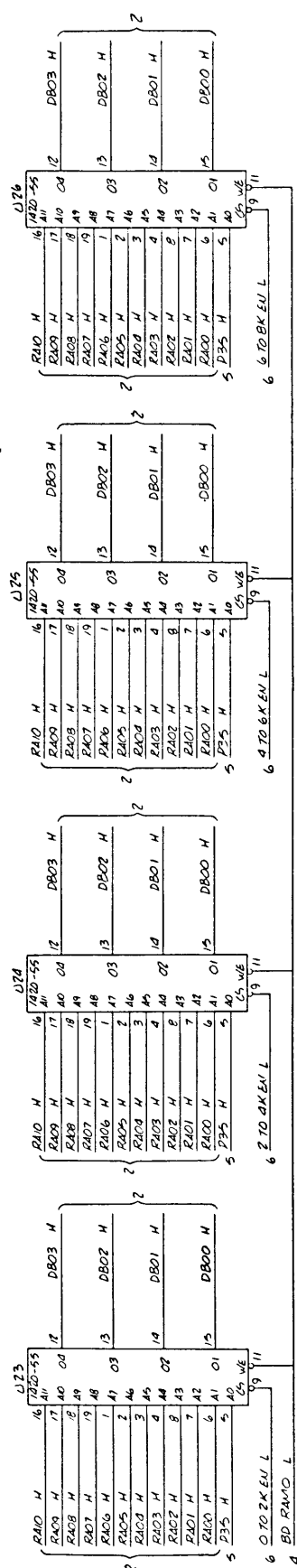
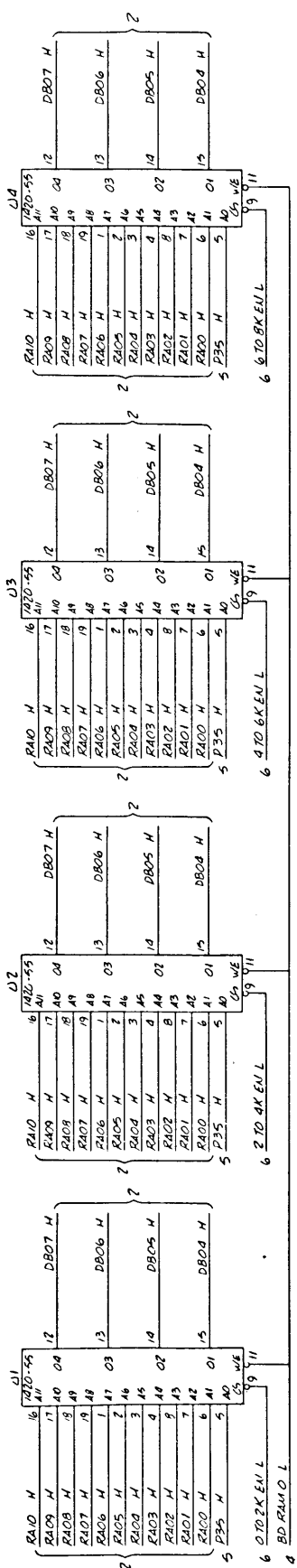
I/O CONTROL REG

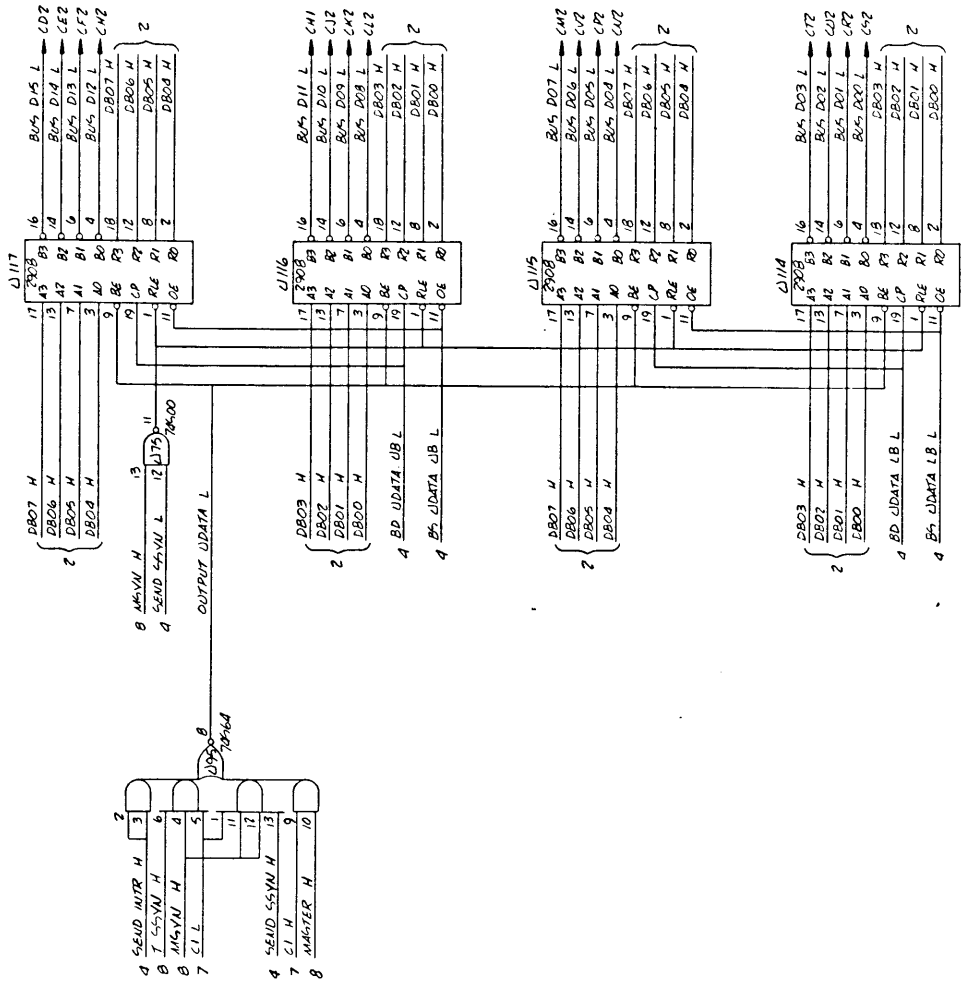
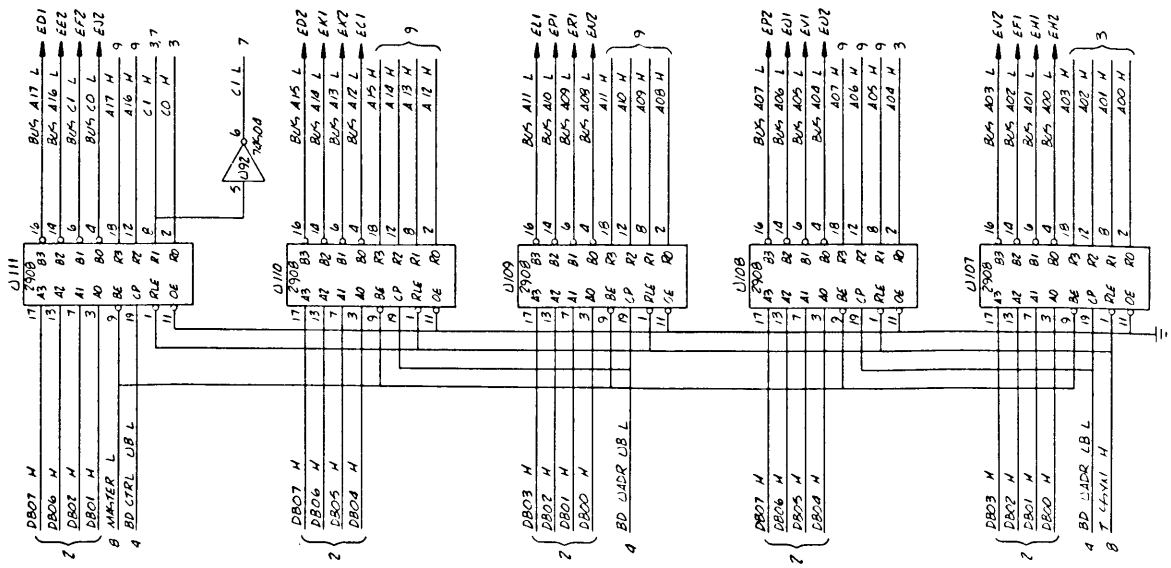


TEST CONNECTOR



RAM ARRAY

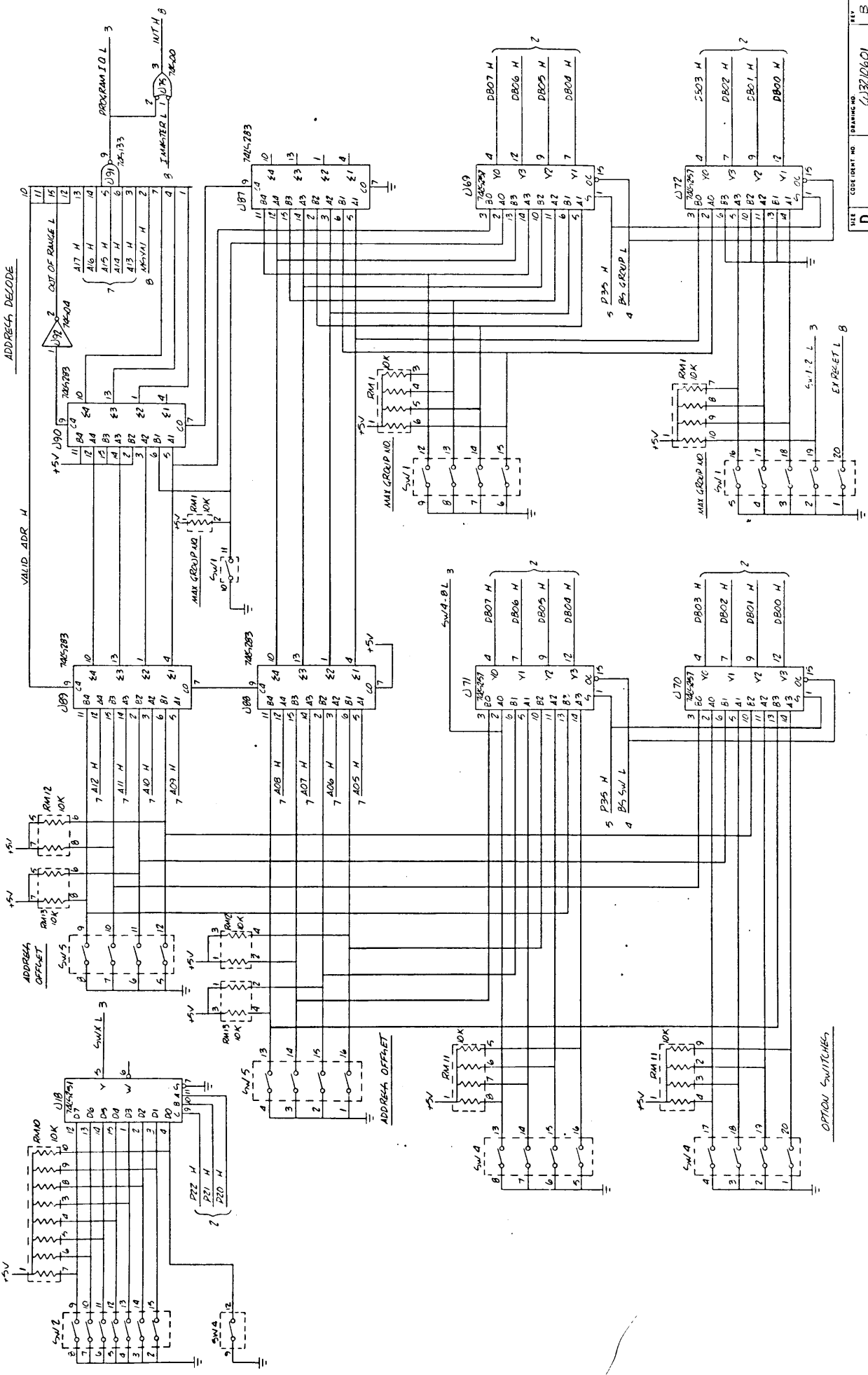




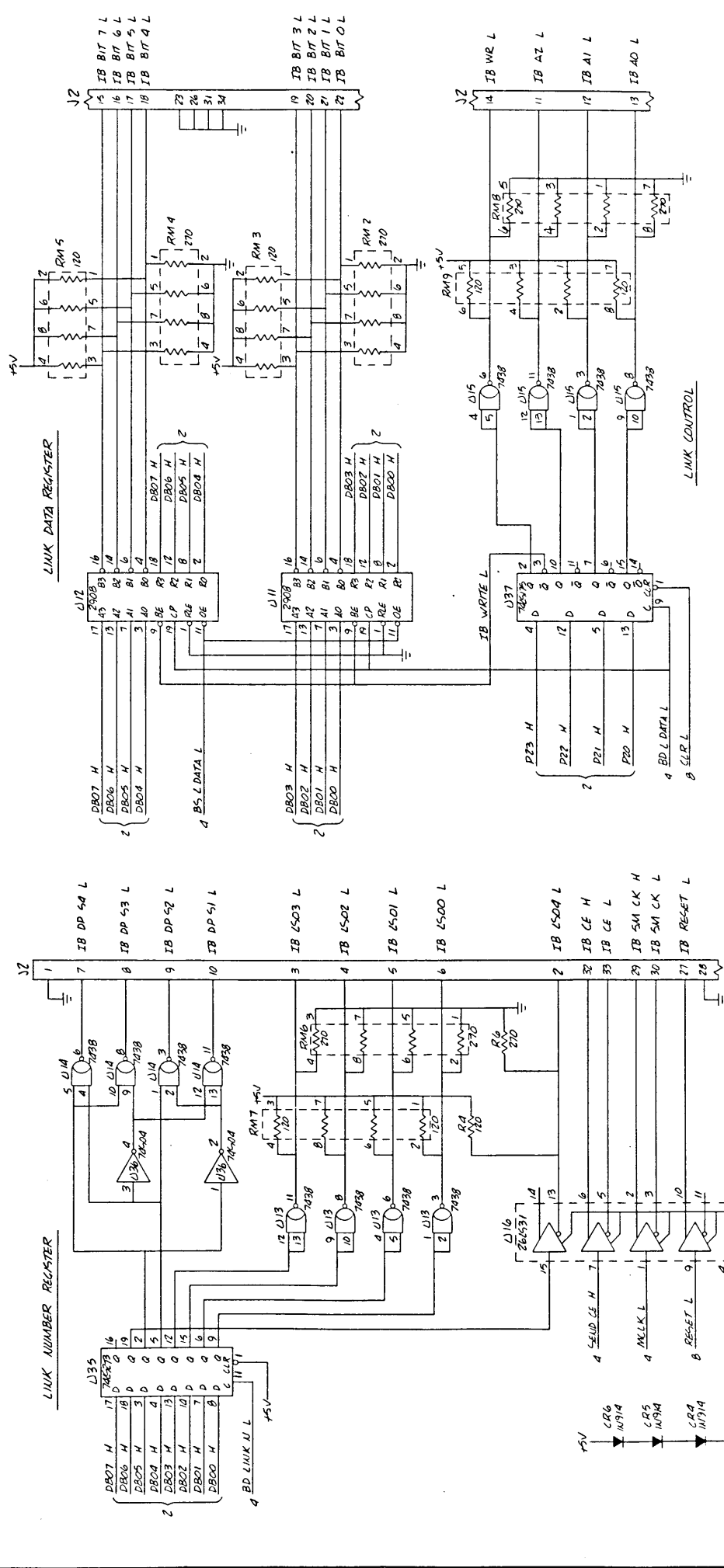
ADDRESS REGISTER

DATA REGISTER

ADDRESS DECODE



OPTION SWITCHES



LINK INTERFACE

LINK DATA REGISTER

LINK NUMBER REGISTER

LINK CONTROL

LINK CONTROL