G15D TECHNICAL MANUAL

REVISION #1

PART II - THEORY OF OPERATION

Bendix Computer

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PREFACE

This manual is primarily for the purpose of clarifying the internal logic and technology of the G-15D. The detailed engineering drawings, series 3D286 - 3D300 (known as the "D-SIZED" or "DETAILED" prints), document the logical composition of the computer and can be understood by a computer engineer, in time, by deductive reasoning without supplementary material.

Since the drawings mentioned above are not necessarily for illustrative purposes, they are supplemented by the "SIMPLIFIED DRAWINGS" in PART I of this manual. These drawings attempt to illustrate the reasoning behind the circuits, while PART II attempts to explain the theory of operation. Additional documentary material will be supplied with each computer.

This manual assumes some knowledge on the part of the reader as to the overall composition and purpose of the computer. Furthermore, a basic knowledge of BINARY ARITHMETIC and BOOLEAN ALGEBRA is a prerequisite, although outlines of fundamental operations are provided in the APPENDIX of this manual (Section H).

The order in which subject matter is presented is such that the reader can start at the beginning and proceed, covering prerequisite material as he advances. For this reason, as the TABLE OF CONTENTS will reveal, some items may appear to be in inappropriate locations. References are provided to assist the reader in refreshing his memory or to satisfy his curiosity.

Maintenance techniques are not discussed to any great extent in this manual. Volumes would be required to do this subject justice. In general, engineering experience and the process of elimination should handle most problems which may arise. The CUSTOMER ENGINEERING department may always be consulted in the event of extraordinary problems.

In conclusion, the object of this manual is to guide the reader through the drawings which describe the computer, pointing out the purposes and reasoning behind the circuits without necessarily repeating in words the facts exhibited in the drawings.

TABLE OF CONTENTS

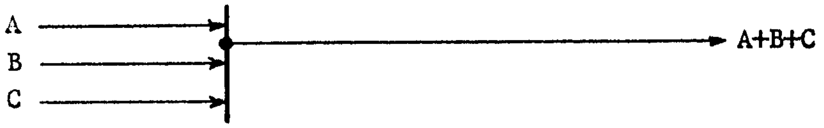
SECTION A

FUNDAMENTAL CIRCUITS

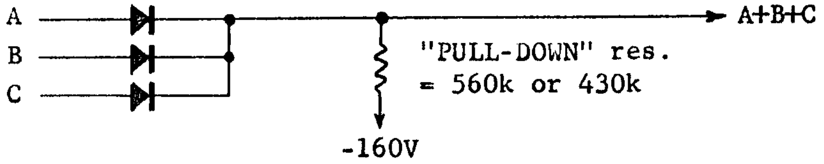
This section is devoted to the fundamental circuits which constitute the "building blocks" of which the G-15D is composed. It is suggested that the reader thoroughly digest this section prior to proceeding further, for in the sections to follow an understanding of these circuits is taken for granted.

"OR" GATES

A-1a An OR gate is a device for the purpose of yielding a high output signal if any of its input terms are high. Symbolically an OR gate is represented as shown:

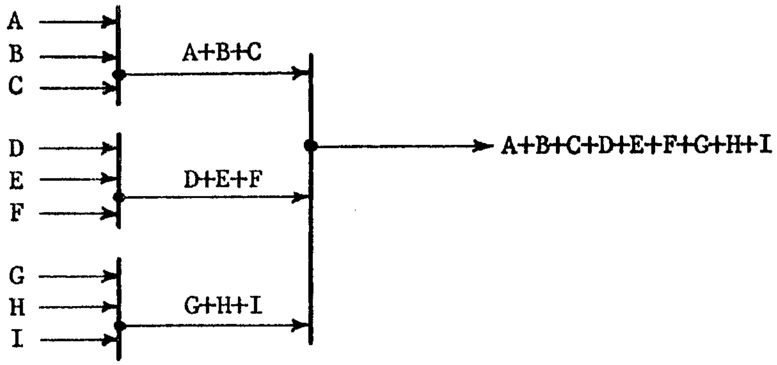


schematically:



A-1b Considering the connection of the diodes, the input terms are isolated from one another by diode back resistance. The common connection of the diodes will yield an output which, for all practical purposes, is short-circuited to the input term having the highest potential. Assuming the inputs are (individually) either at -20V or 0V, the output should be at the highest input potential. That is, if one or more input terms reach 0V the output will reach 0V; if none are above -20V, the output will be at -20V. The loading resistance to -160V is known as the PULL-DOWN resistor; its function is to "pull" the output potential "down", while the input terms pull it up.

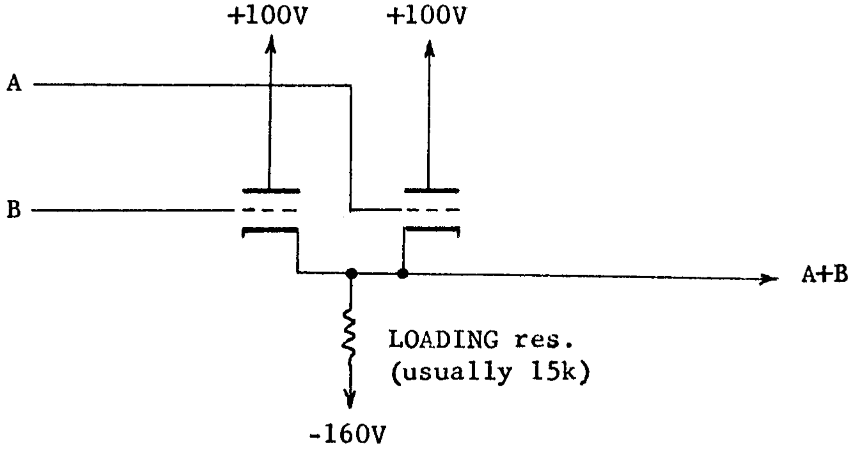
A-1c Should only one input term be high (0V), its diode must handle all of the current required to drop 160V across the PULL-DOWN resistor. The other diodes will be "biased off"; however, a certain amount of reverse current will exist in the "biased off" diodes. This will be a function of the reverse voltage applied (-20V) and the back resistance of each diode. As the number of terms entering an OR gate is increased, the back current loading problem increases. For this reason a limit is placed on how many terms can feed one OR gate. If more than the allowable limit is to be exceeded, a series of OR gates may be employed to relieve the problem. For example, if nine terms are to feed an OR gate, the following arrangement can be used:



A-1d Logically, the function is identical to that of a single nine-term OR gate. Although the total forward resistance may be increased by a trivial amount, the back resistance loading problem is substantially reduced. Drawing #3D293 illustrates the distribution of diodes comprising the "EB", which is a multi-term OR gate.

A-1e Dynamic properties: If an OR gate is fed by a square-wave, and the output is loaded by distributed capacitance to ground, the output signal will rise (from -20V to 0V) quite rapidly since the capacitance will discharge through the forward resistance of the active diode; however, when the output signal drops, the capacitance must charge through the PULL-DOWN resistor, which has a relatively high value. Hence, the decay time of the TRAILING EDGE of an OR gate's output signal is liable to be SLOW.

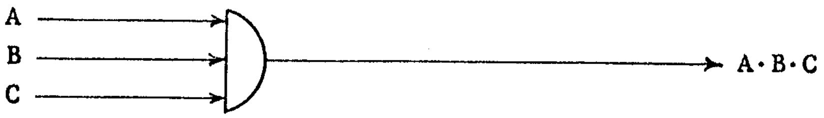
A-1f Cathode-follower OR gates: Cathode-followers may be used in the construction of an OR gate as follows:



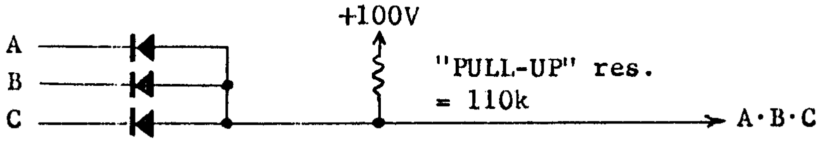
This circuit is advantageous in that (1) loading of the inputs is light, (2) inputs are isolated from the output, and (3) the circuit supplies a power boost to the output term. Only a few such gates exist in the G-15D. One such circuit may be seen on Drawing #3D293 - see "EB". (Cathode-follower OR gates are sometimes referred to as "FAST 'OR' GATES" since they do not suffer from the phenomenon described in section A-1e.)

"AND" GATES

A-2a An AND gate is a logical circuit for the purpose of yielding a high output only if all of its input terms are high. Symbolically, an AND gate is illustrated as follows:

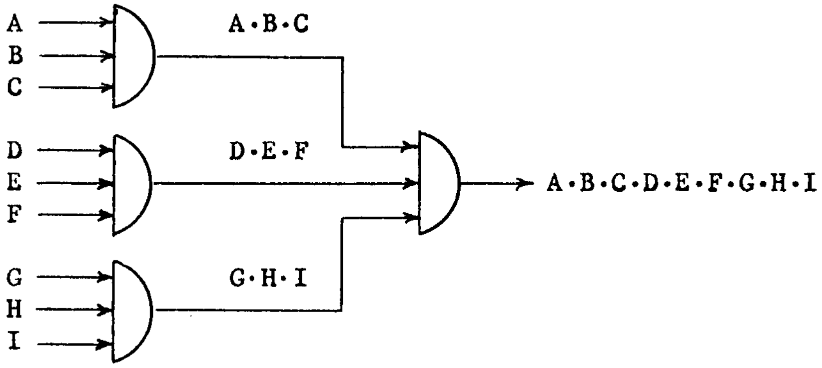


schematically:



A-2b The output is virtually short-circuited to the lowest input term. Therefore, only if all inputs are high (0V) will the output be high. The loading resistor is known as the PULL-UP resistor; its function is to "pull" the output potential "up", while the input terms pull it down.

A-2c As in the case of an OR gate, the input terms are isolated from one another by diode back resistance; also, a single AND gate with an excessive number of input terms will yield a significant back resistance loading problem. Splitting multi-term AND gates as shown below will relieve the back resistance problem (similar to the OR gate case) without altering the logic of the circuit:



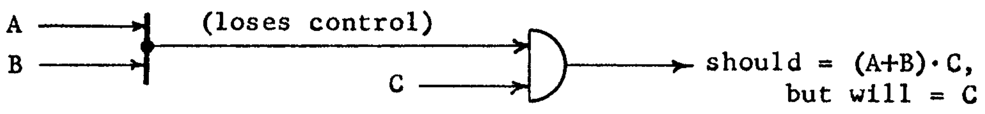
A-2d Dynamic properties: If an AND gate is fed by a square-wave, and the output is loaded by distributed capacitance to ground, the output will rise (from -20V to 0V) by virtue of the capacitance discharging through the PULL-UP resistor; therefore, the rise time of the LEADING EDGE of an AND gate's output is liable to be SLOW. The trailing edge (decline from 0V to -20V) will be rapid since the capacitance will charge through the forward resistance of the active diode. (In some cases, to reduce rise time, PULL-UP resistors have been shunted by "FREE RESISTORS", which are 110k resistors to +100V and are available in certain packages.)

AND GATES and OR GATES - COUPLING

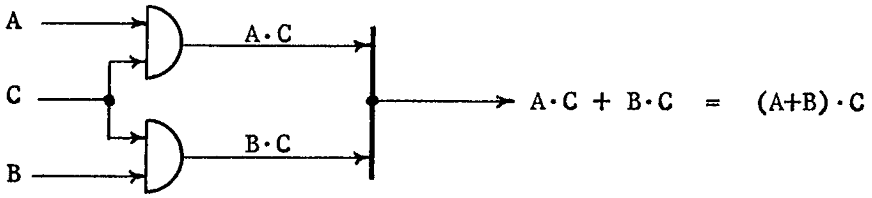
A-3a OR gates and AND gates may be connected to one another subject to the following major restriction: It is permissible for an AND gate to feed an OR gate directly; however, an OR gate may not feed an AND gate without an intervening stage of isolation. (A CATHODE-FOLLOWER or BUFFER-INVERTER can supply the necessary isolation.)

A-3b The reason for this restriction may be attributed to the fact that an OR gate (with or without PULL-DOWN resistor - ref. A-10a) is unable to carry enough current to drop 120V across the 110k PULL-UP resistor in the AND gate; consequently the OR gate cannot render the AND gate's output equal to -20V when the logic calls for such a case. Ohm's law will prove the point.

A-3c As an example, the circuit below should yield (A+B)·C, but will actually yield C since the (A+B) combination cannot disqualify the AND gate.

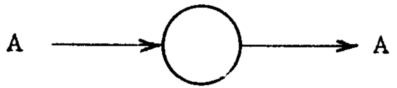


a satisfactory alternative circuit is:



CATHODE-FOLLOWERS

A-4a A CATHODE-FOLLOWER is symbolically noted as follows:



(Schematic on dwg. 13)

A-4b Cathode Followers serve no purpose as far as logic is concerned. They handle certain technicalities in the electronics. The proposition of an OR gate feeding an AND gate (above) is one example. They are installed whenever necessary for purposes such as the following:

1) Isolation (hi Z in, lo Z out).

2) Power boost
    a) Resistive loads
    b) Reactive loads (i.e. preservation of wave shape when distributed capacitance loading is heavy).

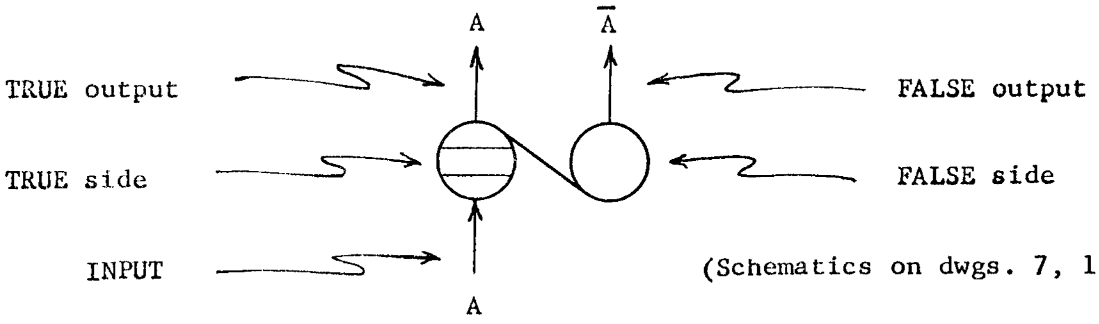
3) Addition of constant voltage to input.

A-4c The CATHODE-FOLLOWER circuits available in the packages provide loading flexibility in some cases. These cases provide optional amounts of cathode loading resistance within the CATHODE-FOLLOWER package itself, allowing a variety of loads. The grid circuits also provide a degree of flexibility in some cases.

Note that the grid return resistances in the packages involve voltage dividers. The reason for this is to render the grid potential -92V (instead of -160V), in the event of removal of the package supplying the input signal. This will prevent the cathode from approaching -160V which could result in (1) exceeding the filament-to-cathode voltage rating of the tube (filaments are returned to -55VDC), and (2) applying excessive inverse voltage to diodes controlled by the cathode-follower.

BUFFER-INVERTER

A-5a A BUFFER-INVERTER is symbolically noted as follows:



(Schematics on dwgs. 7, 13)

A-5b A BUFFER-INVERTER is a follower. Its true output "A" follows the input "A". The false output "$\overline{A}$" is the exact opposite of "A" (i.e. "$\overline{A}$" is "A" inverted, hence the term "inverter").

A-5c The outputs are clamped at -20V or 0V and are capable of feeding several loads. Furthermore, loading of the outputs does not affect the input (hence the term "buffer").

A-5d Refer to Drawing 7 (left), BUFFER-INVERTER schematic: The first inverter (V3A) receives the input signal "A" at pin 2. This signal should be at 0V, -20V, or in transistion - subject to integration. The plate output should yield a potential at the grid of the next inverter (V2A) such that it will either be cut off or fully conducting. C5 and C7 both contribute to high frequency peaking to compensate for possible integration suffered by the incoming signal (V3A, pin 2) due to distributed capacitance. This peaking results in rapid transit time in the output current of V2A (and V3B), effectively "cleaning up" the leading and trailing edges of the incoming signal, hence synthesizing its ideal shape.

A-5e The V2A and V3B plate circuits are completed by components located in DIODE CLAMP package. A schematic of such a package is shown on

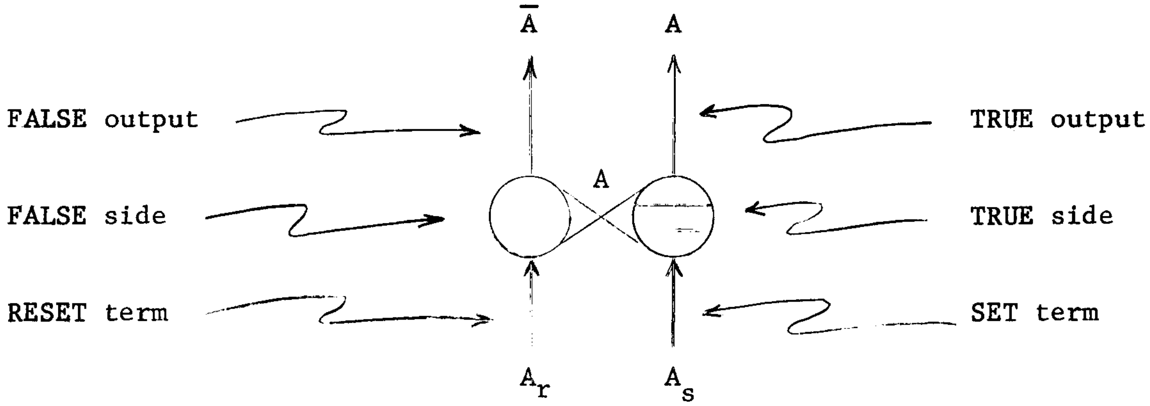
Drawing 12. This packaging system keeps the diodes physically separated from the heat-producing components in the BUFFER-INVERTER package.

A-5f When V2A conducts, its plate will be low consequently cutting off V3B; conversely, if V2A is cut off, its plate will be high causing V3B to conduct. Output pin D will yield the TRUE output "A" - pin C the FALSE output "A". Normally either V2A or V3B (but not both) will conduct providing a potential of approximately -121V to their common cathode connection; C2 holds this potential during transitions.

A-5g The DIODE CLAMP circuits terminating the V2A and V3B plate circuits assure that output pins D and C will be clamped either at -20V or 0V. Loading of the outputs should only serve to add to or subtract from the clamping current. Overloading of these outputs can prevent clamping current, resulting in instability. Low emission triodes can also result in inadequate current for loading and/or clamping.

FLIP-FLOP

A-6a A FLIP-FLOP is symbolically noted as follows:



(Schematics on dwgs. 7, 13)

A-6b A FLIP-FLOP is an ELECTRONIC SWITCH consisting of two D.C. inverters and a trigger circuit. It has two stable states known as SET and RESET. SET is the state in which the TRUE OUTPUT (striped side of symbol) is high (0V) while the FALSE OUTPUT is low (-20V). RESET is the state in which the FALSE OUTPUT is high (0V) and the TRUE OUTPUT is low (-20V). The SET STATE results from the application of a SET TERM, while the RESET STATE results from the application of a RESET TERM. The FLIP-FLOP once rendered in one of its two stable states (SET or RESET) will <u>remain</u> in that state until caused to change by an input term calling for a change in state.

A-6c Drawing 7 (right) shows a schematic of a complete FLIP-FLOP circuit. It can be seen that, with the exception of the NEON SERIES RESISTOR, the two inverters are drawn as mirror-images of each other and that each one feeds the other.

A-6d Normally, one tube will be conducting, thereby holding the other cut off. If V1A is conducting, it will hold V1B cut off maintaining the SET state of the FLIP-FLOP. V1A, by conducting, will render the FALSE output (pin T) low (-20V), while V1B, by not conducting, will allow the TRUE OUTPUT (pin S) to be high (0V). If the above state were reversed, the FLIP-FLOP would be in the RESET state.

A-6e To bring about a change in state, the conducting tube will be driven into cut-off by a negative trigger signal. This will cause a rise in its plate voltage which will turn the non-conducting tube on; this, in turn, will hold the previously conducting tube cut off. This establishes the new stable state in which the FLIP-FLOP will remain until another trigger signal, applied to the opposite side, causes it to change.

A-6f The trigger circuit consists of two identical gates: one for SET and the other for RESET. CLOCK is applied to both, CLOCK consisting of negative pulses of short duration (.3 - .5 microseconds) appearing at 9.3 microsecond intervals. The CLOCK line is normally at 0V, but reaches -13V during a CLOCK pulse. CLOCK is the synchronizing signal that causes the FLIP-FLOP to be SET or RESET depending upon logical presence or absence of the SET TERM or RESET TERM.

A-6g Consider now the RESET circuit. If the RESET TERM is logically absent (at -20V), CLOCK is decoupled from C3 by virtue of the back resistance of CR1, which will be "biased off". In consequence no negative pip should be coupled through C3 to the grid of V1A. On the other hand, if the RESET TERM were to be logically present (at 0V) at CLOCK pulse time, electrons would be transmitted through CR1's forward resistance into the bottom plate of C3 and to R5, which acts as a load resistance. Discharge of electrons from the top plate of C3 causes a negative-going "reset pulse" at the grid of V1A; this will cut V1A off.

A-6h Regenerative action takes over as V1A's current drops: V1A's plate voltage rises, turning on V1B. V1B's plate voltage drops, cutting off V1A, which is the triode which the "reset pulse" was cutting off in the first place. C1 and C2 accelerate the transition. The FLIP-FLOP will remain in this new state until V1B is cut off by a "set pulse".

A-6i Whenever a FLIP-FLOP experiences a change in state, the charges on C1, C2, C3, and C4 will change. Until these charges are almost stabilized, the FLIP-FLOP will not be receptive to further trigger pulses were they to occur in rapid succession. Ample time is available for this stabilization since CLOCK pulses, available for trigger, occur at 9.3 microsecond intervals (i.e. rep. rate = 108 kc.)

A-6j Drawing 7 indicates by waveform that when a CLOCK pulse is concurrent with the leading edge of the RESET TERM, the diode (CR1) will remain "biased-off". Even if the RESET TERM has a steep leading edge this will hold true. The potential at the top of the diode is the controlling potential. This potential will not rise instantly when a square-wave RESET TERM appears since C3 requires time to charge, with R5 (33k) limiting charge current. R5 and C3 then, constitute an integrating circuit in which high frequency components are dropped across R5. Hence, when CLOCK and the leading edge of a RESET TERM are concurrent, CR1 will remain "biased-off" during the first CLOCK pulse and the "reset pulse" will not appear until the next CLOCK pulse.

A-6k Should the trailing edge of a RESET TERM and CLOCK be concurrent, the same reasoning holds true. As the RESET TERM drops, C3 will maintain a qualifying potential at the top of CR1 sufficiently long to permit CLOCK to be transmitted through the diode.

A-6l The RESET TERM itself does not appear to any significant extent at the grid of V1A. The high frequency components of the RESET TERM signal are dropped across R5, while the low frequency components are dropped across C3. If V1A and V1B were removed from the circuit and CLOCK were to be decoupled, the RESET TERM would appear at V1A-pin 2 as a small positive-going signal at leading-edge time and a small negative-going signal at trailing edge time. Neither of these are of any consequence unless marginal conditions exist in the circuit when operating with a weak tube. In such cases, the only malfunction would be a function of the leading-edge of a RESET TERM applied the FLIP-FLOP when it is already in the RESET state. The positive-going signal remnant at V1A-pin 2 could cause V1A to conduct; this could result in SETTING the FLIP-FLOP. This would only occur when V1B is weak and is unable to hold V1A cut off with an adequate safety margin.

A-6m Obviously the analysis of the RESET circuit applies also to the SET circuit since they are identical.

A-6n The example in the lower right section of Drawing 7 indicates FLIP-FLOP reaction to SET and RESET terms.

A-6o FLIP-FLOP SUMMARY: A FLIP-FLOP is an electronic switch which may be SET or RESET by means of CLOCK, which can be gated by the SET or RESET TERMS. Transition can take place only at CLOCK time. If a CLOCK pulse occurs at the instant a SET or RESET TERM begins to rise, it will be the following CLOCK pulse that causes transition. Also, a CLOCK pulse coincident with the beginning of the decline of a SET or RESET TERM will still consider that term high. If the SET TERM occurs during one pulse period, the TRUE OUTPUT of the FLIP-FLOP will not be high until the next pulse period. Similarly, if the RESET TERM occurs during one pulse period the FALSE OUTPUT of the FLIP-FLOP will not be high until the next pulse period.

MEMORY LINES (Ref. Drawing 9)

A-7a The recirculating memory line is the storage device used in the G-15D memory. It consists essentially of a writing station, a time delay, a reading station, and a means of regeneration of information (subject to external control).

A-7b Normal operation of a memory line is recirculation (i.e., information, once written in the line, will remain in the line unchanged and be revealed at the reading station periodically.) Drawing 9 is the schematic of MEMORY LINE #2 which will be used as an example. The line is shown symbolically in the lower left-hand corner in the form it would be found on the "D-SIZED PRINTS".

A-7c The object of this discussion is to trace the writing of one bit of information through a recirculation cycle.

A-7d To begin, to write a ONE, a 2 microsecond WRITE PULSE is coupled to the writing pentode's control grid. This will cause flux in the write head (upper right) and will consequently influence the magnetic drum surface passing under its gap at the time. This magnetic surface approaching the write head is erased by a permanent magnet mounted on the drum shroud. The erasure represents ZERO; writing a ONE on the erased surface causes a distortion of the regular flux pattern of the surface. (Writing a ZERO involves no writing at all, hence no flux distortion.)

A-7e The recorded element is carried by the drum surface past a reading head after a delay determined by the peripheral speed of the drum and the spacing between the writing and reading heads. When the flux irregularity (resulting from writing the ONE) passes under the gap of the reading head, the reading head flux, normally constant, reverses and then returns to normal. This flux change induces an EMF resembling a sine wave in the reading head coil.

A-7f One end of the read head coil is grounded such that the floating end yields a sine wave, the trailing peak of which is positive. Resistance loading of the coil is accomplished in the PREAMPLIFIER CHASSIS and may be varied from 2.2k to 12.2k by a screwdriver adjustment. This is adjusted to minimize ring effect and to shunt the signal to obtain a normal level (500 mv. approx.). This is a factory adjustment and should not require attention unless the associated head is replaced.

A-7g At this point, the signal requires amplification, a matter which is accomplished in a conventional plate-loaded, RC-coupled amplifier employing low loading resistance for good high frequency response. The output is cathode-follower driven out of the PREAMPLIFIER CHASSIS into a READ AMPLIFIER package where monitoring of the signal takes place.

A-7h The first step in the READ AMPLIFIER is to amplify, rectify, then amplify the incoming sine wave to produce a half sine wave of sizable swing for each detected ONE.

A-7i The first operation in amplification is to terminate the cathode follower with a step up (1:4) transformer. (The .27 mfd and 120 ohm combination in the primary circuit is to prevent peak clipping without introducing degeneration and can be considered a biasing requirement.)

A-7j The secondary of the step-up transformer constitutes the input to a "bootstrap" amplifier, which in this case is an over-biased cathode-loaded amplifier. The purpose of the amplifier is to amplify the positive portion of the input wave, without phase inversion. Response is controlled by returning the transformer secondary to a potentiometer in the cathode circuit. This adjustment controls: (1) the amount of degeneration, hence gain, and (2) the static bias on the stage, hence sampling level. It is normally adjusted to yield signals reaching the -50V level at test point K. This potentiometer may occasionally require adjustment to compensate for changing parameters elsewhere in the read-write circuit.

A-7k At this point, the half sine waves are probed by READ CLOCK which is applied to the cathode of a flip-flop trigger tube. In the event of coincidence between READ CLOCK and a ONE waveform, the trigger triode will conduct, setting the READING FLIP-FLOP to ONE. When the trigger triode conducts, grid current is inevitable; this is limited by a 2.2k grid resistor. The 15 mmf. grid-to-ground capacitance counteracts the degenerative effect on the positive going grid signal by the negative going cathode and plate signals. READ CLOCK is obliged to supply grid and plate current to all trigger tubes. This accounts for relatively high peak power requirements of the READ CLOCK pulse driver (Ref. B-3g). Since this grid current load will only present itself when a line yields a ONE, the total load will be a function of the memory contents.

A-7l Approximately 8.3 microseconds after the ONE bit has been stored in the READING FLIP-FLOP, CLOCK unconditionally resets it to ZERO. The flip-flop's ONE output is coupled via gates in the DIODE 3 (D3) package to the WRITE AMP package if the line is recirculating. (Heavy lines in the DIODE 3 package show recirculation path.)

A-7m The first item in the WRITE AMP is a cathode-follower which permits the output of the OR gate in the DIODE 3 package to feed the AND gate feeding a power pentode (Ref. A-3, A-4).

A-7n For the last two microseconds prior to resetting the READING FLIP-FLOP to ZERO, the AND gate in the WRITE AMPLIFIER was qualified by WRITE PULSE. This causes the writing pentode to conduct for two microseconds through the write head, rewriting the original ONE. Had the read head "detected" a ZERO (absence of a ONE), no writing would have taken place, effectively recirculating the ZERO.

A-7o Needless to say, prior to the leading edge of the WRITE PULSE, the ONE output of the READING FLIP-FLOP should have risen to 0V. This allows 6.3 microseconds for rise time. (This 6.3 microsecond rise time requirement factor applies to most signals in the computer and accounts for many CATHODE-FOLLOWERS and resistance-loading of certain circuits - such as AND gates. Decay time is equally important but usually not as critical as rise time.)

A-7p It can be seen that the READING FLIP-FLOP activity depends upon CLOCK for reset and READ CLOCK for set. These pulses synchronize all memory lines with a standard timing reference. WRITE PULSE synchronizes the writing. These pulses are shown on the top of Drawing 6 in approximate terms; their formation is described in Sec. B-3.

A-7q The spacing between read and write heads is governed by the capacity of the particular memory line. In the case of a long memory line, the delay in the line is such that from the time a ONE is written until the time it is rewritten, 3132 (i.e., 108 x 29) pulse periods will elapse. This allows 3132 different bits to be read and rewritten within a recirculation cycle.

A-7r The short lines have shorter delays as follows: 116 pulse periods, 58 pulse periods, and 29 pulse periods. The spacing from read head to write head is known as the TANGENTIAL adjustment. It is made at the factory and should not require any further adjustment. As long as READ CLOCK probes the reading wave at its peak (test pt. K), the adjustment is satisfactory. Misadjustment would be revealed in misphasing of these two signals. CUSTOMER ENGINEERING should be consulted for adjustment details. It is unwise to attempt head adjustment without being well informed as to procedure. Accidental damage to a track could require replacement of the drum.

A-7s Another adjustment of the heads is RADIAL adjustment. This should render head (gap) to drum surface spacing equal to 1 mil. (for both read and write heads.) Proper spacing is essential for good resolution and signal-to-noise ratio. This too is a factory adjustment. Only in the case of subnormal reading waves (not attributable to failing electronic components) should RADIAL adjustment be considered. As in the case of TANGENTIAL adjustment, CUSTOMER ENGINEERING should be consulted.

A-7t Noise mentioned above is insignificant compared to the amplitude of a legitimate ONE being read since it is normally well below the sampling level in the READING FLIP-FLOP trigger stage. The worst noise element will result from crosstalk (magnetic coupling) between the write and read heads of a line. This interference is at its worst in the short (29 bit) memory lines.

A-7u Another factor which may cause deviation from optimal memory line functioning is the result of head misadjustment due to thermal effects. Therefore, if the drum is cold, a line may operate with reduced safety margins. Only a line already in need of maintenance would fail due to this effect. If any memory line adjustments are to be made, it should be done when the drum has reached its normal operating temperature.

MEMORY LINES: READ-OUT, READ-IN FUNCTIONS

A-7v READ-OUT: When information is to be read out of a line, the READ FLIP-FLOP output is coupled to an external circuit by an AND gate qualified by the desired terms. In the case of MEMORY LINE 2 (Drawing 9, lower left), M2 reaches EB if qualifying terms SW and SO are both high. Read-out does not disturb the contents of the source line.

A-7w READ-IN: When information is to be read into a line from an external source, two operations are necessary: (1) allow the new information to reach the writing circuit, and (2) simultaneously block the recirculation path of the old information.

A-7x Item (1) is handled by qualifying an AND gate to which the new information is applied. In LINE 2 (Drawing 9) terms DO and DW permit LB to be written. Item (2) is handled by blocking the gates which allow the READ FLIP-FLOP output to reach the writing station. If LINE 2 is selected as destination, both $\overline{DO}$ and $\overline{TR \cdot DW}$ will be low at the appropriate time.

A-7y Some special purpose memory lines may deviate from this pattern and will be discussed later. Needless to say, all READ-IN - READ-OUT activities are appropriately synchronized by control circuits.

THE MEMORY

A-8a The DRUM MEMORY is composed of many recirculating memory lines such as the one just described. These lines can differ from one another as follows:

1) Capacity
2) Writing control
    a) Recirculation gating
    b) Method of writing new information

A-8b The MEMORY consists of:

21 long lines - 3132 bits (108 words) - Lines 00-19, and CN
5 short lines - 116 bits (4 words) - Lines 20-23, and MZ
3 short lines - 58 bits (2 words) - ID, MQ, PN
2 short lines - 29 bits (1 word) - AR, CM

A-8c Three of the above are not directly available to the programmer since they are for the benefit of internal computer functions. These are CN, MZ and CM. In addition to the recirculating lines mentioned above there are three permanently recorded (non-recirculating) lines known as CLOCK TRACK SPARE CLOCK TRACK, and TIMING TRACK (TM). These are for timing purposes and are discussed in Sections B-3a and B-5a.

A-8d Physically, the short memory lines are sandwiched in between the read heads and erase magnet of the long lines as illustrated on Drawing 8.

A-8e Memory line specifications:

pulse period = 9.3 microseconds
packing density = 90 bits/inch
read-record mode - RETURN TO ZERO
maximum access time = 28.5 milliseconds

PHYSICAL LOCATION OF LOGICAL CIRCUITS

A-9a The fundamental circuits mentioned in the preceding sections (with the exception of READ PREAMPS) are physically located in standard packages distributed about the logic panels of the computer and are interconnected by appropriate inter-package wiring. The package schematics may be found on Drawings 11, 12 and 13. Drawing 10 provides an index of information pertaining to all packages.

A-9b The detailed logical block diagrams ("D-SIZED PRINTS") provide information relating to package locations and package jack pin-connections. Drawing 9 (MEMORY LINE 2) provides an example of a detailed logical block (lower left) and the schematic components and packages it represents. Package locations are designated by coordinates, a letter and a number, which are printed on the jack side of the logic panels themselves.

A-9c Common sense should render the notations self-explanatory with the exception perhaps of CLAMP PACKAGE locations. CLAMP PACKAGES are not shown on any block diagrams, but a notation external to the associated FLIP-FLOP or BUFFER-INVERTER supplies the location information. (On Drawing 9, below lower left FLIP-FLOP "M2", see notation "D E22 C". This states that the CLAMP PACKAGE is located in package jack with coordinates E-22 and that pin connections D and C are used.)

A-9d A few self-imposed exercises requiring translation of information contained in the detailed block diagrams to schematic form should reveal the scheme to the reader.

A-9e Technical details of circuits not included in standard packages will be discussed as they arise.

A-10 MISCELLANEOUS

a) PULL-DOWN resistors associated with OR gates are physically located in the package containing the load presented to the OR gate (e.g. Drawing - 9 - input to WRITE AMP).

b) PULL-UP resistors associated with AND gates are located (1) within the package where the AND gate diodes are, or (2) another package, or (3) in more than one package (when paralleled). Reducing PULL-UP resistance by parallel combinations can be for the purpose of compensating for low PULL-DOWN resistance in a network of gates and/or to reduce rise time of a signal.

c) The diodes associated with a single gate are not necessarily all located in the same package. Pre-wired combinations within D1 and D2 packages provide a variety of options minimizing wiring external to the package.

d) The secondary of the 6.3V filament transformer which feeds all filaments is returned to -55V to minimize possibility of exceeding the heater-to-cathode voltage ratings of all tubes.

e) Utilization of a right-to-left time axis is used as a convenience in analyzing most circuit activity (ref. G-10b).

SECTION B

BASIC TIMING

This section is devoted to the basic timing subdivisions and associated signals involved in the G-15D. The reader is urged to memorize the nature of the timing structure and signals before proceeding to sections to follow since Boolean algebra notations define times merely in terms of signals. It is not necessary to digest all of the details of the electronic circuits which give rise to the various timing signals before reading the sections to follow.

G-15D IN GENERAL

B-1a The G-15D is composed of a combination of logical "building blocks" discussed in Section A. The heart of the computer may be considered the magnetic drum which not only constitutes the MEMORY, but also the source of all timing signals.

B-1b All computer activities are synchronized with the basic timing signals mentioned above in a consistent orderly manner. Since such timing signals control logical activity, the time axis may be considered a standard reference in describing an event, for this reason timing warrants discussion prior to any other functions.

TIMING SUBDIVISIONS

B-2a (Ref. Drawing 6) In general, time in the computer is cyclic as it is on a clock. The basic cycle is known as a DRUM CYCLE (sometimes called a LOGICAL DRUM REVOLUTION), during which the entire contents of the memory are revealed and can be subjected to alteration. A DRUM CYCLE is the recirculation time of a long (3132 bit) memory line and is arbitrarily divided into 108 WORD TIMES (WT) (as a day, which is a cycle, is divided into 24 hours.) These WORD TIMES are numbered 00 - 107.

B-2b Each WORD TIME is divided into 29 PULSE PERIODS (PP) designated T1 - T29.

B-2c Associated with each PULSE PERIOD is a trio of pulses, the most significant one of which is known as CLOCK. CLOCK pulses occur at the junction of two adjacent PULSE PERIODS. The leading edges of these CLOCK pulses cause the transitions in most flip-flops. A CLOCK pulse, the duration of which is logically insignificant (.3 - .5 microseconds), may be considered as designating either the beginning of one PULSE PERIOD or the end of the preceding one. The remaining two pulses of the trio are READ CLOCK and WRITE PULSE, and are necessary for the operation of memory lines. (Their use is restricted to internal functions of the memory lines only, hence they need not be considered as constituting significant general purpose logic pulses.)

B-2d Drawing 6 illustrates the sequence of the above mentioned elements of time. Below is a convenient analogy between the G-15D computer time reference and the familiar times of day:

1 DRUM CYCLE	-----1 day
1 WORD TIME	------1 hour
1 PULSE PERIOD	-------1 minute

B-2e Just as events that occur during any day may be described in terms of hours and minutes, a computer event may be designated by word time and pulse period (e.g.,T29 of Word 107 is the last PULSE PERIOD of a DRUM CYCLE). Also, just as a duration of activity may be described as lasting for N hours, a computer activity may be said to last for N WORD TIMES.

B-2f Unless the computer is caused to alter its internally stored information, any subdivision of information will be available every DRUM CYCLE at the same time in terms of WORD TIME(s) and PULSE PERIOD(s).

B-2g The basic element of information circulating in the computer is the BINARY DIGIT (abbrev: BIT). Timewise, a particular bit of information may be located by designating its PULSE PERIOD and WORD TIME.

B-2h The basic information group consists of 29 bits and will "occupy" one WORD TIME (1 WT = 29 PP). Such a group is known as a WORD and may represent anything the programmer may designate (i. e., an instruction, a number and sign, part of a number, a control code, etc.). It is up to the programmer to determine the information content of the WORDS and their disposition. The computer itself will only do what it is instructed to do.

B-2i In order to logically and electronically identify certain times, it is necessary to have available certain signals which will occur periodically at the designated times. For this purpose three tracks (plus a spare) are available on the drum. These tracks, in conjunction with circuits known as CLOCK CHASSIS, TIMING GATES and CONTROL GATES, yield the necessary signals. Drawing 15 indicates the system.

WRITE PULSE, CLOCK, READ CLOCK - UNCONDITIONAL

B-3a CLOCK TRACK: This trio of signals occurs unconditionally every pulse period.Their origin is the CLOCK TRACK (see Drawing 15 - lower left). This track is permanently recorded around the drum (i.e., it has only a reading head and hence does not recirculate). The reading wave from the head resembles a continuous sequence of sine waves. The manner in which this track is recorded is such that exactly 3596 (i.e., 124 x 29) pulses are recorded around the track in a closed circle. This recording procedure is performed at the factory and would constitute a difficult problem to re-record in the field should an accidental erasure occur. (A grid to plate short in the CLOCK TRACK preamplifier tube could cause track erasure by DC current in the read head.) For this reason a spare recorded CLOCK TRACK is provided. Should the active CLOCK TRACK become erased, the spare may be used until the normally active track is re-recorded. In the unlikely event that re-recording of an erased CLOCK TRACK is necessary, instructions for doing so in the field can be obtained from CUSTOMER ENGINEERING.

B-3b CLOCK CHASSIS: The CLOCK TRACK reading head output is amplified by a pre-amplifier circuit identical to those used with other heads (Drawing 11). The preamplifier output is connected to the input of the CLOCK CHASSIS, which is located in the bottom of the computer (front center). The CLOCK CHASSIS (Drawings 14, 3D293) forms four different output pulses, three of which constitute the trio mentioned above.

B-3c WRITE PULSE: The preamplifier output (a series of sine waves) is "squared" by V1 and V2 in the CLOCK CHASSIS (Dwg. 14). The V2B output, differentiated, triggers multivibrator V3, which yields a 2 microsecond positive-going square wave at V3, pin 1. This 2 microsecond square wave causes power pentode V7 to conduct through its plate transformer T3. The negative end of T3's secondary (term. 4) is returned to -20V; the positive end (WRITE PULSE) is appropriately terminated to -20V and clamped at 0V. Secondary termination is accomplished by (1) a 680 ohm resistor ~~(R20) (2)~~ (R29) (2) the load, and (3) two CLOCK CLAMP PACKAGES - one in each logic panel (see also dwg. 12). (Termination in the logic panels reduces transient problems.)

B-3d CLOCK: The trailing edge of the V3 multivibrator output (pin 6) causes blocking oscillator V4 to cycle yielding a positive-going pulse of .3-.5 microsecond duration at T6, term. 5. This signal, which exists directly after the decline of the WRITE PULSE, causes power pentode V5 to conduct through plate transformer T1. The positive end of the secondary (term .3) is returned to ground; the negative end (CLOCK) is appropriately terminated to ground and clamped at -13V. Secondary termination, as in the case of WRITE PULSE is accomplished (1) in the CLOCK CHASSIS (a 100 ohm res-R28, and CR3), (2) by the load, and (3) in the CLAMP package.

B-3e READ CLOCK: These pulses, used in the READ AMPLIFIER circuits to probe for the presence of ONES, are required to follow CLOCK pulses (unconditionally) by approximately 1 microsecond. They resemble CLOCK in shape, but have a base line of approximately -25V and reach a negative peak of -75V (clamping level). These two levels are both adjustable and may be varied for optimal results.

B-3f To produce READ CLOCK, CLOCK is coupled to the grids of V8 and V9 (power pentodes) via T4 (for inversion and -20V return) and via a 1 microsecond delay line. The result is that the power pentodes conduct through the plate transformer T5 for .3-.5 microsecond at the appropriate time.

B-3g Due to the nature of the load (ref. Section A-7k) and the amplitude of the READ CLOCK pulse itself, four pentode drivers are required to supply the necessary power output. V8 and V9, in the CLOCK CHASSIS itself, are supplemented by two more power pentodes in the READ CLOCK package (the only one of its kind in the computer - location: J-54). The READ CLOCK package contains two power pentodes in parallel feeding one plate transformer. The pentode grids receive the same signal as those in the CLOCK CHASSIS (TS2-9); the transformer secondary is wired in parallel with the READ CLOCK output of the CLOCK CHASSIS (i.e., the T5 secondary).

B-3h The transformers' secondary termination is accomplished in the same general manner as termination of the other signals; however, -25V and -75V are required for reference level and clamping level. V10 and V11 supply these voltages as follows:

B-3i The cathode of V11 yields a potential which is primarily a function of the setting of potentiometer R54. This cathode potential is adjusted to approximately -75V (by R54) and should not vary significantly as a result of loading. V10's function is similar to that of V11 except that V10's cathode will be primarily a function of the setting of potentiometer R51. R51 is set to yield approximately -25V from V10's cathode.

B-3j The reader will note that the -75V output is coupled to the V10 grid circuit and that an inter-action will exist. Furthermore, neon NE2-1 couples the entire amount of any V11 cathode voltage fluctuation to V10's grid, hence will tend to vary the -25V output level. This interaction tends to neutralize the effects of variations in clamping current required by READ CLOCK. (The amount of clamping current is a function of the total number of ONES in the memory.) In adjusting R51 and R54, a "rocking-in" procedure should be followed to allow for this inter-action. Although the two output potentials are called "-25V" and "-75", they are, in practice, adjusted to any levels in the vicinity which yield the most stable reading amplifier behavior.

B-3k A summary of these three pulses may be seen at the top of Drawing 6.

SHIFT PULSE - CONDITIONAL

B-4 (This signal is not among the basic pulses appropriate to mention at this point; however, its formation may as well be discussed while CLOCK CHASSIS is being described.) T6, term.5, which yields CLOCK, also feeds the grid circuit of power pentode V6. However, if the SHIFT COMMAND INPUT (= RC·CJ), which is applied to CR2, is at -20V (one stable state), the grid will not be able to rise above -20V due to clamping by CR2 - hence no V6 output. If the CR2 cathode is at 0V (rather than -20V) V6 will conduct and the T2 secondary will yield a signal of the same type as CLOCK. Clamping follows the same pattern as that for CLOCK except that termination only exists in one of the two logic panels since the entire load is located in that panel only. In general, SHIFT PULSE constitutes a burst of CLOCK pulses dependent upon an externally generated signal = RC·CJ. (Sec. C-5b.)

TIMING PULSES - THE TIMING TRACK (TM)

B-5a T1, T2, T13, T21, T28 and T29: These pulses are required to identify their respective pulse periods every word time. The TIMING TRACK (TM), a permanently recorded track, supplies the necessary information to signify these pulses. The TIMING TRACK, like the CLOCK TRACK, is recorded at the factory. It repeats the same digital configuration 124 times around the periphery of the drum in a closed loop. (It is not necessary for this track to recirculate to stay in step with a DRUM CYCLE since the digital configuration in all WORD TIMES is identical and the only requirement is that an integral number of word times be recorded around the drum.)

B-5b The subdivision of each WORD TIME is illustrated on Drawing 6 (see TIMING TRACK.) The hardware is indicated on Drawing 15. The output of the TIMING TRACK READING FLIP-FLOP (TM) feeds an array of flip-flops and gates in the TIMING GATES. The key outputs from the circuit are high during T1, T2, T13, T21, T28 and T29. Generation of these signals from TM is illustrated on the timing chart on Drawing 15 - lower left. The circuit is self-synchronizing.

B-5c It is not necessary to have a spare TIMING TRACK as was the case with the CLOCK TRACK. A new TIMING TRACK may be recorded in the event of accidental erasure ~~by using the CLOCK TRACK and the PACKAGE TESTER unit.~~ If the case arises, the procedure can be obtained from CUSTOMER ENGINEERING.

WORD TIME INFORMATION - THE NUMBER TRACK (CN)

B-6a The NUMBER TRACK is the word time reference track and supplies the computer with several pieces of information. Drawing 6 (right) illustrates the contents of all words. The purpose of all bits of information will be discussed in this manual as the need for them arises. At this point only one bit need be mentioned: the bit stored at T29 time during each word time. This bit is a ONE during all word times other than WT 107, but during WT 107 itself the bit is a ZERO. The latter may be defined in Boolean algebra terminology as T29·CN, where CN is the READING FLIP-FLOP of the NUMBER TRACK.

This particular signal comes high during the last PULSE PERIOD of a DRUM CYCLE and constitutes an index or ORIGIN PULSE. The signal is called TO (i.e., $TO = T29 \cdot \overline{CN}$), and is used for many purposes. Associated hardware may be found on Drawing 15.

B-6b Needless to say, since an actual physical drum revolution and a DRUM CYCLE differ (by a factor = 124/108), it is necessary that the NUMBER TRACK be a recirculating memory line so its contents will "keep step" with DRUM CYCLES. Since power turn-off involves erasure of all recirculating memory lines, a scheme of renewing the NUMBER TRACK during the power turn-on cycle is provided. This is discussed in Section G.

B-6c Once TO is established, a circuit in the CONTROL GATES (Drawing 15) involving the CE and CF flip-flops yields more timing signals. The CE flip-flop (synchronized by the NUMBER TRACK) yields an output "CE" which is high during EVEN word times only. (Obviously "$\overline{CE}$" will be high during ODD word times.) CF will, under control of CE, etc., be high during word times congruent to 2 and 3 modulo 4.

B-6d CE and CF, once synchronized, will allow the formation of certain other basic timing pulses in the TIMING GATES as follows:

$TE = T1 \cdot CE$ (i.e., T1 of EVEN word times)
$TF = T29 \cdot \overline{CE} \cdot CF$ (i.e., T29 of words congruent to 3 mod. 4)

B-6e The reader will note that the signal TE, which has been defined as $T1 \cdot CE$ is actually formed by $T29 \cdot \overline{CE}$ delayed one pulse period. Frequently the means of forming a signal is not the most straight-forward one. This can usually be attributed to conservation of hardware or preservation of waveshape. Ordinarily a signal is defined by Boolean algebra notation in terms of the conditions under which it occurs -- such notation usually follows the method whereby the signal is formed, but not necessarily.

B-6f Drawings 15 (upper left) and 6 (left) illustrate the signals just encountered. The reasons for them will become apparent later. At this point the reader should attempt to memorize the contents of Drawing 6 with the exception of details of the NUMBER TRACK not discussed in this section. These basic timing signals represent the time references for most computer functions to be discussed in sections to follow.

SECTION C

GENERAL COMPUTER ACTIVITY

This section is devoted to a variety of concepts and circuits. The circuits covered are controlled to some extent by the SPECIAL COMMANDS and other functions to be covered in sections to follow. The sequence of presentation in this particular section is less orderly than that to be found in others. This is necessary to present pre-requisite material first and to minimize forward references.

COMPUTER SEQUENCE OF ACTIVITY

C-1a Unless the computer is idle, it is engaged in a computing cycle illustrated on Drawing 18. The productive portion of the cycle takes place during the time the computer is in the TRANSFER (TR) state. It is during this time (an integral number of WORD TIMES) that an operation is executed. The TRANSFER state is sometimes referred to as the EXECUTE state.

C-1b Needless to say, the computer must know the nature of the operation to be executed; this is determined during the READ COMMAND (RC) state. During this state (lasting one WORD TIME), a command is "read" from a predetermined word location of a pre-determined line (ref. Sec. D-6b). The instant the final bit of the command (T29·RC) has been read, the command has been decoded and has set up all the necessary electronic paths for proper execution of the operation designated by the command.

C-1c Once a command has been read (and decoded) it may be executed immediately provided the command itself calls for immediate execution. If the command is not an IMMEDIATE command it is DEFERRED. As Drawing 18 illustrates, if a command is IMMEDIATE , as soon as the command is read, the TRANSFER state is initiated. If DEFERRED, the computer will rest in the WAIT TO TRANSFER (WTR) state for an integral number of word times until information in the command itself calls for the TRANSFER state.

C-1d How long the computer will remain in the TRANSFER state is also a function of the command.

C-1e Once the TRANSFER state is terminated, the computer will advance to the READ COMMAND state immediately or after an integral number of word times in the WAIT TO READ COMMAND (WRC) state. At this point the cycle repeats unless the computer is purposely caused to stop; in this case it will idle in the WAIT TO READ COMMAND state indefinitely.

COMMANDS

C-2a A command, as mentioned above, controls the computer in regard to timing (i.e., advancement from state to state), and in regard to the nature of the operation to be performed during the designated time of TRANSFER. A command is considered subdivided into two general portions: the STATIC PORTION and the DYNAMIC PORTION. (These names not only describe their purposes, but also their treatment within the computer.) Breakdown of a command is illustrated on Drawing 5 (top.)

THE STATIC PORTION: 13 bits (T1 - T13)

C-2b SOURCE AND DESTINATION (S & D): This information is contained in 10 bits (T2 - T11) which can assume 1024 (i.e. 2^{10}) different configurations, hence there are 1024 different SOURCE - DESTINATION combinations possible. Individually the SOURCE and DESTINATION portions can express SOURCES and DESTINATIONS numbered 00 - 31 (i.e., 00000 - 11111 in binary). If the DESTINATION is specified 00 - 30, the command calls for a transfer of information from a SOURCE (00-31) to the designated destination. However, if DESTINATION is selected equal to 31, the SOURCE number (00 - 31) specifies a SPECIAL COMMAND, not necessarily involving transfer of information at all.

C-2c CHARACTERISTIC (CH): This information is contained in 2 bits (T12 and T13) and can assume 4 (i.e., 2^2) different configurations, designating four options in performing a command defined by S and D. The manner in which the CH code is interpreted (hence, its result), is a function of the particular S and D selected.

C-2d SINGLE OR DOUBLE PRECISION (S/D) bit: This bit (T1) is the only remaining bit of the STATIC PORTION of a command. Its functions depend to some extent upon the remainder of the command (including the DYNAMIC PORTION). It is primarily concerned with setting up logical circuits to comply with timing requirements of SINGLE and DOUBLE precision operations; it does, however, serve other purposes.

THE DYNAMIC PORTION: 16 bits (T14 - T29)

C-2e IMMEDIATE or DEFERRED (I/D) bit: This bit (T29) controls whether the TRANSFER state will be initiated directly after the command is read or wait (in the WAIT TO TRANSFER state) until some other factor calls for it. A "0" specifies IMMEDIATE: a "1", DEFERRED.

C-2f TIMING NUMBER (T): This information is contained in 7 bits (T22 - T28) and can express a number from 00 - 127. This is a controlling factor in either initiating or terminating TRANSFER. The manner in which it is interpreted depends upon other factors in the command.

C-2g NEXT COMMAND LOCATION (N): This information is contained in 7 bits (T14 - T20) and is used to express a number from 00 - 107. These numbers refer to the WORD TIME during which the command to follow is to be read after the current command has been concluded.

C-2h BREAK POINT (BP) bit: This bit (T21) provides a programmable method of interrupting operation of the computer after the command has been executed. The setting of the COMPUTE switch on the BP position will cause the computer to idle in the WAIT TO READ COMMAND state after the TRANSFER state has been terminated.

C-2i (LOCATION of command) (L): This is not actually written as part of the command but is a piece of information associated with it. L is the word time (00 - 107) during which the command is read and usually is N of the previous command.

COMMANDS-SUMMARY

C-2j Commands consist of several subdivisions, all of which contribute to define and control the operation to be performed. The programmer is required to account for all 29 bits of a command; the engineer should be able to determine exactly what will happen within the computer as the result of any command whether or not its composition is legitimate.

NUMBERS

C-3a Ordinarily, the words to which commands make reference contain numbers or portions of numbers. Any word (in the memory) to which a program never makes reference can contain anything--usually all ZEROS.

Numbers are of two general types: SINGLE PRECISION and DOUBLE PRECISION.

C-3b SINGLE PRECISION numbers are held entirely within a single word and consist of a total of 29 bits as follows: 28 (T2 - T29) to express the number and 1 bit (T1) to hold the sign (SIGN BIT = "0" means +; "1" means -). A single precision number can, by virtue of 28 bits, accommodate 2^{28} different binary configurations which amounts to precision up to one part in 268,435,455 (i.e. 1 part in $2^{28}-1$).

C-3c DOUBLE PRECISION numbers require two words and consist of an EVEN numbered word (time) for the lowest order portion and the following ODD numbered word for the highest order portion. Sign is held in the T1 position of the EVEN word (TE = T1·CE), and the remaining 57 bits are devoted to expressing the number. The numerical portion can assume 2^{57} different configurations amounting to precision of one part in 144,115,188, 075,855,871 (i.e. 1 part in $2^{57}-1$).

C-3d When an operation dealing with SINGLE PRECISION numbers is executed, T1 pulses constitute the TS or SIGN TIME pulse; DOUBLE PRECISION operations require TS to consist of TE (i.e., T1·CE). This is one function of the S/D precision bit of a command (ref. drawing 15-upper right).

C-3e Whenever a number is transferred from a SOURCE to a DESTINATION, and is subject to modification in the INVERTING GATES, the modification is a function of the SIGN associated with each individual number being transferred. Obviously pulses interrogating the signs of numbers must occur at the appropriate time. Proper programming of the S/D precision bit of a command therefore is essential.

COMPLEMENTATION OF NUMBERS

C-3f Numbers are normally to be found (in memory) in terms of ABSOLUTE VALUE and SIGN. Furthermore, the BINARY POINT may be assumed to be to the left of the highest order bit of each number, rendering the highest order bit in the 2^{-1} column. (A programmed scaling factor can render such a fractional number a multiplier for 2 raised to any power, hence, order of magnitude is unrestricted - this is the programmer's concern.)

C-3g Should a number be negative, it is desirable (in order to facilitate certain operations such as addition) to convert it to COMPLEMENT form, such that given a fractional number = .N, its COMPLEMENT is (1-.N). The COMPLEMENT represents a number, which if increased by a positive value =.N, will yield all ZEROS in its fractional part and an END CARRY into the imaginary 2^0 position. Such an END CARRY, if added to the imaginary "1" in the 2^0 position, would yield a sum bit of "0" and an end carry which will be killed.

C-3h Evidence of the imaginary "1" in the 2^0 position is the contents of the SIGN BIT. (i.e., a "1" in the sign bit represents a negative number; if the number is in complement form, the "1" (from "1-.N") is held in the SIGN BIT.) Ideally the SIGN BIT, which has a quasi-numerical significance, should appear in a bit location following the highest order numerical bit (2^{-1}) since it represents a state of 2^0. However, it is also vital that this sign bit precede the number (i.e., be at the lowest order end) to facilitate the activity in the INVERTING GATES which must know the sign of a number prior to its transmission from EB to IB (ref. Sec. C-7a).

C-3i The sign then, is applied to the lowest order end of a number for the sake of the INVERTING GATES, but may, when necessary, be influenced by an end carry from the 2^{-1} position in arithmetic operations as will be seen later in Sections C-10m-o.

C-3j To obtain the COMPLEMENT of a number the procedure is: Starting with the lowest order digit and proceeding up, pass all bits unchanged up to and including the first "1" bit; thereafter invert the bits to follow.

Example:

.N	.0110100
1-.N	.1001100

An analysis of the operation is as follows:

$1-2^{-n}$	.1111111
-.N	-.0110100
$1-2^{-n}-.N$	.1001011
$+2^{-n}$corr.	+.0000001
1-.N	.1001100

This may appear to be a round-about method of obtaining 1-.N, but it does not necessitate a subtractor.

C-3k The procedure of "PASS ALL BITS UNCHANGED UP TO AND INCLUDING THE FIRST "1" accomodates the subtraction of .N from all ONES and also the $+2^{-n}$ correction. "INVERSION FOLLOWING THE FIRST "1" handles the higher order portion of the subtraction from all ONES.

C-3l This scheme is know as the "2's complement system". (The "1's Complement System" does not accommodate the $+2^{-n}$ correction). When we say take the "1's complement of a number", this implies a binary point location, hence the value of the highest order numerical bit.

C-3m (The terms "'1's' complement system" and "1's complement of a number" do not necessarily mean the same thing. The G-15D obtains complements of numbers by employing the "2's complement system"; by placing the binary point to the left of the highest order bit a complement represents 1-.N hence is the "1's complement of a fractional number.") In an addition of two numbers of unlike sign, the positive number should be uncomplemented (i.e., NORMAL) and the negative number should be complemented. As a result of addition, the imaginary "1" in the 2^0 position will either remain, indicating a negative sum in COMPLEMENT form, or be changed to "0" indicating positive sum in NORMAL form. An end carry from the highest order numerical bit position (2^{-1}) will decide the fate of the imaginary "1" in 2^0 (ref. dwg. 25).

C-3n The end carry from 2^{-1} (T29 position of a word) will be added to the sign bit "2^0" (T1 position of a word) by virtue of the structure of the adders, which allow the sign position to be available for processing directly after the T29 position. Details of this will be explained under ADDERS (Sec. C-10m-o.)

C-3o Drawing 24 indicates the results of additions of two fractional numbers, a and b. Using the complementation scheme to deal with negative numbers, the chart reveals that all sums (unless they exceed a fractional value and constitute overflows) will be either in NORMAL or COMPLEMENT form and will contain the desired sign bit as CORRECTED SIGN. The results are a function of the signs and relative magnitudes of the AUGEND and ADDEND. Drawing 25 illustrates actual binary examples of the complementation and addition procedure (note that in MEMORY numbers are in terms of SIGN and ABSOLUTE VALUE: in the ADDER itself, NORMALS and COMPLEMENTS appear when appropriate).

SOURCES AND DESTINATIONS IN GENERAL

C-4a The simplest commands are those involving a transfer of information from a SOURCE (usually one memory line) to a DESTINATION (also usually one memory line). A list of SOURCES and DESTINATIONS is provided on Drawing 2. Unless DESTINATION = 31 is selected, the information content of the selected SOURCE will be copied into the DESTINATION subject to control of intervening circuits, which are under the control of the command. Except when DESTINATIONS AR+ and PN+ are selected, the original contents of the DESTINATION line are replaced by the incoming information (ref. Secs. A-7 and C-10h).

C-4b For example: if SOURCE 08, DESTINATION 16, and CHARACTERISTIC 0 are selected, this means that during the time of TRANSFER, the READING FLIP-FLOP of MEMORY LINE 08 will be coupled indirectly to the writing circuit of MEMORY LINE 16, while recirculation of MEMORY LINE 16 is blocked.

C-4c Drawing 20 illustrates the information flow from the READING FLIP-FLOP of the SOURCE line to the writing circuit of the DESTINATION line. The blocks called SOURCE SELECTOR SWITCH and DESTINATION SELECTOR SWITCH are merely portions of the individual memory lines treated collectively. As the notations suggest, activities of the blocks are a function of one or more factors contained in the command being processed.

C-4d Whenever a SOURCE is selected, from the time the STATIC PORTION of a command is read until it is replaced by that of another command, the designated SOURCE will send its information to the EB (EARLY BUS), which is nothing more than a multi-term OR gate. In case SOURCE 27, 30 or 31 is selected, more than one SOURCE line is coupled to the EB; the Boolean algebra notations on Drawing 2 indicate the logical combinations. These combinations are sometimes referred to as the LOGICAL SOURCES; commands employing them are known as EXTRACT COMMANDS. SOURCE 29 will serve to supply nothing but ZEROS to the EARLY BUS unless an extra attachment INPUT-OUTPUT REGISTER is plugged into the G-15D.

C-4e EB (EARLY BUS) information appears on the IB (INTERMEDIATE BUS) subject to modification by the INVERTING GATES. The INVERTING GATES are controlled by command information (ref. Sec. C-7b).

C-4f IB (INTERMEDIATE BUS) information can appear on the LB (LATE BUS) during the time of TRANSFER only. This time-gating by TRANSFER prevents the selected DESTINATION from being influenced at times other than the time of TRANSFER.

SPECIAL DESTINATION 31

C-4g When DESTINATION 31 is selected, the SOURCE code no longer represents a SOURCE to feed a DESTINATION (although the corresponding SOURCE line harmlessly feeds the EB). The SOURCE code designates an operation (or a choice of operations from which one may be selected by the CHARACTERISTIC code). Drawing 3 lists the operations available. (These will be described later in Sec. D.)

THE CONTROL SWITCH

C-5a When a command is read, the STATIC PORTION (T1-T13), which is concerned primarily with the routing of information, is registered in a static register consisting of 13 flip-flops. These are located in the CONTROL SWITCH (Drawing 23), and the entire contents are exhibited on the neon panel (Drawing 17).

C-5b Alteration of information in these flip-flops is possible only during the first 13 pulse periods of the READ COMMAND state defined by RC·CJ. The CX flip-flop can only be triggered when RC·CJ qualifies the AND gates controlling it; the remaining 12 flip-flops can only change state when gated CLOCK pulses are applied to them. These CLOCK pulses are the SHIFT PULSES mentioned in Section B-4. The term permitting generation of these SHIFT PULSES is actually RC·CJ. In conclusion, when a command is read these 13 STATIC FLIP-FLOPS will register T1-T13 (the STATIC PORTION) of the command and will continue to hold the information until equivalent information from the next command replaces it.

C-5c The method of feeding this information into the 13 flip-flops is shown on Drawing 22. Once any information resides in the flip-flops, an array of gates decodes the contents, delivering a variety of signals to control the activities throughout the computer. The decoding scheme is shown on Drawing 23. The output signals are stabilized after T13 of RC, and will remain stable until the end of T1 of the next RC. (During the RC·CJ period, when the flip-flops experience transition, the output signals are not interrogated.)

C-5d A combination of two output signals (Drawing 23) will precisely define a SOURCE or DESTINATION number. For instance DO·DW defines DESTINATION 02 since it is equivalent to $\overline{C6}\cdot\overline{C5}\cdot\overline{C4}\cdot C3.\overline{C2}$ (i.e., 00010_2 or 02_{10} in the DESTINATION flip-flops of the CONTROL SWITCH). Such a signal combination (DO·DW) is used to allow the LATE BUS (LB) to write on LINE 02. (Note on Drawing 9 - lower left - that DO·DW·LB is the writing term of LINE 02 when selected as DESTINATION.)

C-5e Similarly, SO.SW SOURCE codes representing configuration 00010 in the SOURCE flip-flops, are suitable for controlling LINE 02 as a SOURCE. (Note on Drawing 9 that SO·SW·M2 feeds the EARLY BUS when LINE 02 is selected as SOURCE.)

C-5f By forming in this central location (CONTROL SWITCH) key signals to feed the extremities of the computer, economy in wiring and components at the extremities is achieved.

C-5g The signal DS (Drawing 23) is an example of central formation of a signal for use in many locations. DS=D7·DX·TR (i.e., a signal high during TRANSFER if DESTINATION 31 is selected). This signal "operates" the SPECIAL COMMANDS listed on Drawing 3. For instance, to perform the special command "HALT", SOURCE 16 and DESTINATION 31 must be specified (symbol: 16 ⟶ 31). When this configuration enters the 13 flip-flops and when the TRANSFER state arises the signals S4·SU·DS will be present. ($S4\cdot SU\cdot DS = S4\cdot SU\cdot D7\cdot DX\cdot TR = CV\cdot CU\cdot \overline{C9}\cdot \overline{C8}\cdot C7\cdot C6\cdot C5\cdot C4\cdot C3\cdot C2\cdot TR$). The 3-term signal S4·SU·DS (derived from a multitude of terms) is all that is required to initiate the "HALT" command (note dwg. 30 - upper left). The same ingredients, S4, SU, & DS can be used to perform other functions. In case any one signal (such as DS) feeds many loads, it may be "boosted" by simple devices such as cathode-followers; detailed prints supply this type of information.

TRANSFER TIMING

C-6a The DYNAMIC PORTION of a command is concerned with establishing the timing control of the TRANSFER state (TR); however, how the DYNAMIC PORTION is interpreted depends to some extent upon the STATIC PORTION (which resides in the CONTROL SWITCH after T13·RC).

C-6b Drawing 19 illustrates by flow-diagram and examples the various TR timing control options. The DYNAMIC PORTION of a command holds I/D (T29) and T (T28 - T22) information. Furthermore, the factor L (WT_{RC}) has some control on timing. (The N and BP factors, also in the DYNAMIC PORTION, have no bearing on TR timing).

C-6c As the flow diagram shows, I/D and L or T control the initiation of TR regardless of the STATIC PORTION of the command. Termination of TR is a function of the configuration in the STATIC PORTION (i.e., MARK EXIT? SHIFT? MULT? DIV? NORM? S/D?). The CONTROL SWITCH supplies the necessary terms to determine mode of termination; once determined, the termination is performed by the signals occurring at the times shown on Drawing 19.

C-6d In the majority of cases, the "Imm., $\overline{\text{MARK EX.}}$, abs.", "Def., MARK EX., single", or "Def., MARK EX., double" timing will hold true. Note that in the case of SINGLE PRECISION DEFERRED commands, TR lasts one word time only (during WT = T) and in the case of DOUBLE PRECISION, DEFERRED commands, TR lasts 2 word times (T and T+1), provided T is an EVEN number. This is compatible with processing numbers of corresponding precisions.

C-6e IMMEDIATE commands can give rise to TR lasting many word times, hence are capable of processing blocks of numbers (hence, the term BLOCK TRANSFER used in programming language). It can be seen that the S/D bit has no bearing on TR timing in the IMMEDIATE cases; nevertheless, its control over the TS (TIME OF SIGN) signal remains unaffected.

C-6f The signals causing transition (at the bottom of the timing diagram) are generated in the COMMAND REGISTER and associated circuits under the control of the STATIC and DYNAMIC portions of the command. Formation of these signals will be discussed in Section C-17.

THE INVERTING GATES (EB → IB)

C-7a As was mentioned in Sec. C-4e, information may be modified in transit from the EARLY BUS (EB) to the INTERMEDIATE BUS (IB). The modification is under the control of (1) the STATIC PORTION of a command (hence the CONTROL SWITCH), and (2) the SIGNS of the NUMBERS themselves which are being transferred. Since the SIGN bit precedes the number, it is capable of controlling the circuits which process the number to follow.

C-7b The CH (CHARACTERISTIC) bits of the command, in conjunction with the S (SOURCE) and D (DESTINATION) codes control the nature of the modification in accordance with the CHARACTERISTICS TABLE on Drawing 26 upper right. By means of Boolean algebra notation, referring to CONTROL SWITCH output terms, the following transfer characteristics may be obtained:

			ABBREV.
Case I	$\overline{CX}\cdot\overline{CW}$	TRANSFER	TR
	$CX\cdot\overline{CW}\cdot\overline{S7}\cdot\overline{D7}$	TRANSFER VIA AR	TVA
Case II	$\overline{CX}\cdot CW$	ADD	AD
	$CX\cdot CW\cdot\overline{S7}\cdot\overline{D7}$	ADD VIA AR	AVA
Case III	$CX\cdot\overline{CW}\cdot(S7+D7)$	ABSOLUTE VALUE	AV
Case IV	$CX\cdot CW\cdot(S7+D7)$	SUBTRACT	SU

C-7c The CASES (I-IV) mentioned above, control the INVERTING GATES such that they transmit EB information to the IB in the manners indicated at the bottom of Drawing 26. Note that both the SIGN BIT of the number on EB and the CASE (I-IV) determine: (1) the SIGN BIT to be placed in the IB, and (2) whether or not the numerical portion of the EB number should be complemented in transit.

Drawing 26 also shows the INVERTING GATES circuit that performs these operations. CONTROL SWITCH and EB sign information controls the INVERTING GATES via gates 1-5. TS identifies the TIME of SIGN. Since the INVERTING GATES behave in accordance with TS, and TS is controlled by the S/D bit, the S/D bit has an indirect controlling effect on the INVERTING GATES.

C-7e The IS flip-flop, when set, calls for complementation of a number; when reset, the number should be transferred without being complemented (i.e., NORMAL). IS may be called the "WHETHER TO COMPLEMENT FLIP-FLOP". Note also that the RC (READ COMMAND) signal resets IS so that in the absence of any other IS control signals, no complementation will take place.

C-7f In the cases of ABSOLUTE VALUE and SUBTRACT, gate 5 prevents EB information from reaching IB at the time of the SIGN BIT. In the event that a positive number is transmitted with a SUBTRACT characteristic, gate 4 enters a "1" on the IB at sign time to provide the necessary MINUS sign. In all other cases (other than those associated with the 2-WORD LINES), the SIGN BIT on the EB will reach the IB without modification. The treatment of the sign by this circuit fulfills all of the requirements outlined on the chart at the bottom of Drawing 26.

C-7g IC is the flip-flop which scans for the first numerical "1" bit in a number to be complemented. At the beginning of a number (T2 or T2·CE), IC will be in the reset state allowing EB to reach IB without modification. If IS has been set ("WHETHER TO COMPLEMENT"), the first EB "1" bit thereafter (during TRANSFER) will set IC causing every EB bit that follows to arrive on IB inverted (i.e., after IC is set, $IB = \overline{EB}\cdot\overline{TS}\cdot IC$). This circuit fulfills all requirements of the complementation of numbers technique described in Section C-3f-k. The sole purpose in qualifying gate 6 by TR is to prevent random setting of the OVERFLOW FLIP-FLOP (ref. Sec. C-11).

IB ⟶ LB

C-8a IB information can appear on the LATE BUS (LB) only during the time of TRANSFER (TR). If the CONTROL SWITCH yields the signal $\overline{CS}$ meaning "NOT VIA AR", this results in LB = IB·TR.

C-8b If the CONTROL SWITCH yields the signal CS this calls for a "VIA AR" characteristic and IB will be routed via the 1 word memory line AR in transit to LB.

C-8c This results in the following: (1) During the first word time of TRANSFER the original contents of AR will appear on the LB; (2) During the remaining word time(s) of TRANSFER, IB will appear on the LB delayed by one word time; and (3) During the last word time of TRANSFER, IB will be stored in AR (but will not reach the LB). This operation is a powerful programming tool.

C-8d In either case (VIA AR or NOT VIA AR) the LB will only contain information during the time of TRANSFER and consequently cannot influence DESTINATIONS at any other time.

EXECUTION OF A SAMPLE COMMAND

C-9a The performance of a sample command will now be illustrated to tie together some of the circuits and concepts discussed so far. The command is as follows:

```
I/D      T        BP       N        CH     S       D     S/D
 ↓   ___/\___     ↓   ___/\___    _/\_  __/\__  __/\__   ↓
 1 0 0 0 0 1 1 1 0 0 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 1 1 0
 ↑                                                       ↑
T29                                                      T1
          (L = 0 0 0 0 0 0 1 = 01)
```

C-9b The binary configuration of this command (one of the 536,870,912 possible configurations) states the following:

(L = 01	i.e. the command is read during WT 1.)
I/D = 1	i.e. the command is DEFERRED.
T = 07	i.e. TRANSFER will be initiated at the beginning of WT 7 by T29·(T-1). For termination see S/D.
BP = 0	i.e. when this command has been performed, advance, non-stop, to the next command.
N = 10	i.e. the NEXT command is to be read during WT 10

CH = 1	i.e. ADD characteristic - complement negative numbers, pass positive numbers unchanged.
S = 05	i.e. MEMORY LINE 5 will feed the EARLY BUS
D = 07	i.e. the LATE BUS will feed the writing station of MEMORY LINE 7 during the time of TRANSFER. Also, recirculation of LINE 7 will be blocked during this time.
S/D = 0	i.e. SINGLE PRECISION: (1) TS will = T1, and (2) TRANSFER will be terminated at the end of WT 7 by T29·TR)

C-9c Result: This command, read at WT 1, causes LINE 5 to copy its contents into LINE 7 during WT 7, subject to complementation if the number in LINE 5, WT 7 is negative. The next command will be read from WT 10. The computer cycle is as follows:

RC (READ COMMAND)	WT 1	i.e. L
WTR (WAIT TO TRANSFER)	WT's 2, 3, 4, 5, 6	
TR (TRANSFER)	WT 7	i.e. T
WRC (WAIT TO READ COMMAND)	WT's 8,9	
RC (READ COMMAND - next)	WT 10	i.e. N

OPERATION ANALYSIS

C-9d (Ref. Drawing 22) During RC the command is read from a memory line previously selected and appears inverted as $\overline{MC}\cdot CG\cdot RC$. During the first 13 pulse periods of RC, RC·CJ allows the STATIC PORTION of the command to enter the 13 STATIC FLIP-FLOPS (C1-CX). The DYNAMIC PORTION, selected by RC·CJ, enters the COMMAND REGISTER ADDER (discussion in Sec. C-17) to yield a trigger pulse to initiate TR at T29·(T-1).

C-9e After T13 of RC, the 13 STATIC FLIP-FLOPS in the CONTROL SWITCH stabilize yielding the following signals:

$\overline{C1}$	Means SINGLE PRECISION: (1) controls the TIMING GATES to yield TS=T1 and (2) sets up CONTROL GATES to terminate TRANSFER at ~~T29·(T-1)~~. T29 ·TR
S1,SV	SOURCE designators: qualify read-out gate of LINE 5, therefore EB = M5·S1·SV
D1,DX	DESTINATION designators: qualify writing gate of LINE 7, yielding write term = LB·D1·DX. Also, during TR, the term $\overline{D1\cdot DX\cdot TR}$ is absent. $\overline{D1\cdot DX\cdot TR}$ qualifies recirculation of LINE 7. During TR recirculation is blocked since the recirculation term of LINE 7 is M7·$\overline{D1}$+M7·$\overline{DX\cdot TR}$. (DeMorgan's Law)
$\overline{CX}\cdot CW$	CHARACTERISTIC designators: These qualify gates 2 and 3 controlling the IS flip-flop in the INVERTING GATES so that TS·EB will set IS or TS·$\overline{EB}$ will reset it, consequently complementing the EB number (M5·S1·SV) in transit to IB in accordance with its sign.
$\overline{CS}$	CHARACTERISTIC designator: means "NOT VIA AR". LB will = IB·$\overline{CS}$·TR and will constitute the information to be written into the DESTINATION, LINE 7.

C-9f The following prints may be consulted to verify the above:

	DWG. NO'S.
"Control Switch":	23
"Timing gates" (for TS):	15
"Memory Lines":	3D296, 3D297
"Inverting Gates":	26

C-9g It may be seen that a variety of commands of this sort may be written and analyzed in a manner similar to that above.

ADDERS

C-10a The G-15D is provided with three adders (Drawing 27):

(1) AR (ACCUMULATOR REGISTER) - a single precision (1 word) adder
(2) PN (PRODUCT-NUMERATOR REGISTER) - a double precision (2 word) adder
(3) CM (COMMAND REGISTER) - a 1 word adder for special purposes. It is not available to the programmer.

C-10b The AR and PN are available for use by the programmer as general purpose adders. They are also employed to facilitate operations involved in certain special commands. (i.e. AR is used in conjunction with SHIFT and NORMALIZE, PN with MULTIPLY and DIVIDE.)

C-10c In addition to their adder capabilities, AR and PN also serve as rapid-access memory lines in that unless a NON-ZERO addend is being added to either of their contents, the contents remain unchanged (i.e., $n + 0 = n$) and merely recirculate in the line, available for many purposes.

C-10d Associated with each adder are three major terms: (1) the AUGEND (U), (2) the ADDEND (D), and (3) the SUM (A). In addition to these, there is the CARRY (C) term and its control system. By programming the control of U and D, the following operations are available pertaining to AR and PN:

AUGEND (U)	+	ADDEND (D)	=	SUM (A)	
U	+	(D=0)	=	U	(recirculation)
(U=0)	+	D	=	D	(read-in)
U	+	D	=	U+D	(addition)

C-10e In any case involving either U or D equal to zero, the CARRY CIRCUIT will be inactive unless triggered by some external signal.

C-10f ADDER RECIRCULATION: If programmed reference is not made to either AR or PN, whatever number happens to be in the adder (resulting from a previous operation) will recirculate as follows: A bit at the READING FLIP-FLOP will be applied to the AUGEND to which "0" will be "added" via the inactive ADDEND. This results in a SUM equal to the AUGEND. The SUM is written and will re-appear at the READING FLIP-FLOP during the next recirculation cycle.

C-10g ADDER READ-IN: When an adder is programmed as destination (but not to perform an addition), during the time of TRANSFER recirculation is blocked. That is, the information from the READING FLIP-FLOP is not allowed to reach the AUGEND input to the adder gates. Simultaneously the LB (LATE BUS) is applied to the ADDEND. This means that the writing term, A (SUM), is equal to U+D = 0+LB = LB. (Hardware is illustrated on Drawing 27.)

C-10h ADDITION: An addition is based upon the assumption that the AUGEND term is recirculating in the line. If AR+ or PN+ is selected as destination, the LB will feed the ADDEND term from the appropriate SOURCE line during the time of TRANSFER. The recirculating AUGEND term will not be blocked. The result is that a set of gates, in conjunction with the CARRY flip-flop, will add the two terms (U and D) yielding their sum, A, which will be written on the adder's line to re-appear at the READING FLIP-FLOP during the next recirculation cycle.

C-10i SUBTRACTION: An adder may perform a subtraction by adding the negated ADDEND term. Negation of the ADDEND is performed in the INVERTING GATES which are controlled mainly by the CHARACTERISTIC (CH) bits of the command.

C-10j In loading an adder with AUGEND and ADDEND terms, the CH bits usually are selected to provide either the ADD or SUBTRACT characteristic. Below are examples, using AR, to illustrate ADDITION and SUBTRACTION programming:

ADDITION: $S+S' \longrightarrow A \longrightarrow$ AR write

	S	CH	D	SYMBOL
Load AUGEND	S	1	28	$S \xrightarrow{AD} AR_C$
Load ADDEND	S'	1	29	$S' \xrightarrow{AD} AR_+$

--the SUM is generated at the same time the ADDEND is entered

SUBTRACTION: $S-S' \longrightarrow A \longrightarrow$ AR write

	S	CH	D	SYMBOL
Load AUGEND	S	1	28	$S \xrightarrow{AD} AR_C$
Load ADDEND	S'	3	29	$S' \xrightarrow{SU} AR_+$

--the SUM (in this case DIFFERENCE) is generated at the same time the ADDEND is entered.

C-10k The ADD characteristic should be used even when loading the AUGEND. This is necessary in case the AUGEND term is a negative number. In this case the INVERTING GATES will complement the number. This is a requirement of the arithmetic.

C-10l The internal workings of the AR adder follow a conventional pattern. Addition, like transfer, is serial, bit-by-bit. Needless to say, the bits must be added starting with the lowest order bit for CARRY purposes. (This is the reason data is handled lowest order bit first and the time axis, for convenience, is usually considered going from right to left. Right-to-left time places the lowest order bit to the right. Oscilloscope horizontal-deflection plates may be reversed for this reason.)

C-10m As the reader may recall, the SIGN BIT occures at T1 of a SINGLE PRECISION number, therefore, the lowest order bit in a number is T2. An END CARRY from the T29 bit can influence the sign bit as the following paragraphs will reveal.

C-10n Prior to the addition of two numbers, the SIGN BITS (T1 of the AUGEND and ADDEND) are added, producing the UNCORRECTED SIGN bit in the SUM. No CARRY is allowed to emerge from T1 to influence the numerical portion. Furthermore, the CARRY flip-flop is unconditionally reset at the end of T1 time so it will "contain zero" at T2.

C-10o Starting with T2, the bits are added, producing the sum. Should an END CARRY emerge from T29 (highest order bit), it will be added to the UNCORRECTED SIGN during T1 of the following word time. This is because T1 of the original SUM (i.e., the UNCORRECTED SIGN) appears as the T1 AUGEND bit after the 1 word delay in the line. The final result in T1 of the SUM is the CORRECTED SIGN. The processing of the sign bit takes place twice--at the beginning of a number, then again at the end. The effect is the same as if it had all been accomplished at T1 following the highest order numerical bit (T29). An ADDITION example is provided on Drawing 29.

C-10p The principle upon which the DOUBLE PRECISION adder (PN) operates is the same as that employed by AR except that TS only occurs at T1 of EVEN word times (TE = T1·CE) and the highest order bit is T29 of the following ODD word time (T29·CE). T29 and T1 at the junction of the EVEN and ODD words (T29·CE and T1·CE) are numerical bits and are treated accordingly.

C-10q Drawing 27 illustrates the three adders. CM,which is not a general-purpose programmable adder, is discussed in Sec. C-17.

C-10r Note that CARRY FLIP-FLOP control differs in the AR and PN. The result is the same; only the means differ. The AR CARRY FLIP-FLOP (AC) is set or reset every single pulse period (i.e., if two or more ONES exist in U, D, and C, set AC -- otherwise reset AC). The PN (and CM) operate on the ORIGINATE-PROPAGATE-KILL basis (i.e., leave the CARRY flip-flop in its previous state unless conditions of U, D, and C call for a change.)

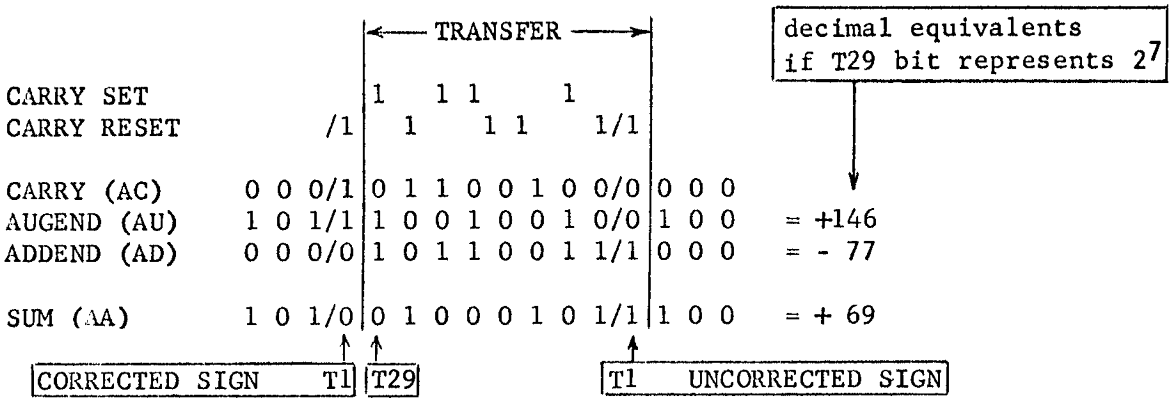
C-10s The latter case conserves hardware; the former case is required for the benefit of an external circuit (CONTROL GATES: in terminating TRANSFER in the case of a SHIFT command - see D-12e). Determination of sum bits is identical in AR, PN, and CM.

C-10t The CARRY set term for AR is supplemented by $T29 \cdot TR \cdot D7 \cdot \overline{C3} \cdot IS \cdot \overline{IC} \cdot \overline{AD}$, and that of PN by $T29 \cdot TR \cdot CE \cdot DW \cdot C6 \cdot C5 \cdot IS \cdot \overline{IC} \cdot PD$. These terms identify "MINUS ZERO" reaching the adder in question from the INVERTING GATES at the time of the highest order bit. By setting CARRY at this time, the CORRECTED SIGN bit will be made equal to ZERO, preventing MINUS ZERO as a number from engaging in any adder activity. Drawing 27 indicates the purpose of the various terms listed above.

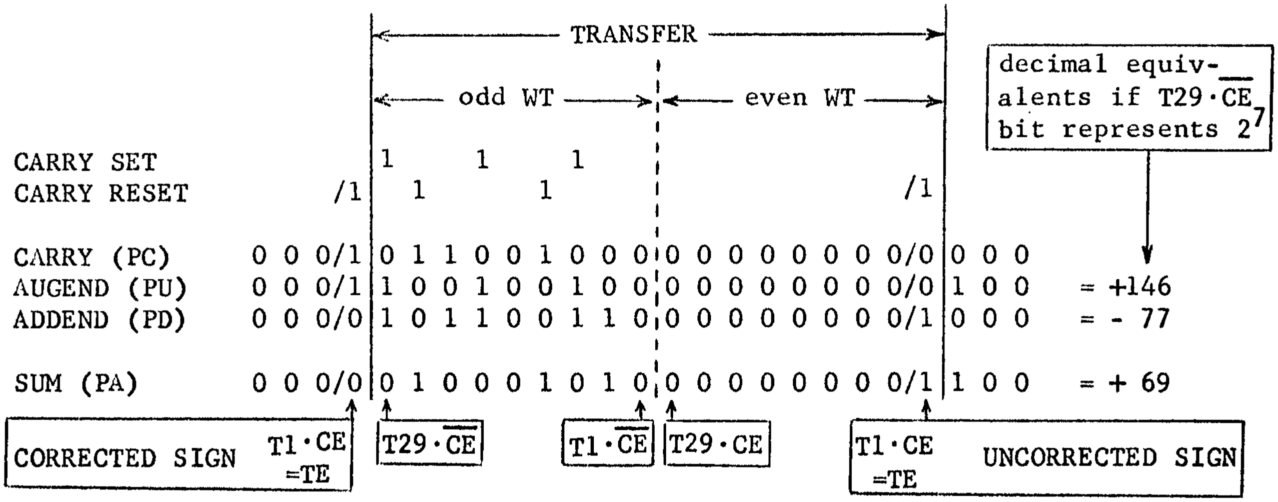
(MINUS ZERO, though equal in magnitude to the normal PLUS ZERO, is incompatible with the SIGN and NUMBER scheme employed in the adders.)

C-10u To summarize ADDER activity, below are two examples showing addition of numbers of unlike sign (using 9-bit word examples for the sake of brevity):

ACCUMULATOR REGISTER (AR):



PRODUCT-NUMERATOR REGISTER (PN):



C-10v COMMAND CONTROL OF THE ADDERS: Needless to say, the AUGEND and ADDEND terms are under the control of the command which makes reference to the adder in question. The STATIC PORTION of the command, registered in the 13 STATIC FLIP-FLOPS yields the necessary output terms from the CONTROL SWITCH as follows:

AR:

(1) Block AUGEND recirculation: D7·DU·TR = DESTINATION 28 during time of TRANSFER

(2) Supply LATE BUS to ADDEND: D7·DV·LB + D7·DU·TR·LB = AD during time of TRANSFER if DESTINATION = 28 or 29. (TR in the term above is a harmless redundancy; it can be attributed to hardware conservation.)

PN:

(1) Block AUGEND recirculation: D6·DW·TR = DESTINATION 26 during time of TRANSFER

(2) Supply LATE BUS to ADDEND: $LB\cdot D6\cdot DW\cdot TR\cdot\overline{CE\cdot CS} + LB\cdot D7\cdot DW = PD$ during time of TRANSFER if DESTINATION = 26 or 30 (subject to control in case of DEST. = 26 by $\overline{CE\cdot CS}$ to be discussed in Section C-12d.

C-10w In both cases (AR and PN), other terms serve to control A and U to facilitate certain SPECIAL COMMANDS. The terms above pertain only to AR, AR+, PN and PN+ as DESTINATIONS. The READ-OUT gates follow the same pattern as general-purpose memory lines.

C-10x BLOCK ADDITIONS: It is perfectly legitimate to accumulate the sum of many numbers by allowing TRANSFER to last for several word times. In such a case, ADDENDS appear one right after the other with no "barrier" pulse periods. This means that, CORRECTED SIGN of one number will be processed in the adder at the same time as UNCORRECTED SIGN of the next number (at TS time). This, however, is permissible since the net result will be the legitimate UNCORRECTED SIGN of the second number. Drawing 29 is an example of such a case.

OVERFLOW DETECTOR (FO)

C-11a An overflow arising due to an addition may be defined as the magnitude of a sum exceeding the capacity of the adder. That is, if an adder is assumed to accommodate fractional numbers only, but as the result of adding two fractional numbers a sum is produced equal to or greater than unity, the integral portion (2^0), for which the adder has no accommodation, constitutes an overflow. Such a case can only arise from addition of numbers of like sign, which may be identified by a "0" in the UNCORRECTED SIGN bit.

C-11b An overflow may be identified by comparing certain factors including: UNCORRECTED SIGN, SIGN of ADDEND, END CARRY, etc. Drawing 27 (top) indicates the factors compared, with notes indicating the significance of the signal combinations.

C-11c The detector circuit is required to detect overflows in both the AR and PN. Furthermore, discriminating terms (from CONTROL SWITCH) are required to prevent conditions in one adder from adversely influencing the detector gates interrogating the other adder.

C-11d The term DS, which holds FE reset, prevents the OVERFLOW FLIP-FLOP (FO) from being set during a DIVIDE operation. A DIVIDE may yield legitimate overflows in PN. The DIVIDE system can set FO by "CIRCLE X" (ref. Sec. D-11ae).

C-11e The "DA-1 OVERFLOW" term can only arise if a DA-1 unit is plugged into the G-15D and is operating.

C-11f Once the OVERFLOW FLIP-FLOP (FO) is set, it will accomplish nothing unless tested by the "OVERFLOW to TEST" command (see Secs. D-14F and C-19).

This command will reset FO upon interrogation, clearing it for the next overflow. The condition of FO is exhibited on the NEON PANEL (Drawing 17).

THE TWO-WORD LINES: ID, MQ, AND PN

C-12a The two-word lines are primarily for special purposes such as MULTIPLY and DIVIDE. To facilitate these operations, certain control features are associated with information transfer to and from them. These features affect the READ-IN activity of the lines and the INVERTING GATES. Such activity is under the control of the CHARACTERISTIC bits of the associated command.

C-12b If the CH specifies anything other than TRANSFER (TR) or TRANSFER VIA AR (TVA), the two-word lines behave just as other lines do as far as READ-IN and READ-OUT are concerned. In the event that one of these lines is selected as SOURCE or DESTINATION the TR or TVA characteristic will control activity as follows:

C-12c READ-IN (Ref. Drawing 34): If ID, MQ, or PN is selected as DESTINATION with a TR or TVA characteristic, EB will be transmitted to IB; however, the SIGN BIT of each number will be blocked in transit, supplying only the absolute value to IB. IB will feed LB according to the usual rules. The SIGN BIT is fed to the IP FLIP-FLOP circuit (ref. Sec. C-13).

C-12d The LB signal will appear at the READ-IN gates of the 3 lines. CONTROL SWITCH terms will qualify the READ-IN gates and block recirculation as follows when the line in question is selected as destination:

ID:

(1) $TR \cdot D6 \cdot DV$ blocks recirculation during time of TRANSFER

(2) $TR \cdot D6 \cdot DV \cdot LB \cdot \overline{CS \cdot CE}$ writes LB in the line. The $\overline{CS \cdot CE}$ term allows LB to be written during the entire time of TRANSFER if TR, AD, AV, or SU is the characteristic. If TVA or AVA is the CHARACTERISTIC, during EVEN word times nothing is written (i.e. ZEROS); during ODD word times LB is written. This permits transfer of a SINGLE PRECISION word from an EVEN word time to the ODD (highest order) word time of a two-word line, padding the EVEN word time with ZEROS regardless of the original contents of AR. (Note that ID has only a 57 pulse delay in the line but a compensatory 1 bit delay exists in PI. PJ may be thought of as the READ-OUT FLIP-FLOP since it's output is appropriately phased.)

PN:

(1) $TR \cdot D6 \cdot DW$ blocks recirculation of the AUGEND during time of TRANSFER.

(2) $TR \cdot D6 \cdot DW \cdot LB \cdot \overline{CS \cdot CE}$ enters ~~LB~~ PN as the ADDEND. $\overline{CS \cdot CE}$ performs the same function as mentioned in the case of ID. (If PN+ is selected as destination, $CS \cdot CE$ does not apply; furthermore, no unusual INVERTING GATES activity will take place.)

(3) In the event that ID is selected as destination with a TR or TVA characteristic, recirculation of PN (AUGEND) will be blocked during the time of TRANSFER by $TR \cdot D6 \cdot DV \cdot \overline{CW} \cdot (CS+\overline{CX})$.

This interaction means that loading ID with CH = TR or TVA loads ZEROS in PN. This is a programming convenience prior to a MULTIPLY command.

MQ: (1) TR·D6·DU blocks recirculation during time of TRANSFER.
(2) TR·D6·DU·LB·$\overline{\mathrm{CS}\cdot\mathrm{CE}}$ writes LB in the line during TRANSFER. Again, $\overline{\mathrm{CS}\cdot\mathrm{CE}}$ controls read-in as in the case of ID.

C-12e READ-OUT: Information will be coupled to the EARLY BUS (EB) in the same manner as that in other lines. That is, CONTROL SWITCH terms allow the READING FLIP-FLOP of the appropriate line to reach EB.

C-12f The activity of the INVERTING GATES in transmitting EB to IB will be subject to supplementary control if one of the two-word lines is selected as SOURCE and certain other conditions exist as outlined in Sec. C-13 and illustrated in Drawing 34.

C-12g Several other terms exist to control recirculation, READ-IN and READ-OUT of these lines. They are only active when certain SPECIAL COMMANDS are programmed and shall be discussed later.

THE IP FLIP-FLOP

C-13a The IP FLIP-FLOP circuit in the INVERTING GATES deals with SIGN information in cases where two-word lines are involved in READ-IN or READ-OUT and a TR or TVA characteristic is used.

C-13b In most operations related to use of the two-word lines, only absolute values of numbers are desired. SIGN information is "side-tracked" during EB to IB transmission and "stored" in the IP FLIP-FLOP when destination is ID, MQ, or PN and TR or TVA is the CHARACTERISTIC. Then, when a number in ID, MQ or PN is to be transmitted through the INVERTING GATES, the "stored" sign information is sent from IP to the IB: effectively re-assembling the SIGN and ABSOLUTE VALUE.

C-13c For example, when a MULTIPLY is to be performed, ID (MULTIPLICAND) and MQ (MULTIPLIER) are loaded with ABSOLUTE VALUES only. When the two lines were loaded, SIGN information from each number set up the IP FLIP-FLOP such that it contains the SIGN of the product to be formed by the multiplication to follow. (i.e. + x + = +, + x - = -, - x + = -, and - x - = +). When the product is formed in PN, it will be in terms of absolute value. Then when PN (PRODUCT) is transferred to memory with a TR or TVA characteristic the STORED SIGN is attached to the ABSOLUTE VALUE.

C-13d If a two-word line is the SOURCE and another two-word line is DESTINATION, the IP FLIP-FLOP will remain static. This permits data transfer among these lines to be programmed without affecting IP. Nevertheless, in such a transfer, sign information is blocked in the INVERTING GATES.

C-13e A special operation is available which appears contrary to all rules: if PN is both SOURCE and DESTINATION and TR is the characteristic, the contents of PN remain unchanged if a POSITIVE SIGN exists in IP, but will be COMPLEMENTED if a NEGATIVE SIGN is in IP. Furthermore, if a NEGATIVE SIGN is in IP, PN will acquire a "1" in its TS position. This is accomplished in the INVERTING GATES by gate 1 and gate D (dwg. 34). The operation is a convenience to the programmer, enabling him to use a PRODUCT as an AUGEND for a future ADD or SUBTRACT operation.

C-13f Drawing 34 (top) illustrates the hardware associated with the IP FLIP-FLOP and should serve to indicate the resulting activity in any particular case. The chart at the upper right illustrates how the IP FLIP-FLOP will register a PRODUCT or QUOTIENT sign according to the law of signs, provided ID is the first of the two registers to be loaded prior to a MULTIPLY or DIVIDE command. Drawing 35 shows some examples of READ-IN and READ-OUT.

THE "LOGICAL" SOURCES and SOURCE 29

C-14a The "LOGICAL" SOURCES are source numbers 27, 30, and 31. Drawing 2 defines these sources; drawing 28 shows how the appropriate terms qualify the EARLY BUS.

C-14b SOURCE 29 involves transmission of certain signals to a connector on the back of the computer into which an INPUT-OUTPUT REGISTER accessory may be plugged. These signals may be found on Drawing 23 (lower right); however, there is no need to consider them unless the accessory is used. If the accessory is not employed, the term IR will be at -20V and source 29 will constitute a convenient source of ZEROS to feed a DESTINATION when required.

THE FOUR-WORD LINES (M20 - M23)

C-15a These lines, sometimes called the RAPID-ACCESS LINES, combine the economy and versatility of drum storage with the speed of other types of storage media. Their read-in, read-out, and recirculation features resemble those of the general-purpose 108 word lines; however, LINE 23 has supplementary control features for the benefit of the INPUT/OUTPUT system.

C-15b Addressing of these lines is on the basis of "modulo 4". That is, each line has four words, numbered 0,1,2, and 3, which may be addressed during the 108 words of a drum cycle as follows:

Word 0 - word times ≅ 0 mod 4
Word 1 - word times ≅ 1 mod 4
Word 2 - word times ≅ 2 mod 4
Word 3 - word times ≅ 3 mod 4

C-15c For instance, word 1 of LINE 20 may be addressed during WT 1, 5, 9, 13, 17, etc. The word-time cycle on Drawing 6 indicates by markers the recirculation cycles of these lines. TF (i.e. T29·CE·CF) is the signal indicating the end of a 4-word recirculation cycle as TO indicates the end of a 108-word recirculation cycle.

SOURCE AND DESTINATION RESTRICTIONS

C-16a LINE 0 and LINE 1: Words 107 of these two lines are reserved for the typewriter MARK and RETURN features (ref. Sec. E-9).

C-16b LINE 2 and LINE 3: Words 0-3 of these two lines are employed by the OUTPUT system. Programmed reference can be made to these words during an OUTPUT operation only under well calculated conditions.

C-16c LINE 19 and LINE 23: These lines are employed by the INPUT-OUTPUT system and should not be referred to in a program during such an operation.

C-16d LINES 14, 16, 17, 21 and 22: These lines are employed by the DA-1 (DIGITAL DIFFERENTIAL ANALYZER attachment). If such an attachment is in use and is in the "GO" state, the following terms control the lines:

LINE NO.	PERMIT RECIRC.	WRITE
14	$\overline{GO}$	M14W
16	$\overline{GO}$	M16W
17	$\overline{GO}$	M17W
21	$\overline{GO}$	ZEW
22	$\overline{GO}$	ZSW

C-16e If the DA-1 is in the "GO" state, $\overline{GO}$ is at -20V and blocks recirculation of the lines while terms arising from the logic of the DA-1 become the writing terms. If no DA-1 is attached, restrictions on use of these lines need not be considered.

THE COMMAND REGISTER (CM)

C-17a The COMMAND REGISTER is a one-word adder, the function of which is to arithmetically determine the times at which the computer should advance from state to state (i.e. RC, WTR, TR and WRC).

C-17b Unlike many computers, the G-15D does not employ "coincidence detectors" to identify word times around the drum. Instead, the COMMAND REGISTER will yield END CARRIES at times which are a function of the T and N numbers of a command. These END CARRIES will occur in accordance with the requirements of Drawing 19 (for TRANSFER TIMING).

C-17c For instance, take the example of "Def., $\overline{\text{MARK EX.}}$, single" on Drawing 19. A signal is required to initiate TRANSFER at T29·(T-1). This signal is actually T29·CC, an END CARRY out of the T28 bit of the COMMAND REGISTER, high during T29 of WT = T-1.

C-17d When the command was read during WT 3 (L = 3), the T22 - T28 bits of the command contained $T = 8_{10} = 0001000_2$. This information was directed (in inverted form) into the AUGEND term of the COMMAND REGISTER (i.e., CU). Simultaneously, the previously recirculating AUGEND was blocked. Refer to Drawing 22: The "block old AUGEND recirculation" term is $RC \cdot \overline{CJ}$; the new AUGEND term is $RC \cdot \overline{CJ} \cdot MC \cdot \overline{CG}$. In the latter, $\overline{MC}$ is the INVERTED COMMAND, and $\overline{CG}$ is a control term assumed to be high unless a special command ("NEXT COMMAND FROM AR") is being obeyed (ref. sec. D-16).

C-17e Among other terms which enter CU is the T22 - T28 ("T" number) information, which is: 1110111. This is 0001000 inverted, and may be thought of as representing "-8" in the "1's COMPLEMENT SYSTEM" (inversion yields this form of complement). Assuming the lowest order bit (T22) represents 2^0 of the T number, the 1110111 configuration will represent 2^7-9, or a departure from an END CARRY (2^7 position) by a factor of 9.

If we should choose to represent the same binary configuration (1110111) in terms of the "2's COMPLEMENT SYSTEM" and "T", it is 2^7-T-1 = 128-T-1. (Ref. sec. C-3k-m)

C-17f The command was read during WT 3. At the same time that the above AUGEND (128-T-1) was being established, the NUMBER TRACK (CN) information entered the ADDEND under control of the CT flip-flop, which, in the "Def., MARK EXIT., Single" case, is high to include T3 - T28 of RC. Drawing 6 illustrates the contents of CN (the WORD-TIME reference track). From Drawing 6 it may be determined that T22 - T28 contains a factor = 'WT + 1' in all words other than WORD 107. In this case, 'WT +1' = L+1 = 3+1 = 4 = 0000100.

C-17g Drawing 22 will reveal that T21 unconditionally sets CC (CM CARRY FLIP-FLOP), rendering it high at T22 time, effectively adding a ONE to the 2^0 position of the sum. The result in the COMMAND REGISTER is as follows: CU = 128-T-1, CD = L+1, and CC = 1, yielding a sum, CA, of 128-(T-L-1), which represents a departure from 128 (END CARRY in T29) be a factor of the relative time elapsing between T29·L (i.e. T29·RC) and T29·(T-1). This relative time amounts to -(T-L-1), in this case = -(8-3-1) = -4, and will appear as the CA term in the "2's COMPLEMENT SYSTEM" form (i.e., 2^7-4 = 128-4 = 124 = 1111100_2. (The "1" in the CN 'WT+1' factor may be thought of as a $+2^{-n}$ correction factor to compensate for the negative AUGEND appearing in the "1's COMPLEMENT SYSTEM" form.)

C-17h Unconditionally, during every word time, the COMMAND REGISTER CARRY FLIP-FLOP (CC) will be high at T22 time. Also, during each word time following RC, CU = CA of the previous word time due to the one word delay in the line and the fact that the READING FLIP-FLOP supplies the AUGEND. In consequence, the SUM is increased by ONE each word time. In the example above, at T29 of the fourth word time after T29·L, the sum will represent 128-4+4 = 128-0. An END CARRY will be in CC at T29 and T22-T28 of CA will contain all ZEROS. This END CARRY, T29·CC, is the T29·(T-1) which will initiate the TRANSFER state.

C-17i This T29·CC will produce a "1" in T29·CA and will be written in the CM line. This will appear as T29·CM during the following word time and 127 word times to follow. Use of this is made in a discriminatory circuit discussed in Section C-18h.

C-17j A summary of the COMMAND REGISTER activity dealing with the "T" number using the example above is as follows:

(See next page)

				T28						T22		L = 3, T = 8 (abs.)
	AUG	(CU):	X	1	1	1	0	1	1	1	= 128-T-1	= inv. T no. from command
WT 3	ADD	(CD):	0	0	0	0	0	1	0	0	= +L+1	= CN info. = WT+1
(L)	CAR	(CC):	0							1	= +1	= add 1 [illegible] (CC_s = T21)
	SUM	(CA):	X	1	1	1	1	1	0	0	= 128-(T-L-1)	= ~~add 1 (CC_s = T21)~~ neg. rel. time
	AUG		0	1	1	1	1	1	0	0	= 128-4	= SUM del. one WT
WT 4	ADD			0	0	0	0	0	0	0	= 0	= (no addend term)
	CAR									1	= +1	= add 1
	SUM			1	1	1	1	1	0	1	= 128-3	= neg. rel time remaining
	AUG			1	1	1	1	1	0	1	= 128-3	
WT 5	ADD			0	0	0	0	0	0	0	= 0	
	CAR									1	= +1	
	SUM			1	1	1	1	1	1	0	= 128-2	= neg. rel time remaining
	AUG			1	1	1	1	1	1	0	= 128-2	
WT 6	ADD			0	0	0	0	0	0	0	= 0	
	CAR									1	= +1	
	SUM			1	1	1	1	1	1	1	= 128-1	= neg. rel time remaining
	AUG			1	1	1	1	1	1	1	= 128-1	
WT 7	ADD			0	0	0	0	0	0	0	= 0	
(T-1)	CAR		1							1	= +1	
	SUM		1	0	0	0	0	0	0	0	= 128-0	= 0 time remaining

T29·CC

C-17k The example above does not include the case in which the boundary between WT 107 and WT 0 is crossed in the timing cycle. In such a case, an addition of a "CORRECTIVE 20" takes place during WT 107. This CORRECTIVE 20 may be considered a factor which, when added to the 108 CARRIES added during the course of one drum revolution yields a total of 128 or 2^7 units of addition. 128 units of addition increase the magnitude of the number in CM (T22 - T28) by a net amount of ZERO since the END CARRY effectively subtracts 128 from the 128 added. Perhaps a more convenient way of interpreting the CORRECTIVE 20 is to consider it representing 128-108 = 2^7-108 = "-108". Whenever WT 107 is passed, the next WT is 0 instead of 108. The "-108" can be thought of as "changing" WT "108" into WT 0.

C-17l The example below may serve to illustrate the function of CORRECTIVE 20:

```
                           T28          T22        L = 105, T = 2 (abs)
                            |            |
                            v            v
          AUG  (CU): X| 1 1 1 1 1 0 1 | = 128 -T-1  = 128 -2-1  = 128 -3
WT 105    ADD  (CD): 0| 1 1 0 1 0 1 0 | =     +L+1  =    +105+1 =    +106
 (L)      CAR  (CC): 1|             1 | =-128*  +1  =-128*  +1  =    -127
                     -  -------------                             --------
          SUM  (CA): X̄| 1 1 0 1 0 0 0 | = 128 -(T-L-1)-128*     = 128-24

          AUG        0| 1 1 0 1 0 0 0 | = 128 -24         (* END CARRY subtracts
WT 106    ADD         | 0 0 0 0 0 0 0 | =       0            128 from SUM)
          CAR         |             1 | =      +1
                      | ------------- |   --------
          SUM         | 1 1 0 1 0 0 1 | = 128 -23

          AUG         | 1 1 0 1 0 0 1 | = 128 -23
WT 107    ADD         | 0 0 1 0 1 0 0 | =     +20 = CORRECTIVE 20
          CAR         |             1 | =      +1
                      | ------------- |   --------
          SUM         | 1 1 1 1 1 1 0 | = 128  -2 = neg. rel. time remaining
______________________|_______________|______________________________________

          AUG         | 1 1 1 1 1 1 0 | = 128  -2
WT 0      ADD         | 0 0 0 0 0 0 0 | =       0
          CAR         |             1 | =      +1
                      | ------------- |   --------
          SUM         | 1 1 1 1 1 1 1 | = 128  -1 = neg. rel time remaining

          AUG         | 1 1 1 1 1 1 1 | = 128  -1
WT 1      ADD         | 0 0 0 0 0 0 0 | =       0
(T-1)     CAR        1|             1 | =      +1
                    / - ------------- |   --------
          SUM      / 1| 0 0 0 0 0 0 0 | = 128  -0 = 0 time remaining
                  /
           |T29·CC|
```

C-17m Since the NUMBER TRACK contains "CORRECTIVE 20" instead of "WT+1" during WT 107, The COMMAND REGISTER will not function properly in obtaining the relative timing factor if RC takes place during WT 107. Although it is possible to calculate programming methods to compensate for this discrepancy, WT 107 is <u>disqualified</u> as a storage location in command lines 00 and 01 (ref. sec. C-16c). Therefore, in general, use of WT 107 as a command location is not recommended. If WT 107 is to be used as a command location the T and N numbers must be 20 higher than the values normally calculated. In cases of MULTIPLY, DIVIDE, SHIFT, and NORMALIZE, only the N number should be so treated.

C-17n During the READ COMMAND state, when the NEGATIVE RELATIVE TIMING NUMBER is initially established in the COMMAND REGISTER, a ONE may appear in the SUM term at T29 time (T29·CA). This is a function of (1) the I/D information from the command, which enters the AUGEND at T29·RC time, and (2) the possibility of an END CARRY, T29·CC, which can arise as a result of the arithmetic in this initial iteration. To assure that a ZERO will be written in the line at this time, CA is qualified by $\overline{T29}$ + CQ + CL + $\overline{CK}$, which excludes the possibility of a ONE being written at T29·RC time. In consequence, the T29·CM term cannot contain a ONE until one word time after a T29·CC·$\overline{RC}$. (Section C-18h makes reference to this particular bit.)

C-17o In the event that a command is read during one drum cycle and the T29·CC should occur during the next, the arithmetic (by virtue of the "CORRECTIVE 20") will still yield the T29·CC at WT = T-1. Also, once a command is read, the T29·CC will be generated at T29 of WT = T-1 of all drum cycles to follow until a new command replaces the old one.

RELATIVE TIMING NUMBERS

C-17p There are four SPECIAL COMMANDS (MULTIPLY, DIVIDE, SHIFT, & NORMALIZE) in which the T number is to be interpreted as a RELATIVE TIMING NUMBER rather than a reference to a particular word time. (i.e., T specifies how many word times TRANSFER should last.) These commands may be defined in terms of the following signals originating in the CONTROL SWITCH: D7·DX·S6. In these cases, when the command is read, all terms entering the COMMAND REGISTER follow the regular pattern except that the NUMBER TRACK (CN) T22-T28 contents do not reach the ADDEND term - neither during READ COMMAND nor during WT 107. The reason for this is that the T number is a relative value in the first place and it is not necessary to obtain the difference between the two absolute values of T and L to produce a relative indication of time as in the general case.

C-17q The NUMBER TRACK (CN) information is prevented from entering the ADDEND term of the CM in the RELATIVE TIMING NUMBER case by resetting the CT flip-flop (Dwg. 22) by D7·DX·S6·T21·(CL+CK) at T21 time instead of T28--provided the computer is not in the WAIT TO READ COMMAND state. This prevents CN from becoming ADDEND to affect the T number computation which takes place during pulse periods T22 - T28 of each word time. For the benefit of the typewriter MARK and RETURN features discussed in section E-9, CL+CK (=$\overline{CL \cdot CK}$) prevents the special CT_r during the WAIT TO READ COMMAND state. This preserves the "WORD 107" signal.

C-17r Processing of the N number in the COMMAND REGISTER is analogous to that of the T number. The N number is located in the T14 - T20 pulse periods of the word in the COMMAND REGISTER. Inversion of N to supply the AUGEND takes place by virtue of the same circuit which supplies inverted T. NUMBER TRACK information is supplied as the ADDEND during READ COMMAND and WT 107 (WT+1 and "CORRECTIVE 20") in the same manner as it is in dealing with the T number except that the NUMBER TRACK information for N takes place during pulse periods T14 - T20. A "1" is added to the lowest order place of the AUGEND by unconditionally turning the CC flip-flop on by the set term T13. An END CARRY resulting from the arithmetic, signifying the proximity of WT = N, takes place at T21 time instead of T29. The signal that is used to initiate the advancement of the computer to the READ COMMAND state is T21·CC. This will occur at T21·(N-1).

C-17s The arithmetic operations affecting the T number and N number are isolated from one another by pulse period T21. During this pulse period CC is unconditionally set by T21 (reset is prevented by $\overline{T21}$ -- among other terms), therefore, no end carry from N, or absence thereof, can have any influence upon the T number arithmetic. Drawing 33 illustrates the arithmetic in the COMMAND REGISTER that will take place in accordance with a series of three commands.

C-17t In conclusion, the COMMAND REGISTER serves the purpose of generating END CARRIES as a function of the DYNAMIC PORTION of any command, but subject to some control by the STATIC PORTION. These END CARRIES may be defined as T29·CC and T21·CC. T29·CC will occur during WT = T-1 or L+T depending upon whether the T number is interpreted as being ABSOLUTE or RELATIVE. T29·CC, in conjunction with other terms, will either initiate TRANSFER or terminate it depending on whether the command is IMMEDIATE or DEFERRED. The T21·CC will unconditionally occur during WT = N-1 and will serve to initiate the READ COMMAND state (at T29 time) providing conditions permit it. (Other aspects of the COMMAND REGISTER will be discussed in section D-6e-1.)

RC - WTR - TR - WRC CONTROL

C-18a Ref. Drawing 30: The four major states of the computer are designated by the states of three flip-flops, CL, CK, and CQ, as follows:

RC	$\overline{CL}\cdot CK\cdot\overline{CQ}$
WTR	$CL\cdot\underline{CK}$
TR	$\underline{CL}\cdot\underline{CK}$
WRC	$CL\cdot CK$

C-18b The CQ term can inhibit the RC state and in so doing creates another minor state, READ COMMAND NEXT WT. This state can only arise in the event of a TEST command (Ref. Sec. C-19). Assume CQ will always be in the reset state for the sake of the discussion to follow.

C-18c This discussion will involve starting in the READ COMMAND state and advancing through the other states. Assuming that CL·CK·CQ (i.e., RC) is established by a T29 pulse, the following T29 will set CL (CL_s= RC·T29). This unconditionally terminates RC after one word time. The state to follow is a function of CK.

C-18d Had the command been an IMMEDIATE command, its T29 bit would = 0. This renders the term $\overline{CI}$ (inverted COMMAND INFORMATION) high at T29 of READ COMMAND (Dwg. 22) giving rise to T29·RC·CI, which resets CK. Control of CK at T29 of RC is a function of the I/D bit. At this point CL and CK can assume one of the following configurations:

$CL\cdot\underline{CK}$	WAIT TO TRANSFER (if I/D bit =1)
$CL\cdot CK$	TRANSFER (if I/D =0)

C-18e In the event that TR was not initiated at T29·RC, the T29·CC END CARRY signal from the COMMAND REGISTER will initiate it (by resetting CK) at T29 of WT = T-1. Since an unwanted T29·CC could have existed at T29·RC (Ref. Sec. C-17n), a means must be provided to prevent it from prematurely initiating TR. CL·CK defines the WTR state (which does not include RC), hence T29·CC·CL·CK is a satisfactory reset term for CK in the DEFERRED command case. This accounts for the programming restriction that any DEFERRED command will involve at least one word time in WTR, hence if T = L+1, 108 word times will be spent in the WTR state.

C-18f TERMINATION OF TR: This is accomplished by resetting CL. The manner in which this is done depends upon the command--the desired results are shown on Drawing 19.

C-18g IMMEDIATE commands: T29·CC·TR normally terminates TR. This takes place as a result of the arithmetic in CM : T29·(T-1) for ABSOLUTE timing numbers, T29·(L+T) for RELATIVE. Other terms can also terminate TR for certain special commands:

DS·S6·SX·PM·	--NORMALIZE	(Ref. Sec. D-13c)
DS·S6·SW·T29·$\overline{CE}$·AC_S	--SHIFT	(Ref. Sec. D-12e)
DS·S5·SV·T29	--MARK EXIT	(Ref. Sec. D-6f)

DEFERRED COMMANDS

C-18h SINGLE PRECISION: T29·TR·$\overline{Cl}$·CM terminates TR. The T29·TR portion terminates TR after one word time, provided $\overline{Cl}$ (STATIC FF: S/D bit = 0, meaning SINGLE precision) is high and CM contains a "1" at the time. CM can qualify this gate only after a T29·CC (not generated during RC) has occurred, thus preventing the gate from prematurely terminating TR in IMMEDIATE command cases. (Ref. Secs. C-17j and C-17n.)

C-18i DOUBLE PRECISION: T29·$\overline{CE}$·TR·CM terminates TR at the end of the first ODD word time after it is initiated. The purpose of the CM term is the same as in the SINGLE PRECISION case. T29·DS·S5·SV terminates TR in the MARK EXIT command case resulting in TR lasting only one word time regardless of the S/D bit (ref. Sec. D-6f).

C-18j Resetting of CL terminates TRANSFER; control of CK determines whether WRC or RC follows directly. If the TRANSFER terminating signal (TRr) occurs at T29·(N-1) time, it can, in all but the SHIFT and NORMALIZE cases, set CK avoiding the WRC state. Otherwise T29·(N-1) will set CK if WRC state is in effect, this state being identified by $\overline{CL\cdot CK}$.

C-18k The reader may recall that the COMMAND REGISTER "N" number END CARRY occurs at T21 time. T21·CC is not suitable for direct initiation of RC since it does not occur at T29 time; therefore, it is stored in flip-flop CJ, which qualifies gates probed either by TR_r or T29·$\overline{CK}$·$\overline{CL}$ ($\overline{CK}$·$\overline{CL}$ = WRC). CJ is normally reset by the next T13 pulse whether a T29 probing pulse sets CK or not. T21·CC will be available to control CJ on subsequent drum cycles during WT = N-1 if the first one was not used to initiate RC.

C-18l Note that T21·CC can set CJ only if the term CH·CZ·$\overline{CK}$ is high. CH and CZ are the terms which allow stopping and starting of the computer (Ref. Sec. C-20) $\overline{CK}$ prevents any unwanted T21·CC generated during RC from setting CJ. Other gates capable of setting CJ will be discussed in Section D-6.

C-18m Assuming that $\overline{CQ}$ has been high during the above discussion, as soon as CK was set, the configuration CL·CK·$\overline{CQ}$ is true and the RC state exists again, starting a new cycle.

C-18n Note that when RC starts, CJ is reset by the next T13 pulse (T13·CJ·$\overline{\mathrm{CQ}}$ + T13·CJ·TR); hence, CJ is high during the first 13 pulse periods of RC. Therefore, RC·CJ (T1 - T13) defines the STATIC portion of a command -- RC·CJ (T14 - T29) defines the DYNAMIC portion of a command.

THE "WRC NEXT WT" STATE (TEST COMMANDS)

C-19a When a TEST COMMAND is performed, an interrogation will take place during the TRANSFER state. As a result, CQ may or may not be set in accordance with the information being interrogated. If set, the set term will occur during TR.

C-19b When T29·(N-1) yields the $\overline{\mathrm{CL}}$·CK configuration, RC exists during WT = N, providing CQ is reset; if CQ is set, CL·CK·CQ exists, defining the RC NEXT WT state instead of RC. At the end of WT = N, T29·CL·CK resets CQ yielding the RC state. The RC state, then, has been postponed by one word time and takes place during WT = N+1. Reset of CJ, in this case is delayed by the absence of $\overline{\mathrm{CQ}}$ until T13 of RC to provide the desired RC·CJ and RC·$\overline{\mathrm{CJ}}$ signals.

C-19c The CJ reset gate, qualified by T13·CJ·TR, prevents RC from taking place during WT = T+1 (instead of WT = N+1) in case certain adverse time relationships exist between the setting of CQ and the word times specified by N and T.

C-19d The timing example of Drawing 31 should summarize state-to-state advancement activity.

COMPUTER START-STOP

C-20a Ref. Drawing 30 (upper left): CH and CZ permit the T21·CC signal to set CJ, hence initiate the READ COMMAND state, allowing execution of the next command. Should either CH or CZ be reset, the computer will idle in the WRC state until CH·CZ is restored. Control of these flip-flops can START and STOP the computer.

C-20b MANUAL CONTROL: The right hand switch on the typewriter base is known as the COMPUTE switch. It has two compute positions--GO and BP. If it is not in either of these positions it is in the center position, $\overline{\mathrm{GO}}$, and the computer will be stopped (in the WRC state).

C-20c With the switch on $\overline{\mathrm{GO}}$, the $\overline{\mathrm{CZ}}$.CH configuration will exist and RC cannot be initiated. If, the switch is thrown to GO or BP, CZ will be set at T0 time and the CZ·CH configuration will be established allowing RC to be initiated by T21·CC. T21·CC will occur at T21·(N-1), where N is usually a function of the last command read. (N = WT 0 can also be established by other means -Sec. E-8.)

C-20d If the switch is on GO, only a "HALT" command can stop the computer. If it is on BP, either a HALT command or a BP bit = 1 in a command can stop it. In any event, manually switching to the GO position will cause a stop.

C-20e HALT: If HALT command is programmed, during the time of TRANSFER the following signal will be high: DS·S4·SU. This will reset CH yielding $\overline{\text{CH}}$·CZ stopping the computer. To resume operation, the COMPUTE switch must be set to GO, establishing CH·$\overline{\text{CZ}}$, then back to GO or BP, establishing CH·CZ.

C-20f BREAK POINT: Should the COMPUTE switch be in the BP position and the BP bit of a command =1, T21·CI·RC·<BP> will become high, resetting CH. Note that this term can only become high if <BP> is present; BREAK POINTS are ignored if the COMPUTE switch is on GO. <BP> must qualify the CH_T gate prior to starting the computer so the first BP's in a program cannot be bypassed; for this reason, the <BP> contact of the COMPUTE switch must be grounded prior to the [<GO> + <BP>] contact.

C-20g "I" key operation: This provides a means of performing one command then stopping and is sometimes called the SINGLE CYCLE operation. See Section E-5.

C-20h NOTE: A neon is applied to the false side of CH to indicate the "HALT" state of the computer (neon panel is Drawing 17). On some D-SIZED prints, the stripe on the CH flip-flop's symbol may be found on the side opposite to that shown on Drawing 30. This introduces confusion, however, it does not change the circuit's theory of operation.

DESTINATION 27 - TEST (NON-ZERO)

C-21 Any SOURCE may feed DESTINATION 27. If during the time of TRANSFER one or more ONES appear on the LATE BUS, the test will be met, CQ will be set, and the next command will be read at WT = N+1 (instead of N). The term LB·D6·DX in this case will set CQ (ref. dwg. 30) causing a one word delay in the RC state.