Chapter 8

Diagnostic Tests – Models 71R/72R/73R

DIAGNOSTIC TESTS – MODELS 71R/72R/73R

PROCESSOR

TEST 1 – 80186 TRAP TEST

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the RAM memory, including the RAM supplied by the 512-Kbyte Memory PCB. A marching 1s test is used so that each bit position is tested. A 16-bit checksum is then computed over the 8K words of EPROM memory.

Error Code	Meaning
1	Memory test failed
2	EPROM checksum test failed
3	NMI detected during memory test
4	Feature configuration register not detected

TEST 3 – 80186 INTERNAL DMA TEST

The 80186 built-in DMA feature is verified by this test. A block of memory is moved via DMA, and the two blocks of memory are compared.

Error Code	Meaning
1	DMA transfer not done in time
2	DMA move compare failed
3	Same as 1, starting on odd boundary
4	Same as 2, starting on odd boundary

TEST 4 – TIMER TEST

This test verifies the operation of timer 2 of the 80186 processor. The test starts the timer, waits for a time-out, then verifies that an interrupt was generated and the proper trap was taken.

Error Code	Meaning
1	Timer 2 trap failed
2	Timer 2 Interrupt not cleared from ISR

TEST 5 – 8530 SCC LOOPBACK TEST

The 8530 SCC is configured in asynchronous loopback mode at 9600 baud to test the transmitter/receiver operation using single character I/O. Data values from 0 to 127 are used, with parity masked.

Error Code	Meaning
1	Character not received
2	Incorrect received character

TEST 6 – 8530 DMA LOOPBACK TEST

This test configures the 8530 SCC to operate in synchronous (SDLC) loopback mode and uses DMA for transfers. The DMA internal to the iAPX186 processor is used for receive access in the loopback test. Variable frame lengths are tested by first sending a 1-byte I-field, then a 2-byte field, etc. up to a 100-byte field. The bytes in each I-field are sent in a "counting" format starting with 1 (i.e., 01 will be sent, then 0102, then 010203 etc.). End of frame and CRC are also verified for each iteration.

Error Code	Meanings
1	CRC error detected in frame
2	Incorrect received character
3	DMA transfer (receive) not completed
4	End of frame never received

TEST 7 – 8530 SCC INTERRUPT TEST

The 8530 interrupt function to the 80186 processor is verified in this test. Transmit interrupts are enabled on the 8530 and a byte is written to the transmitter, causing simulation of the INT1 interrupt.

Error Code	Meaning
1	INT1 not generated (8530 SCC source)
2	Extra interrupt detected

TEST 8 – PORT OPTION PCB TEST

This test exercises either the Serial Port Option PCB or the Parallel Port Option PCB. The serial test exercises the 8530 SCC inherent to the Serial Port Option PCB. The serial test is identical to test 10, using the Serial Port Option PCB instead.

For the Serial Port Option PCB, an external loopback plug with the following connections is required:

DTR (pin 4) jumpered to DSR (pin 6)
RTS (pin 7) jumpered to CTS (pin 8)
RxD (pin 2) jumpered to TxD (pin 3)

The Parallel Port Option PCB test sets up the 8255 PPI with ports A, B, and C (on the chip) as outputs (control word 80H) and verifies that data can be written to and read back from each port.

NOTE: This test does not appear on the default test list (it is not selected with the '*' specifier), it must be manually selected. If two Port Option PCBs are installed, each is tested and verified by this test.

Error Code	Meaning
1	Character not received
2	Incorrect received character
4	DCD not detected
5	CTS not detected
6	8255 Port A (on the chip) value incorrect
7	8255 Port B (on the chip) value incorrect
8	8255 Port C (on the chip) value incorrect
10	Neither expansion board detected

NOTE: The remaining Processor Tests, tests 9, 10, 11, 12, and 13, can only be selected individually (not on default test list).

TEST 9 – COMPREHENSIVE MEMORY TEST

This test may take 10 to 20 minutes to complete, depending on the amount of memory installed. This is a more rigorous memory test than Test 2. A memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written, it is checked for its initial value. This will identify if a memory write alters any word other than the intended one. This is done in both a forward and backward direction. The test is then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The main purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory error

TEST 10 – 8530 SCC EXTERNAL LOOPBACK TEST

This test is similar to the internal loopback test, but requires an external connection to Port A for the loopback. This test also verifies the RTS, CTS, and DCD signals.

NOTE: This test requires an external loopback connector wired as shown next.

71R (RS 232C):
Pin 6 jumpered to Pins 8 and 20
Pin 4 jumpered to Pin 5
Pin 3 jumpered to Pin 2

71R (V.35):
Pin 6 jumpered to Pins 8 and 20
Pin 14 jumpered to Pin 7
Pin 10 jumpered to Pin 12
Pin 13 jumpered to Pin 9
Pin 4 jumpered to pin 5

72R (X.21):
Pin 2 jumpered to Pin 4
Pin 9 jumpered to Pin 11
Pin 3 jumpered to Pin 5
Pin 10 jumpered to Pin 12

Error Code	Meaning
1	Character not received
2	Incorrect received character
4	DCD not detected
5	CTS not detected
6	RIA stuck on
7	RIA not detected
8	DSR stuck on
9	DSR not detected

TEST 11 – MAINTENANCE PORT (PORT B) LOOPBACK TEST

This test is similar to Test 5 but tests Port B instead.

NOTE: A coax type terminal must be used to run this test since Port B is the access port for ASCII terminals. Attempting to run this test from an ASCII terminal causes the following warn ing message to appear:

WARNING

PROC test 11 should be run from a coax type terminal!

Error Code	Meaning
1	Character not received
2	Incorrect received character

TEST 12 – COMPREHENSIVE PARALLEL PORT OPTION PCB TEST

This test is a more rigorous test of the Parallel Port Option PCB than test 8. The 8255 PPI is configured (control word A2H) so that all printer control lines can be exercised.

NOTE: A supported printer (either default or configured) must be attached.

Error Code	Meaning
4	Printer fault
5	INT3 not generated by output buffer empty
6	INT3 not cleared by a write to the output buffer

TEST 13 – DISK DRIVE TEST

This test exercises the diskette drive. The test first formats the diskette, verifying each sector during the formatting process. The test then verifies that it can successfully write and read the first track and the last track on the diskette.

NOTE: When selecting this test, a blank or scratch diskette should be installed in the diskette drive as this test destroys any data that may be contained on the diskette.

Error Code	Meaning
1	Seek error
2	Format error or disk not ready
3	Verify error while formatting
4	Cannot write track 79
5	Cannot write track 0
6	Cannot read track 79
7	Cannot read track 0
8	Data miscompare, track 79
9	Data miscompare, track 0
10	General disk failure
11	Recalibration failure after format

COAX CONTROLLER

TEST 1 – COAX LOOPBACK TEST

This test exercises the coax transmitter and receiver hardware. The hardware is tested in two internal loopback configurations.

Error Code	Meaning
1	Receiver error on Loopback Word 2: Port number (0-7)
2	Did not get Data Available Word 2: Port number (0-7)
3	Loopback data incorrect Word 2: Port number (0-7)
14	Coax receiver parity bit D10 invalid
15	Coax receiver bit D11 invalid Word 2: Port number (0-8)

TEST 2 – DMA TRANSFER TEST

This test checks the basic DMA mechanism by setting up the DMA request/acknowledge sequence in the Coax Controller PCB. A word of data (55AAH) is also looped back using the transmit leg of the DMA to more extensively exercise the related hardware.

Error Code	Meaning
4	Transmitter did not go active
5	DMA transfer not completed
6	Receiver error on Loopback
7	Did not receive data available
8	Loopback data incorrect (DMA Transmit)
9	Loopback data incorrect (DMA Receive)
10	INT2 not generated by end of DMA

TOKEN-RING (73R)

NOTE: The cable between the control unit and the Token Ring must be disconnected from the concentrator and must be left connected to the Token-Ring Adapter prior to running any Token Ring diagnostic tests. The following message appears when any token ring tests are selected:

WARNING

Be sure that the Token Ring board lobe media cable has been removed from the wiring concentrator before continuing with the diagnostics! Hit any key when ready.

TEST 1 – BRING-UP DIAGNOSTIC TEST

This test checks a status byte generated at power-up time that indicates the initial state of the Token-Ring chip-set. The Token-Ring chip-set goes through four phases at power-up time:

1 Bring-up diagnostics
2 Chip-set initialization and expansion memory verification using the Open command
3 Adapter Debug Software (ADS) download to the Token-Ring expansion memory
4 ADS stage 1 Lan Adapter bus verification

The bring-up diagnostic performs the following tests on the Token-Ring chip-set:

1 Test of the TMS38020 ROM
2 Instruction and interrupt test of the TMS38010
3 Transmit wrap test through the ring interface (loopback)
4 Register access test of the TMS 38030

The ADS Stage 1 diagnostic exercises the Token-Ring chip-set by going through five verification phases:

1 Reset Verification – verifies that the TMS38030 Communications Processor and on-chip oscillator are functional and that basic access to the ADS EPROM is successful
2 EPROM checksum verification – verifies that the ADS EPROMs and the LAN Adapter bus interface to the ADS EPROMs is fully functional
3 TMS38010 RAM verification – verifies that the RAM contained in the TMS38010 Communications Processor is fully functional
4 TMS38020 Protocol Handler register verification – verifies that the TMS38010 Communications Processor can read and write selected registers of the TMS38020 Protocol Handler
5 TMS38030 System Interface register verification – verifies that the TMS38010 can read and write selected registers of the TMS38030 System Interface

Error Code	Meaning
1	Bring-up diagnostics (BUD) failed (Chip-set failure)
2	Bring-up diagnostics hung
3	Token-Ring Adapter will not initialize
4	Token-Ring Adapter will not open
5	Failure detected during Token Ring Open
6	Token-Ring will not enter download state
7	Data miscompare in code download verification
8	ADS Stage 1 bus verification failure
9	Burned in address invalid (EPROM)
10	Could not read burned-in address

TEST 2 – DIRECT I/O INTERFACE TESTS

This test exercises the direct I/O interface to the chip-set by verifying that bits 0-6 (where 0 is the LSB) in the most significant byte of the interrupt register can be set by the processor, and by writing and comparing bit patterns 5555H and AAAAH to each of the internal Adapter RAM locations (0580H to 07FEH).

Error Code	Meaning
1	Invalid read of the TMS38030 interrupt register
2	Invalid read of the TMS38030 internal RAM
10	ADS software was not downloaded

TEST 3 – ADS STAGE 2 DMA TEST

This test verifies the proper operation of the chip set DMA using commands inherent to the ADS EPROMs. The following Stage 2 commands are used to exercise the DMA:

1 Clear DMA RAM
2 Fill DMA RAM
3 Test DMA to chip-set
4 Test DMA from chip-set

After verifying the Clear and Fill functions of the chip-set DMA, the test exercises the chip-set DMA by transferring the contents of the 73R on-board memory (location 200000H to DFFFH) to the chip-set RAM (beginning at location 1000H) 4000H bytes at a time, verifying the transfer each time by DMAing the 4000H bytes of data back to the 73R memory at location DC000H for verification. If DIB memory is present, it is also tested (from 100000H to 180000H).

Error Code	Meaning
1	Clear DMA RAM test failed
2	Fill DMA RAM test failed
7	DMA to chip-set failure
8	DMA from chip-set failure
9	DMA verification failure
10	ADS software was not downloaded

TEST 4 – ADS STAGE 2 MISCELLANEOUS TESTS

This test uses commands inherent to the ADS EPROMs to exercise various miscellaneous parts of the chip-set. The following Stage 2 commands are used:

1 Set Interrupt Active
2 Test Expansion Memory (1000H-3FFEH, 8000H-FFFEH)
3 Test Wrap Function (loopback)

Error Code	Meaning
1	Could not activate chip-set interrupt
2	Interrupt not received from chip-set
3	Expansion memory test failed
4	Wrap function test failed
10	ADS Software was not downloaded

TEST 5 – ADS STAGE 2 EXTERNAL TESTS

This test runs diagnostics that require an external lobe media cable equipped with a self-shorting connector. These tests are comprised of a test of the watch dog time function implemented by the 74LS122 located between the TMS38020 and the ring interface, and a loopback test that causes frames to circulate on the lobe media cable.

Error Code	Meaning
1	Lobe function test failed (external loopback)
2	Watchdog timer test failed
10	ADS Software was not downloaded

NOTE: Test 6 is not selected with the * specifier. It must be individually selected.

TEST 6 – INSERT FUNCTION TEST

This test activates the phantom drive of the ring interface to insert the PCB into a ring. The PCB must be connected to an external wiring concentrator through a lobe media cable.

Error Code	Meaning
1	Insert function test failed
10	ADS Software was not downloaded