Chapter 7

Diagnostic Tests – Model 61R

DIAGNOSTIC TESTS – MODEL 61R

PROCESSOR

TEST 1 – 80186 TRAP TEST

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the RAM memory, including the 512-Kbyte Memory Expansion PCB (if installed). A marching 1s test is used so that each bit position is tested. A 16-bit checksum is then computed over the 8K words of EPROM memory.

Error Code	Meaning
1	Memory test failed
2	EPROM checksum test failed
3	NMI detected during memory test
4	Feature configuration register not detected
6	Could not force parity error on even byte
7	Could not force parity error on odd byte

TEST 3 – 80186 INTERNAL DMA TEST

This test verifies the 80186 built-in DMA feature. A memory block is moved via DMA, and the two blocks of memory are compared.

Error Code	Meaning
1	DMA transfer not done in time
2	DMA move compare failed
3	Same as 1, starting on odd boundary
4	Same as 2, starting on odd boundary
5	Mapping RAM location '6' verification failure
6	Mapping RAM location 'F' verification failure

TEST 4 – TIMER TEST

This test verifies the operation of timer 2 of the 80186 processor. The test starts the timer, waits for a time-out, then verifies that an interrupt was generated and the proper trap was taken.

Error Code	Meaning
1	Timer 2 trap failed
2	Timer 2 Interrupt not cleared from ISR

TEST 5 – 8530 SCC LOOPBACK TEST

The 8530 SCC is configured in asynchronous loopback mode at 9600 baud to test the transmitter/receiver operation using single character I/O. Data values 0 to 127 are used, with parity masked.

Error Code	Meaning
1	Character not received
2	Incorrect received character

TEST 6 – 8530 DMA LOOPBACK TEST

This test configures the 8530 SCC to operate in synchronous (SDLC) loopback mode and uses DMA for transfers. The DMA internal to the iAPX186 processor is used for receive access in the loopback test. Variable frame lengths are tested by first sending a 1-byte I-field, then a 2-byte field, etc. up to a 100-byte field. The bytes in each I-field are sent in a counting format starting with 1 (i.e., 01 will be sent, then 0102, then 010203 etc.). End of frame and CRC are also verified for each iteration.

Error Code	Meaning
1	CRC error detected in frame
2	Incorrect received character
3	DMA transfer (receive) not completed
4	End of frame never received

TEST 7 – 8530 SCC INTERRUPT TEST

The 8530 interrupt function to the 80186 processor is verified in this test. Transmit interrupts are enabled on the 8530 and a byte is written to the transmitter, causing simulation of the INT1 interrupt.

Error Code	Meaning
1	INT1 not generated (8530 SCC source)
2	Extra interrupt detected

TEST 8 – PORT OPTION PCB TEST

This test exercises either the Serial Port Option PCB or the Parallel Port Option PCB. The serial test exercises the 8530 SCC inherent to the Serial Port Option PCB. The serial test is identical to test 10, using the Serial Port Option PCB instead.

For the Serial Port Option PCB, an external loopback plug with the following connections is required:

DTR (pin 4) jumpered to DSR (pin 6)
RTS (pin 7) jumpered to CTS (pin 8)
RxD (pin 2) jumpered to TxD (pin 3)

The Parallel Port Option PCB test sets up the 8255 PPI chip with ports A, B, and C on the chip as outputs (control word 80H) and verifies that data can be written to and read back from each port.

NOTE: This test does not appear on the default test list (it is not selected with the '*' specifier), it must be manually selected. If two Port Option PCBs are installed, each is tested and verified by this test. Error codes 1 through 5 apply to the serial interface PCB, 6 through 8 to the parallel interface PCB.

Error Code	Meaning
1	Character not received Byte 1: Expansion slot # (2 or 3)
2	Incorrect received character Byte 1: Expansion slot # (2 or 3)
4	DCD not detected Byte 1: Expansion slot # (2 or 3)
5	CTS not detected Byte 1: Expansion slot # (2 or 3)
6	8255 Port A (on the chip) value incorrect
7	8255 Port B (on the chip) value incorrect
8	8255 Port C (on the chip) value incorrect
10	Neither expansion board detected

NOTE: The remaining Processor Tests, tests 9, 10, 11, 12, and 13, can only Continuedbe selected individually (not on default test list).

TEST 9 – COMPREHENSIVE MEMORY TEST

This test may take 10 to 20 minutes to complete, depending on the amount of memory installed. This is a more rigorous memory test than Test 2. A memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written, it is checked for its initial value. This will identify if a memory write alters any word other than the intended one. This is done in both a forward and backward direction. The test is then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The main purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory error

TEST 10 – 8530 SCC EXTERNAL LOOPBACK TEST

This test is similar to the internal loopback test, but requires an external connection to Host 1 for the loopback. This test also verifies the RTS, CTS, and DCD signals.

NOTE: This test requires an external loopback connector wired as shown next.

RS 232C:
Pin 6 jumpered to Pins 8 and 20
Pin 4 jumpered to Pin 5
Pin 3 jumpered to Pin 2

V.35:
Pin 6 jumpered to Pins 8 and 20
Pin 14 jumpered to Pin 7
Pin 10 jumpered to Pin 12
Pin 13 jumpered to Pin 9
Pin 4 jumpered to pin 5

Error Code	Meaning
1	Character not received
2	Incorrect received character
4	DCD not detected
5	CTS not detected
6	RIA stuck on
7	RIA not detected
8	DSR stuck on
9	DSR not detected

TEST 11 – MAINTENANCE PORT LOOPBACK TEST

This test is similar to Test 5 but tests the maintenance port.

NOTE: A coax type terminal must be used to run this test since the Maint Port is the access port for ASCII terminals. Attempting to run this test from an ASCII terminal causes the following warning message to appear:

WARNING

PROC test 11 should be run from a coax type terminal!

Error Code	Meaning
1	Character not received
2	Incorrect received character

TEST 12 – COMPREHENSIVE PARALLEL PORT OPTION PCB TEST

This test is a more rigorous test of the Parallel Port Option PCB than test 8. The 8255 PPI is configured (control word A2H) so that all printer control lines can be exercised.

NOTE: A supported printer (either default or configured) must be attached.

Error Code	Meaning
4	Printer fault
5	INT3 not generated by output buffer empty
6	INT3 not cleared by a write to the output buffer

TEST 13 – DISK DRIVE TEST

This test exercises the diskette drive. The test first formats the diskette, verifying each sector during the formatting process. The test then verifies that it can successfully write and read the first track and the last track on the diskette.

NOTE: When selecting this test, a blank or scratch diskette should be installed in the diskette drive as this test destroys any data that may be contained on the diskette.

Error Code	Meaning
1	Seek error
2	Format error or disk not ready
3	Verify error while formatting
4	Cannot write track 79
5	Cannot write track 0
6	Cannot read track 79
7	Cannot read track 0
8	Data miscompare, track 79
9	Data miscompare, track 0
10	General disk failure
11	Recalibration failure after format

COAX CONTROLLER

TEST 1 – COAX LOOPBACK TEST

This test exercises the coax transmitter and receiver hardware. The hardware is tested in two internal loopback configurations.

Error Code	Meaning
1	Receiver error on Loopback Byte 4: Port number (0-8)
2	Did not get Data Available Byte 4: Port number (0-8)
3	Loopback data incorrect Byte 4: Port number (0-8)
14	Coax receiver parity bit D10 invalid
15	Coax receiver bit D11 invalid Byte 4: port number (0-8)

TEST 2 – DMA TRANSFER TEST

This test checks the basic DMA mechanism by setting up the DMA request/acknowledge sequence in the Coax Controller PCB. A word of data (55AAH) is also looped back using the transmit leg of the DMA to more extensively exercise the related hardware. To test using both states of the Frequency Select B bit, this test is run twice.

Error Code	Meaning
4	Transmitter did not go active
5	DMA transfer not completed
6	Receiver error on Loopback
7	Did not receive data available
8	Loopback data incorrect (DMA Transmit)
9	Loopback data incorrect (DMA Receive)
10	INT2 not generated by end of DMA

HOST SERIAL EXPANSION

TEST 1 – 8530 SCC INTERNAL LOOPBACK TEST

The 8530 SCC is configured in asynchronous loopback mode at 9600 baud to test the transmitter/receiver operation using single-character I/O. Data values 0 to 127 are used, with parity masked.

Error Code	Meaning
1	Character not received
2	Incorrect received character

TEST 2 – 8530 DMA LOOPBACK TEST

This test configures the 8530 SCC to operate in synchronous (SDLC) loopback mode and uses DMA for transfers. The DMA internal to the iAPX186 processor is used for receive access in the loopback test. Variable frame lengths are tested by first sending a 1-byte I-field, then a 2-byte field, etc. up to a 100-byte field. The bytes in each I-field are sent in a "counting" format starting with 1 (i.e., 01 will be sent, then 0102, then 010203 etc.). End of frame and CRC are also verified for each iteration.

Error Code	Meaning
1	CRC error detected in frame
2	Incorrect received character
3	DMA transfer (receive) not completed
4	End of frame never received

TEST 3 – 8530 SCC INTERRUPT TEST

This test simulates an interrupt from the 8530 and verifies that the interrupt is received at the 80186 internal interrupt controller.

Error Code	Meaning
1	Interrupt not received at PCB PIC
2	Interrupt cannot be cleared

TEST 4 – 8530 SCC EXTERNAL LOOPBACK TEST

This test is similar to the internal loopback test, but requires an external connection to each port for the loopback. This test also verifies the RTS, CTS, and DCD signals.

NOTE: This test does not appear on the default test list (it is not selected with the '*' specifier), it must be manually selected.

This test requires an external loopback connector, as shown next.

RS 232C:
Pin 6 jumpered to Pins 8 and 20
Pin 4 jumpered to Pin 5
Pin 3 jumpered to Pin 2

V.35:
Pin 6 jumpered to Pins 8 and 20
Pin 14 jumpered to Pin 7
Pin 10 jumpered to Pin 12
Pin 13 jumpered to Pin 9
Pin 4 jumpered to pin 5

Error Code	Meaning
1	Character not received
2	Incorrect received character
3	DCD and/or DSR not detected in serial port status register
4	DCD not detected
5	CTS not detected