Chapter 6

Diagnostic Tests – Models 51R/52R/53R

DIAGNOSTIC TESTS – MODELS 51R/52R/53R

PROCESSOR

TEST 1 – 80186 TRAP TEST

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the 1.5-Mbyte local DRAM memory and the RAM (.5 to 4 Mbytes) supplied by the Memory Expansion PCB. The alternating word pattern 55AA AA55 is written to memory and verified. Then, the one's complement (AA55 55AA) is written and verified. This tests also verifies the parity generating circuitry by forcing bad parity on even and odd memory accesses and confirming that the proper response (NMI) is received.

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read
3	Memory error, byte write, word read
4	Memory error, byte write, byte read
5	NMI detected during memory test
6	Could not force parity error on even byte
7	Could not force parity error on odd byte

TEST 3 – 80186 INTERNAL DMA TEST

The 80186 built-in DMA feature is verified by this test. A block of memory is moved via DMA, and the two blocks of memory are compared.

Error Code	Meaning
1	DMA transfer not done in time
2	DMA move compare failed
3	Same as 1, starting on odd boundary
4	Same as 2, starting on odd boundary

TEST 4 – SYSTEM BUS TEST

This test checks access to shared on the option module if the option module is a smart processor (Asynchronous Adapter PCB or Token-Ring Adapter PCB). The entire 512 Kbytes of memory (except for the first 64 Kbytes, which are reserved for the option PCB and the last 4 Kbytes, which are reserved for the mailboxes) on remote processor is tested. Before testing on of the eight 64-Kbyte segments, the processor locks out the segment from access by the option PCB processor to prevent a bus conflict. This allows one processor to test one segment while the other processor tests another segment. In addition, the bus arbitration circuitry is verified by this test.

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read
3	Memory error, byte write, word read
4	Memory error, byte write, byte read
5	NMI detected during memory test
9	Could not gain access to system memory

TEST 5 – HARDWARE REGISTER TEST

This test verifies Mapping RAM and the FF register. Mapping RAM page registers 0-3 are verified by writing and comparing the patterns 0 through 7F for page registers 0-1 (bit 7 does not exist in these registers), and the patterns 0 through 7FF for page registers 2-3. A rotating 1s pattern is then tested on the page registers. The NMI bit in the FF register is verified by setting and resetting the bit and verifying it. The NMI interrupt is then verified at the processor.

Error Code	Meaning
1	Invalid read of Mapping RAM
2	Could not set NMI bit in FF register
3	Could not clear NMI bit in FF register
4	NMI interrupt not received at processor

TEST 6 – HOST SERIAL INTERFACE 8530 SCC INTERNAL LOOPBACK TEST

The 8530 SCC for the host port (HOST1) on the processor PCB is configured in asynchronous loopback mode at 19200 baud to test the transmitter/receiver operation using single character I/O. Data values from 0 to 127 are used, with parity masked. If a Host Serial Interface Extender (HSIE) PCB is installed, this test is repeated for the 8530 SCC on the HSIE (HOST2).

Error Code	Meaning
1	Character not received Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2
2	Incorrect received character Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2

TEST 7 – HOST SERIAL INTERFACE 8530 DMA LOOPBACK TEST

This test configures the 8530 SCC for the host port on the processor PCB to operate in synchronous (SDLC) loopback mode and uses DMA for transfers. The DMA internal to the iAPX186 processor is used for receive access in the loopback test.

Error Code	Meanings
1	CRC error detected in frame
2	Incorrect received character
3	DMA transfer (receive) not completed
4	End of frame never received

TEST 8 – 8530 SCC INTERRUPT TEST

The 8530 interrupt function to the 80186 processor is verified in this test. Transmit interrupts are enabled on the 8530 and a byte is written to the transmitter, causing simulation of the INT1 interrupt. If a Host Serial Interface Extender (HSIE) PCB is installed, this test is repeated for 8530 on the HSIE (HOST2). This test also checks for any stray interrupts on INT0, INT2, and INT3.

Error Code	Meaning
1	Interrupt not received at PCB PIC Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2
2	Interrupt cannot be cleared Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2
3	Stray interrupt detected

TEST 9 – HOST SERIAL INTERFACE 8530 SCC EXTERNAL LOOPBACK TEST

This test exercises the Host Serial Interface on the processor PCB. For this test, an external loopback plug with the following connections is required:

51R (RS 232C):
Pin 6 jumpered to Pins 8 and 20
Pin 4 jumpered to Pin 5
Pin 3 jumpered to Pin 2

51R (V.35):
Pin 6 jumpered to Pins 8 and 20
Pin 14 jumpered to Pin 7
Pin 10 jumpered to Pin 12
Pin 13 jumpered to Pin 9
Pin 4 jumpered to pin 5

52R (X.21):
Pin 2 jumpered to Pin 4
Pin 9 jumpered to Pin 11
Pin 3 jumpered to Pin 5
Pin 10 jumpered to Pin 12

Error Code	Meaning
1	Character not received Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2
2	Incorrect received character Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2
4	DCD not detected Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2
5	CTS not detected Word 3: Port that failed 0X0A = HOST1 0X0B = HOST2

NOTE: The remaining tests, tests 10, 11, 12, and 13, can only be selected individually (not on default test list).

TEST 10 – COMPREHENSIVE MEMORY TEST

This test make take 10 to 20 minutes to complete, depending on the amount of memory installed. This is a more rigorous memory test than Test 2. A memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written, it is checked for its initial value. This will identify if a memory write alters any word other than the intended one. This is done in both a forward and backward direction. The test is then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The main purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory error

TEST 11 – MAINTENANCE PORT LOOPBACK TEST

This test is similar to Test 6 but tests the Maintenance Port. The port is configured in loopback mode at 19,200 baud to test the transmitter/receiver operation using single character I/O. Data values from 0 to 127 are used, with parity masked.

NOTE: A coax type terminal must be used to run this test since the Maintenance Port is the access port for ASCII terminals.

Error Code	Meaning
1	Character not received
2	Incorrect received character

TEST 12 – LOCK TEST

NOTE: This test cannot be run in conjunction with any other diagnostic tests. Failure to observe this precaution may cause the control unit to enter a state from which it cannot be recovered except by re-IMLing the system.

This test verifies the proper operation of the Lock signal between the main processor and the PCB plugged into the option slot. The processor tests its Lock operation by incrementing a specific 16-bit word in shared memory while the option slot processor decrements the same word. A failure occurs when both processors complete and the word count is not zero. A count less than zero indicates the main processor is failing. A count greater than zero indicates the option slot processor is failing.

Error Code	Meaning
3	Lock failure in IOCs shared memory
5	Could not communicate with remote board

TEST 13 – DISK DRIVE TEST

This test exercises the diskette drive. The test first formats the diskette, verifying each sector during the formatting process. The test then verifies that it can successfully write and read the first track and the last track on the diskette.

NOTE: When selecting this test, a blank or scratch diskette should be installed in the diskette drive as this test destroys any data that may be contained on the diskette.

Error Code	Meaning
1	Seek error
2	Format error or disk not ready
3	Verify error while formatting
4	Cannot write track 79
5	Cannot write track 0
6	Cannot read track 79
7	Cannot read track 0
8	Data miscompare, track 79
9	Data miscompare, track 0
10	General Disk Failure (miscompare)
11	Recalibration failure after format

COAX CONTROLLER

TEST 1 – DUAL ACCESS MEMORY TEST

The Coax DAM segment F000H, from offset 1000H through 1FFFH is tested. The pattern 55AAH is written to the block and verified, then the pattern AA55H is written and verified with word write and word read operations. Byte write and byte read operations are then used to write and verify three patterns: LSB of the address offset, 55H, and AAH.

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read

TEST 2 – DAM BUS ARBITRATION

Bus arbitration and DAM are tested when test 1 is invoked concurrently with an 8344 test of DAM. The 8344 writes and verifies the compliment of the LSB of each address from 0F00H through 0FFFH. The 8344 repeats its test 240 times.

Error Code	Meaning
1	80186 memory error: word write, word read
2	80186 memory error: byte write, byte read
3	8344 memory error
8	Time-out – no response from 8344
9	Time-out – 8344 did not return from routine

TEST 3 – INTERNAL LOOPBACK TEST

A data frame is sent and verified, then a command frame is sent and verified. The test data is then changed from 55H to AAh and the test is repeated.

Error Code	Meaning
1	8344 Receiver error
2	Data Available flag not set
3	D11 error
4	Data byte incorrect
5	TT/AR not valid
6	Parity error (D10)
8	Time-out – no response from 8344
9	Time-out – 8344 did not return from routine
10	Transmit FIFO flag failure
11	Receive FIFO flag failure
12	Register failure
13	Stack failure

NOTE: Tests 4 and 5 cannot be selected with the * specifier. They must be individually selected.

All coax devices except the device used for monitoring the diagnostics should be removed before executing Test 4.

TEST 4 – EXTERNAL LOOPBACK TEST

A data frame is sent and verified, then a command frame is sent and verified. The test data is then changed from 55H to AAH and the test is repeated. A new port is selected and the test is repeated until all of the ports have been tested.

Error Code	Meaning
1	8344 Receiver error Byte 1: Port number
2	Data Available flag not set Byte 1: Port number
3	D11 error Byte 1: Port number
4	Data byte incorrect Byte 1: Port number
5	TT/AR not valid
6	Parity error (D10)
8	Time-out – no response from 8344
9	Time-out – 8344 did not return from routine

TEST 5 – 8344 INSTRUCTION MEMORY AND PROGRAM COUNTER TEST

This test is not intended for use with a coax terminal. The 8344 program counter is tested by writing and verifying 55H and AAH to both the low byte and high byte of the program counter. The instruction memory is tested by writing at each byte the LSB of the address of that byte and verifying. The patterns AAH, 55H, AAH, ... and 55H, AAH, 55H, ... are then written and verified. Finally, the 8344 code is downloaded and verified.

Error Code	Meaning
1	8344 program counter low byte error
2	8344 program counter high byte error
3	Instruction memory error
4	Download error

TOKEN-RING ADAPTER

TEST 1 – 80186 TRAP TEST

NOTE: The cable between the control unit and the Token Ring must be disconnected prior to running the Token-Ring Gateway diagnostic tests. This cable must be disconnected at the Token-Ring and remain connected to the control unit. The diagnostic tests may have adverse effects on the Token Ring if the control unit is attached.

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the 512-Kbyte DRAM memory and the additional 512 Kbytes of option memory, if present. The alternating word pattern 55AA AA55 is written to memory and verified, then a 1s complement pattern AA55 55AA is written and verified. The PROC PCB also verifies this memory from its side. The TRA processor must gain access to each 64-Kbyte segment by setting a bit in memory (called a semaphore) to signal the PROC to not attempt a memory access until the TRA processor has cleared the semaphore. There are eight semaphores for each of the eight 64-Kbyte memory segments. This test also verifies the parity generating circuitry by forcing bad parity on even and odd memory accesses and confirming that the proper response (NMI) is received.

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read
3	Memory error, byte write, word read
4	Memory error, byte write, byte read
5	NMI detected during memory test
6	Could not force parity error on even byte
7	Could not force parity error on odd byte

TEST 3 – 80186 INTERNAL DMA TEST

The 80186 built-in DMA feature is verified by this test. A block of memory is moved via DMA, and the two blocks of memory are compared.

Error Code	Meaning
1	DMA transfer not done in time
2	DMA move compare failed
3	Same as 1, starting on odd boundary
4	Same as 2, starting on odd boundary

TEST 4 – IPI TEST

This test verifies that the IPI bit in the FF register can be set and cleared directly, then verifies that INT3 was received. This test also checks for stray interrupts on INT0-INT2.

Error Code	Meaning
1	Cannot clear IPI bit in FF register
2	Cannot set IPI bit in FF register
3	INT3 not generated
4	INT0 also generated
5	INT1 also generated
6	INT2 also generated

TEST 5 – BRING-UP DIAGNOSTIC TEST

This test checks a status byte generated at power-up time that indicates the initial state of the Token-Ring chip-set. The Token-Ring chip-set goes through four phases at power-up time:

1 Bring-up diagnostics
2 Chip-set initialization and expansion memory verification using the Open command
3 Adapter Debug Software (ADS) download to the Token-Ring expansion memory
4 ADS stage 1 Lan Adapter bus verification

The bring-up diagnostic performs the following tests on the Token-Ring chip-set:

1 Test of the TMS38020 ROM
2 Instruction and interrupt test of the TMS38010
3 Transmit wrap test through the ring interface (loopback)
4 Register access test of the TMS 38030

The ADS Stage 1 diagnostic exercises the Token-Ring chip-set by going through five verification phases:

1 Reset Verification – verifies that the TMS38030 Communications Processor and on-chip oscillator are functional and that basic access to the ADS EPROM is successful
2 EPROM checksum verification – verifies that the ADS EPROMs and the LAN Adapter bus interface to the ADS EPROMs is fully functional
3 TMS38010 RAM verification – verifies that the RAM contained in the TMS38010 Communications Processor is fully functional
4 TMS38020 Protocol Handler register verification – verifies that the TMS38010 Communications Processor can read and write selected registers of the TMS38020 Protocol Handler
5 TMS38030 System Interface register verification – verifies that the TMS38010 can read and write selected registers of the TMS38030 System Interface

Error Code	Meaning
1	Bring-up diagnostics (BUD) failed (Token-Ring chip-set failure)
2	Bring-up diagnostics hung
3	Token-Ring Adapter will not initialize
4	Token-Ring Adapter will not Open
5	Failure detected during Token Ring Open
6	Token Ring won't enter download state
7	Data miscompare in code download verification
8	ADS Stage 1 bus verification failure
9	Burned in address invalid (EPROM)
10	Could not read burned-in address

TEST 6 – DIRECT I/O INTERFACE TESTS

This test exercises the direct I/O interface to the chip-set by verifying that bits 0-6 (where 0 is the LSB) in the most significant byte of the interrupt register can be set by the processor, and by writing and comparing bit patterns 5555H and AAAAH to each of the internal Adapter RAM locations (0580H to 07FEH).

Error Code	Meaning
1	Invalid read of the TMS38030 interrupt register
2	Invalid read of the TMS38030 internal RAM
10	ADS software was not downloaded

TEST 7 – ADS STAGE 2 DMA TEST

This test verifies the proper operation of the chip set DMA using commands inherent to the ADS EPROMs. The following stage 2 commands are used to exercise the DMA:

1 Clear DMA RAM
2 Fill DMA RAM
3 Test DMA to chip-set
4 Test DMA from chip-set

This test exercises the chip-set DMA by transferring the contents of the TRA on-board memory starting at address 10000H to the chip-set RAM (beginning at location 8000H) 4000H bytes at a time, then DMAs the 4000H bytes of data back to the TRA on-board memory at location 70000H for verification (70000H to 73FFFH is always the destination block used for comparing against the source block). If option memory is present, it is also tested (80000H to EFFFFH). This test skips the 20000H segment (20000H to 2FFFFH) since part of this memory is used for terminal I/O.

Error Code	Meaning
1	Clear DMA RAM test failed
2	Fill DMA RAM test failed
7	DMA to chip-set failure
8	DMA from chip-set failure
9	DMA verification failure
10	ADS software was not downloaded

TEST 8 – ADS STAGE 2 MISCELLANEOUS TESTS

This test uses commands inherent to the ADS EPROMs to exercise various miscellaneous parts of the chip-set. The following Stage 2 commands are used:

1 Set Interrupt Active
2 Test Expansion Memory (1000H-3FFEH, 8000H-FFFEH)
3 Test Wrap Function (loopback)

Error Code	Meaning
1	Could not activate chip-set interrupt
2	IPI4 not received from chip-set
3	Expansion memory test failed
4	Wrap function test failed
10	ADS Software was not downloaded

TEST 9 – ADS STAGE 2 EXTERNAL TESTS

This test runs diagnostics that require an external lobe media cable equipped with a self-shorting connector. These tests comprise a test of the watch dog time function implemented by the 74LS122 located between the TMS38020 and the ring interface, and a loopback test that causes frames to circulate on the lobe media cable.

Error Code	Meaning
1	Lobe function test failed (external loopback)
2	Watchdog timer test failed
10	ADS Software was not downloaded

NOTE: Tests 10 and 11 are not selected with the * specifier. They must be individually selected.

TEST 10 – INSERT FUNCTION TEST

This test activates the phantom drive of the ring interface to insert the PCB into a ring. The PCB must be connected to an external wiring concentrator through a lobe media cable.

Error Code	Meaning
1	Insert function test failed
10	ADS Software was not downloaded

TEST 11 – COMPREHENSIVE MEMORY TEST

This test may take 10 to 20 minutes to complete, depending on the amount of memory installed. This is a more rigorous memory test than Test 2. A memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written, it is checked for its initial value. This will identify if a memory write alters any word other than the intended one. This is done in both a forward and backward direction. The test is then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The main purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory error

ASYNCHRONOUS ADAPTER

TEST 1 – 80186 TRAP TEST

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the 512-Kbyte DRAM memory. The alternating word pattern 55AA AA55 is written to memory and verified. Then, the one's complement (AA55 55AA) is written and verified. The PROC PCB also verifies this memory from its side. The ASC processor must gain access to each 64-Kbyte segment by setting a bit in memory (called a semaphore) to signal the PROC to not attempt a memory access until the ASC processor has cleared the semaphore. There are eight semaphores for each of the eight 64-Kbyte memory segments. This test also verifies the parity generating circuitry by forcing bad parity on even and odd memory accesses and confirming that the proper response (NMI) is received.

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read
3	Memory error, byte write, word read
4	Memory error, byte write, byte read
5	NMI detected during memory test
6	Could not force parity error on even byte
7	Could not force parity error on odd byte

TEST 3 – 80186 INTERNAL DMA TEST

The 80186 built-in DMA feature is verified by this test. A block of memory is moved via DMA, and the two blocks of memory are compared.

Error Code	Meaning
1	DMA transfer not done in time
2	DMA move compare failed
3	Same as 1, starting on odd boundary
4	Same as 2, starting on odd boundary

TEST 4 – IPI TEST

This test verifies that the IPI bit in the FF register can be set and cleared directly, then verifies that INT3 was received. This test also checks for stray interrupts on INT0-INT2.

Error Code	Meaning
1	Cannot clear IPI bit in FF register
2	Cannot set IPI bit in FF register
3	INT3 not generated
4	INT0 also generated
5	INT1 also generated
6	INT2 also generated

TEST 5 – 8530 SCC INTERNAL LOOPBACK TEST

The 8530 SCC for each port is configured in asynchronous loopback mode at 19,200 baud to test the transmitter/receiver operation using single character I/O. Data values from 0 to 127 are used, with parity masked.

Error Code	Meaning
1	Character not received Byte 1: Port ID
2	Incorrect received character Byte 1: Port ID

TEST 6 – 8530 DMA LOOPBACK TEST

This test is similar to test 5, but uses the 80186 internal DMA as the receive leg of the loopback transfer.

Error Code	Meaning
3	DMA Transfer not completed Word 3: Port ID
2	Incorrect received character Word 3: Port ID

TEST 7 – 8530 SCC INTERRUPT TEST

The 8530 interrupt function to the 80186 processor of each of the ports is verified in this test. Transmit interrupts are enabled on the 8530 and a byte is written to the transmitter, causing simulation of the INT1 interrupt.

Error Code	Meaning
2	Stray interrupt detected Word 2: Port ID
3	INT1 not generated by XMIT int Word 2: Port ID
4	INT1 not generated by RCV int Word 2: Port ID
5	Overrun condition not detected Word 2: Port ID

NOTE: The remaining tests, tests 8, 9, and 10, can only be selected individually (not on default test list).

TEST 8 – COMPREHENSIVE MEMORY TEST

This test may take 10 to 20 minutes to complete, depending on the amount of memory installed. This is a more rigorous memory test than Test 2. A memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written, it is checked for its initial value. This will identify if a memory write alters any word other than the intended one. This is done in both a forward and backward direction. The test is then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The main purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory error

TEST 9 – 8530 SCC EXTERNAL LOOPBACK TEST

This test is similar to the internal loopback test, but an external loopback plug with the following connections is required for each port:

NOTE: Each of the following jumpers: JP1, JP3, JP5, JP7, JP9, JP11, JP13, and JP15 on the Asynchronous Adapter Connector Panel (for ports 0 though 7, respectively) must be set to positions 2-3 for each port being tested for RS 422-A configuration.

RS 232C:
Pin 6 jumpered to Pins 8 and 20
Pin 4 jumpered to Pin 5
Pin 3 jumpered to Pin 2

RS 422A:
Pin 12 jumpered to Pin 16
Pin 14 jumpered to Pin 19
Pin 7 jumpered to Pin 13
Pin 4 jumpered to Pins 5 and 6

Error Code	Meaning
1	Character not received Byte 1: Port that failed
2	Incorrect received character Byte 1: Port that failed
4	DCD not detected Byte 1: Port that failed
5	CTS not detected Byte 1: Port that failed
6	Stray data detected at other port's receiver

TEST 10 – 8530 SCC EXTERNAL LOOPBACK TEST, PORT SELECTABLE

This test is the same as test 9, but tests a single port instead, as selected by the user. When this test is selected, the following prompt appears on the screen: "Enter ASYNC Port to test (0-7):". The user then selects the desired port to test.

Error Code	Meaning
1	Character not received Byte 1: Port that failed
2	Incorrect received character Byte 1: Port that failed
4	DCD not detected Byte 1: Port that failed
5	CTS not detected Byte 1: Port that failed