Chapter 4

Diagnostic Tests – Models 1L/1R/2R/3R

DIAGNOSTIC TESTS – MODELS 1L/1R/2R/3R

PROCESSOR

TEST 1 - PROCESSOR TRAP TEST

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the DRAM memory, including segments A, B, C, and D (configured as on-board DRAM) as well as the Device Image Buffer (DIB) memory accessible through the E8000 segment. When testing DIB memory, the verification is through the E0000 segment (by setting up mapping RAM location 6). The alternating word pattern 55AA AA55 is written to memory and verified, then the 1s complement pattern AA55 55AA is written and verified so that each bit position is tested. If the processor is an 80386, the parity generation circuitry is also verified (error codes 7 through 10).

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read
3	Memory error, byte write, word read
4	Memory error, byte write, byte read
5	NMI detected during memory test
6	Memory error, double word write, double word read (80386 processor only)
7	Could not force byte 0 parity error (80386)
8	Could not force parity error on byte 1 (80386)
9	Could not force parity error on byte 2 (80386)
10	Could not force parity error on byte 3 (80386)

TEST 3 – 8255 PROGRAMMABLE PERIPHERAL INTERFACE TEST

This test verifies Port C on the 8255 PPI chip by writing and reading the bit patterns 55H and AAH.

Error Code	Meaning
1	PPI Port C value incorrect

TEST 4 – MULTIBUS MEMORY TEST

This test checks access to Multibus memory. Multibus memory on all smart IOCs and on the SSP is tested. An 8 Kbyte block of memory is copied from the power-up EPROMs to Multibus memory by first using a Repeat Move Byte String operation and verifying the transfer using (1) byte reads, (2) word reads, and (3) a Repeat Compare String operation. A Repeat Move Word String operation is then performed and the data is verified in the same fashion. Access to multibus memory is done through the 'D' segment by setting up the mapping RAM accordingly.

The SSP will verify the 'D' segment on its own board and will test the 2nd shared RAM bank on each of the IOCs (i.e. if an IOCs shared RAM starts at 80000H, then the test will verify 90000H-92000H on that board).

Error Code	Meaning
1	Byte write, byte read comparison failed Byte 1: Slot number of board
2	Byte write, word read comparison failed Byte 1: Slot number of board
3	Byte write, byte string comparison failed Byte 1: Slot number of board
4	Word write, byte read comparison failed Byte 1: Slot number of board
5	Word write, word read comparison failed Byte 1: Slot number of board
6	Word write, byte string comparison failed Byte 1: Slot number of board
7	NMI detected during test
10	Could not gain access to system memory Word 1: Slot number of board

TEST 5 – IPI TEST

The IPI test first verifies that the IPI bit in the FF register can be set and cleared directly. The test verifies that the interrupt was received at the Master PIC and no stray interrupts occurred.

Error Code	Meaning
1	Cannot clear IPI bit in FF register
2	Cannot set IPI bit in FF register
3	IPI bit not set by I/O write
4	FF-IPI interrupt not received
5	Stray interrupt detected
6	IPI Interrupt did not go away
7	Could not set NMI in FF register
8	NMI interrupt to processor not received
9	PIT interrupt not being received
11	Incorrect PUSH of flags during interrupt

TEST 6 – ADMA BLOCK MOVE TEST

This test verifies the memory move operation for each channel of the 82257 ADMA. The test exercises data transfers from the start of EPROM (FB00:0) to local memory (8000:0), system memory (B000:0), and DIB memory (E000:0, page 0) using a 4 Kbyte block of the EPROM as test data. The first 4 Kbytes of EPROM is then compared to the block at 8000:0, B000:0, and E000:0.

Error Code	Meaning
1	ADMA Premature termination
2	ADMA fatal error detected
3	ADMA hung up (transfer not completed)
4	ADMA move compare failed
5	ADMA interrupt not received
6	ADMA move compare failed (local side)
7	ADMA move failure from system to local memory

NOTE: Tests 7-10 are not selected with the * specifier. They must be individually selected.

TEST 7 – COMPREHENSIVE MEMORY TEST

This test may take from 10 to 20 minutes to complete, depending on the amount of memory installed. More rigorous than Test 2, a memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written, it is checked for its initial value. This will identify if a memory write alters any word other than the intended one. This is done in both a forward and backward direction. The test is then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The main purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory error

TEST 8 – 8530 SCC INTERNAL LOOPBACK TEST

The maintenance port SCC is configured in asynchronous, loopback mode at 9600 baud to test the transmitter/receiver operation using single character I/O. Data values from 0 to 127 are used, with parity masked. A coax type terminal must be used to run this test since this port is the access port for ASCII terminals.

Error Code	Meaning
1	Character not received
2	Incorrect received character

TEST 9 – LOCK TEST

NOTE: This test cannot be run in conjunction with any other diagnostic tests. Failure to observe this precaution may cause the control unit to enter a state from which it cannot be recovered except by re-IMLing the system.

This test verifies proper operation of the Lock signal for each of the appropriate processors in the system (PROC, all IOCs, and the HCA). PROC tests its Lock operation versus each IOC in the system by incrementing a specific 16-bit word in shared memory (initialized to 0) while the IOC concurrently decrements the same word from its side. A failure is indicated if both sides are finished and the count is not zero. If the count is less than zero, the PROC lock mechanism is likely failing, and if the count is less than zero, the remote IOC is likely failing. PROC tests itself against each IOC in the system under four different scenarios: test word located in PROC memory, PROC local access, test word in PROC memory, system bus access, test word in remote IOCs shared memory, IOC local access, and test word in remote IOCs shared memory, IOC system bus access.

Error Code	Meaning
1	Lock failure, PROC side, PROC local access Word 1: slot of board being tested with PROC
2	Lock failure, PROC side, PROC system access Word 1: slot of board being tested with PROC
3	Lock failure, remote board side, local access Word 1: slot of board being tested with PROC
4	Lock failure, local board side, system access Word 1: slot of board being tested with PROC
5	Could not communicate with remote board Word 1: slot of board that did not respond
6	Lock failure, other IOCs memory (MCA Only) Word 1: slot of target IOC

TEST 10 – DISK DRIVE TEST

This test exercises the user specified disk drive in the control unit. This test takes about ten minutes to complete for each disk being tested. This test first formats the diskette and verifies each sector during the formatting process. The test then verifies that it can successfully write and read the first track and then writes and reads the last track on the disk.

NOTE: When selecting this test, a blank or scratch diskette should be installed in the diskette drive as this test destroys any data that may be contained on the diskette.

Error Code	Meaning
1	Seek error
2	Format error or disk not ready
3	Verify error while formatting
4	Cannot write track 79
5	Cannot write track 0
6	Cannot read track 79
7	Cannot read track 0
	Data miscompare, track 79
9	Data miscompare, track 0
10	General disk failure
11	Recalibration failure after format

COAX ADAPTER

TEST 1 – 8051 POWER-UP VERIFICATION

This test checks the status report returned by the 8051 at power-up regarding its own power-up self diagnostics. If any "soft" errors occurred when the 8051 went through its power-up sequence, they will be reported by this test. This test also reports any detectable problems when downloading code to the 8051. (This test is a status report and never runs any actual diagnostic tests).

Error Code	Meaning
1	8051 stack test failed
2	8051 internal RAM test failed
3	8051 internal RAM addressing test failed
4	8051 PROM checksum test failed
5	8051 register switching test failed
6	8051 external RAM test failed
7	8051 external RAM addressing test failed
8	8051 internal timer test failed
9	8051 did not send initialization code
10	8051 did not accept download command

TEST 2 – COAX LOOPBACK TEST

The loopback test will verify the coax transmitter and receiver hardware using the byte patterns 55H and AAH as the test data. The Data Available, RCVR.TT/AR, RCVR.D10, and RCVR.D11 signals will also be verified in this test.

Error Code	Meaning
1	Error detected by 8341 during loopback Byte 2: port number (0-1FH)
2	Data Available not received from 8341 Byte 2: port number (0-1FH)
3	Received data incorrect Byte 2: port number (0-1FH)
4	Coax receiver data bit D11 invalid
5	RCVR.TT/AR signal invalid
6	Coax receiver parity bit D10 invalid
7	No response from 8051 regarding test

TEST 3 – MEMORY TEST

An alternating word pattern 55AA AA55 is written to the CAs Dual Access Memory (DAM) and verified, then the 1s complement pattern AA55 55AA is written and verified so that each bit position is tested. The DAM is tested from offset 1000H to 1FFFH.

Error Code	Meaning
1	Memory test failed, word read
2	Memory test failed, byte read
3	NMI detected during memory test

TEST 4 – BUS ARBITRATION MEMORY TEST

This test runs the above memory test while the 8051 runs a memory test in a different part of the DAM. This will verify that dual accesses can occur at the same time in different parts of the memory. The 8051 runs its memory test in the DAM at offset 2000H to 20FFH. The test writes a pattern of 55H to the 256-byte block and verifies the data, then the pattern AAH is tested.

Error Code	Meaning
1	Memory test failed, word read, processor side
2	Memory test failed, byte read, processor side
3	NMI detected during memory test, processor side
4	Memory test failed, 8051 side
7	No response from 8051 regarding test

TEST 5 – COAX INTERRUPT TEST

This test causes the 8051 to strobe an interrupt signal (IPI-0) and verifies that the interrupt was received at the IPI slave PIC on the main processor.

Error Code	Meaning
1	Interrupt (IPI-0) not received
2	Interrupt (IPI-0) does not go away
7	No response from 8051 regarding test

ASYNCHRONOUS ADAPTER

TEST 1 – 80186 TRAP TEST

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the DRAM memory. The alternating word pattern 55AA AA55 is written to memory and verified, then the 1s complement pattern AA55 55AA is written and verified so that each bit position is tested. A 16-bit checksum is then computed over the 8K words of EPROM memory.

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read
3	Memory error, byte write, word read
4	Memory error, byte write, byte read
5	NMI detected during memory test
6	EPROM checksum test failed

TEST 3 – 80186 INTERNAL DMA TEST

The 80186 built-in DMA feature is verified by this test. A block of memory is moved via DMA, and the two blocks of memory are compared.

Error Code	Meaning
1	DMA transfer not done in time
2	DMA move compare failed
3	Same as 1, starting on odd boundary
4	Same as 2, starting on odd boundary

TEST 4 – SYSTEM BUS MEMORY TEST

This test checks access to Multibus memory. It exercises system bus memory on the SSP as well as any other IOCs in the product, including itself. An 8 Kbyte block of memory is copied from the power-up EPROMs to Multibus memory by first using a Repeat Move Byte String operation and verifying the transfer, then a Repeat Move Word String operation is performed and the data is verified. The move is first compared by byte reads, then word reads, and finally a Repeat Compare String comparison. The chunk of memory tested by the ASYNC board on the SSP and any IOCs depends on the order in which the board appears in the product. The SSP always tests the first 8K, then the next IOC found in the product (by order of slot #) will test the next 8K, and the next IOC will test the next 8K etc. (i.e., if a product contains an SSP in slot 0, an ASYNC IOC in slot 4, and an ENC IOC in slot 5, the SSP will test system memory at x0000-x1FFF, the ASYNC IOC tests x2000-x3FFF, and the ENC IOC tests x4000-x5FFF).

Error Code	Meaning
1	Byte write, byte read comparison failed
2	Byte write, word read comparison failed Byte 1: Slot number of board
3	Byte write, byte string comparison failed Byte 1: Slot number of board
4	Word write, byte read comparison failed Byte 1: Slot number of board
5	Word write, word read comparison failed Byte 1: Slot number of board
6	Word write, byte string comparison failed Byte 1: Slot number of board
7	NMI detected during test
10	Could not gain access to system memory Word 1: Slot number of board accessed

TEST 5 – IPI TEST

The IPI test first verifies that the IPI bit in the FF register can be set and cleared directly. The test will then verify that the interrupt was received at the Master PIC and no stray interrupts occurred.

Error Code	Meaning
1	Cannot clear IPI bit in FF register
2	Cannot set IPI bit in FF register
3	IPI bit not set by I/O write
4	"BUSY" status bit not set with IPI bit
5	INT3 not generated
6	INT0 also generated
7	INT1 also generated
8	INT2 also generated

TEST 6 – 8530 SCC INTERNAL LOOPBACK TEST

The 8530 SCC for each port is configured in asynchronous, loopback mode at 9600 baud to test the transmitter/receiver operation using single character I/O. Data values from 0 to 127 are used, with parity masked.

Error Code	Meaning
1	Character not received Byte 1: port ID (0-7)
2	Incorrect received character Byte 1: port ID (0-7)

TEST 7 – 8530 DMA LOOPBACK TEST

This test configures the 8530 SCC for each port to operate in synchronous (SDLC) loopback mode and uses the internal 80186 DMA on the receive leg of the transfers. Variable frame lengths are tested by first sending a 1-byte I-field, then a 2-byte field, etc. up to a 100-byte field. The bytes in each I-field will be sent in a "counting" format starting with 1 (i.e., 01 will be sent, then 0102, then 010203 etc.). End of frame and CRC are also verified for each iteration. The transmit buffer is at 60000H and the receive buffer is at 70000H.

Error Code	Meaning
3	DMA transfer not completed Word 3: Port ID (0-7)
2	Incorrect received character Word 3: Port ID (0-7)

TEST 8 – 8530 SCC INTERRUPT TEST

The 8530 interrupt function to the 80186 processor of each of the ports is verified in this test. Transmit interrupts are enabled on the 8530 and a byte is written to the transmitter, causing simulation of the interrupt.

Error Code	Meaning
2	Extra interrupt detected Word 2: Port ID (0-7)
3	INT1 not generated by XMIT int Word 2: Port ID (0-7)
4	INT1 not generated by RCV int Word 2: Port ID (0-7)
5	Overrun condition not detected Word 2: Port ID (0-7)

NOTE: Tests 9 through 11 are not accessed with the * specifier, and must be individually selected.

TEST 9 – COMPREHENSIVE MEMORY TEST

This test may take from 10 to 20 minutes to complete, depending on the amount of memory installed. This is a more rigorous memory test than Test 2. A memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written, it is checked for its initial value. This will identify if a memory write alters any word other than the intended one. This is done in both a forward and backward direction. The test is then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The main purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory error

TEST 10 – 8530 SCC EXTERNAL LOOPBACK TEST

This test is similar to the internal loopback test, but requires an external connection to each port for the loopback. This test also verifies the RTS, CTS, and DCD signals. The external connector for each port should have the following connections:

DTR(12) jumpered to DSR(6)
RTS(4) jumpered to CTS(5)
RxD(3) jumpered to TxD(2)

Error Code	Meaning
1	Character not received Byte 1: Port that failed (0-7)
2	Incorrect received character Byte 1: Port that failed (0-7)
4	DCD not detected Byte 1: Port that failed (0-7)
5	CTS not detected Byte 1: Port that failed (0-7)
6	Stray data detected at other port's receiver Word 1: Port that had stray data

TEST 11 – 8530 SCC EXTERNAL LOOPBACK TEST, PORT SELECTABLE

This test is the same as test 10, but tests a single port instead, depending on which port the user selects for testing. After selecting this test, the following question appears: "Enter ASYNC Port to test (0-7): ". The user could then enter the desired port to run the loopback test.

Error Code	Meaning
1	Character not received Byte 1: port that failed (0-7)
2	Incorrect received character Byte 1: port that failed (0-7)
4	DCD not detected Byte 1: port that failed (0-7)
5	CTS not detected Byte 1: port that failed (0-7)

CHANNEL ADAPTER

TEST 1 – 29116 REGISTER TEST

This test checks the internal registers of the 29116. All registers except R15 are tested. R15 is used to hold the error code and therefore cannot be tested. An error is indicated when the expected data (AAAAH) does not equal the received data.

Error Code	Meaning
1	29116 register test failure
2	ul parity Error
10	Cannot communicate with HCA board

TEST 2 – LOCAL STORE MEMORY TEST

This test verifies the Local Store Memory. It first writes the address to each location and verifies that it was written, then the memory is cleared and a marching 1 pattern is used to exercise the memory.

Error Code	Meaning
2	Local store address test failure
3	Local store data test failure
9	DRAM parity error detected
10	Cannot communicate with HCA board

TEST 3 – SHARED MEMORY TEST (HCA, BIT SLICE POCESSOR SIDE)

This test verifies the Shared Memory. The test first writes the address to each location and verifies that it was written, then the memory is cleared and a marching 1 pattern is used to exercise the memory.

Error Code	Meaning
4	Shared memory address test failure (HCA side)
5	Shared memory data test failure (HCA side)
9	DRAM parity error detected
10	Cannot communicate with HCA board

TEST 4 – CHANNEL ADDRESS RAM TEST

This test checks the Channel Address RAM. The RAM is filled with ones and verified, then all odd addresses are written with zeros and each location is verified. All even addresses are then written with zeros and each location is checked for zeros.

Error Code	Meaning
6	Channel address RAM test
10	Cannot communicate with HCA board

TEST 5 – SHARED MEMORY TEST (SYSTEM PROCESSOR SIDE)

This test verifies the shared memory on the HCA from the processor side (CPU7 or MP2). An alternating pattern of 55AA AA55 is used to test the memory from 00000H to 6FFFFH using segment 'C' as the access window through the mapping RAM. The 1s complement pattern AA55 55AA is then tested through the memory. The test then does an address check, one segment at a time, by writing the offset to each location in the segment and verifying the result (verifies address bits 0-15).

Error Code	Meaning
1	Memory error, word write, word read (PROC side)
2	Memory error, word write, byte read (PROC side)
3	Memory error, byte write, word read (PROC side)
4	Memory error, byte write, byte read (PROC side)
5	NMI detected during memory test
9	Address Failure

TEST 6 – SHARED MEMORY ARBITRATION TEST

This test exercises the bus arbitration of the shared memory between the system processor and the bit slice processor on the HCA. The system processor runs its memory test (test 5) on the lower segment, 00000H to 0FFFFH, while the bit slice processor concurrently runs its shared memory test (test 3) from 10000H to 6FFFFH.

Error Code	Meaning
1	Memory test failed, word read (MP2 side)
2	Memory test failed, byte read (MP2 side)
3	NMI detected during memory test
4	Memory test failed, HCA side
9	DRAM parity error detected
10	Cannot communicate with HCA board

TEST 7 – CHANNEL ADAPTER INTERRUPT TEST

The Channel Adapter is told to simulate an interrupt and the interrupt is verified at the system processor through the Master PIC on system processor board.

Error Code	Meaning
1	Interrupt not received
2	Interrupt does not go away
10	Cannot communicate with HCA board

TEST 8 – WRITABLE CONTROL STORE (WCS) TEST

This test verifies the Writable Control Store (WCS) function of the HCA. 8 Kbytes of the data pattern 5555 AAAA 5555 starting at 30000H is downloaded to the HCA and verified. This test should only be run if there was a problem at start up time in downloading the channel code. Running this test overwrites any previously downloaded code and thus the other diagnostic tests could not be run.

Error Code	Meaning
1	HCA download failure

HOST SERIAL INTERFACE

TEST 1 – 8530 SCC INTERNAL LOOPBACK TEST

The 8530 SCC chip on the HSI PCB is configured in asynchronous, loopback mode at 9600 baud to test the transmitter/receiver operation using single character I/O. Data values from 0 to 127 are used, with parity masked. If the Host Serial Interface Expander (HSIE) is present, Port B of the SCC chip is also tested. In the following error descriptions, the ports indicate ports on the chip.

Error Code	Meaning
1	Character not received Word 3: 0X0A = Port A, 0X0B = Port B
2	Incorrect received character Word 3: 0X0A = Port A, 0X0B = Port B

TEST 2 – 8530 DMA LOOPBACK TEST

This test configures the 8530 SCC chip to operate in synchronous (SDLC) loopback mode and uses the utility processor 82257 baby ADMA for transfers. Variable frame lengths are tested by first sending a 1-byte I-field, then a 2-byte field, etc. up to a 100-byte field. The bytes in each I-field will be sent in a "counting" format starting with 1 (i.e., 01 will be sent, then 0102, then 010203 etc.). End of frame and CRC are also verified for each iteration. The transmit buffer is at 60000H and the receive buffer is at 70000H. If the Host Serial Interface Expander (HSIE) is present, Port B of the SCC chip is also tested. In the following error descriptions, the ports indicate ports on the chip.

Error Code	Meaning
1	ADMA premature termination Word 3: 0X0A = Port A, 0X0B = Port B
2	ADMA fatal error detected Word 3: 0X0A = Port A, 0X0B = Port B
3	ADMA hung up (transfer not completed) Word 3: 0X0A = Port A, 0X0B = Port B
5	CRC error detected in frame Word 3: 0X0A = Port A, 0X0B = Port B
6	Incorrect received character Word 3: 0X0A = Port A, 0X0B = Port B
8	Premature underrun
9	End of frame never received Word 3: 0X0A = Port A, 0X0B = Port B
10	Failure in half-duplex configuration Word 3: 0X0A = Port A, 0X0B = Port B

TEST 3 – 8530 INTERRUPT TEST

This test simulates an interrupt from the 8530 and verifies that the interrupt gets received at the Master PIC on the SSP. In the following error descriptions, ports indicate ports on the chip.

Error Code	Meaning
1	Interrupt not received at Master PIC Word 3: 0X0A = Port A, 0X0B = Port B
2	Interrupt does not go away Word 3: 0X0A = Port A, 0X0B = Port B

TEST 4 – 8530 SCC EXTERNAL LOOPBACK TEST

This test is similar to the internal loopback test, but requires an external connection to the host port (HOST1) for the loopback. This test also verifies the RTS, CTS, and DCD signals. In the error descriptions, ports indicate ports on the chip. The external connector should have the following connections:

RS 232C:
DTR(20) jumpered to DCD(8) and DSR(6)
RTS(4) jumpered to CTS(5)
RxD(3) jumpered to TxD(2)

V.35:
DTR(20) jumpered to DCD(8) and DSR(6)
CDID6(14) jumpered to GND(7)
XMTDAT A-(10) jumpered to RCVDAT A-(12)
RCVDAT B+(13) jumpered to XMTDAT B+(9)
Pin 4 jumpered to pin 5

X.21:
T-A(2) jumpered to R-A(4)
C-A(3) jumpered to I-A(5)
T-B(9) jumpered to R-B(11)
C-B(10) jumpered to I-B(12)

Error Code	Meaning
1	Character not received Word 3: 0X0A = Port A, 0X0B = Port B
2	Incorrect received character Word 3: 0X0A = Port A, 0X0B = Port B
4	DCD not detected Word 3: 0X0A = Port A, 0X0B = Port B
5	CTS not detected Word 3: 0X0A = Port A, 0X0B = Port B

TOKEN-RING GATEWAY

NOTE: The cable between the control unit and the Token Ring must be disconnected prior to running the Token-Ring Gateway diagnostic tests. This cable must be disconnected at the Token Ring and remain connected to the control unit. Diagnostic tests may have adverse effects on the Token Ring if the control unit is attached.

TEST 1 – 80286 TRAP TEST

The trap vectors for interrupt types 4 through 40 are set with unique values. The interrupt handler for each type writes the interrupt type to a word in memory. In this test, each interrupt type is forced to occur using the INT instruction, and the word in memory is examined for the proper interrupt type value.

Error Code	Meaning
1	Incorrect trap taken

TEST 2 – MEMORY TEST

This test verifies the integrity of the 512-Kbyte DRAM memory as well as the Frame Image Buffer (FIB) memory accessible through the B0000 and E0000 segments (implemented with up to 8.0 Mbyte memory expansion PCBs). The alternating word pattern 55AA AA55 is written to memory and verified. Then the one's complement pattern AA55 55AA is written and tested. The FIB memory is written using E0000 as access, and read using B0000 as access. This test also verifies the parity generation by forcing an incorrect parity at 3000:0 and 3000:3 and confirming the result by reading the NMI status.

Error Code	Meaning
1	Memory error, word write, word read
2	Memory error, word write, byte read
3	Memory error, byte write, word read
4	Memory error, byte write, byte read
5	NMI detected during memory test
6	Could not force parity on even byte
7	Could not force parity on odd byte

TEST 3 – MAPPING RAM TEST

This test verifies the mapping RAM registers B through E by writing and verifying the test patterns 0 through FF, as well as a rotating 1s pattern.

Error Code	Meaning
1	Invalid read of mapping RAM

TEST 4 – MULTIBUS MEMORY TEST

This test checks access to Multibus memory on all relevant IOCs and on the SSP. An 8-Kbyte block of memory is copied from the power-up EPROMs to Multibus memory by first using a "Repeat Move Byte String" operation and verifying the transfer using (1) byte reads, (2) word reads, and (3) a "Repeat Compare String" operation. A "Repeat Move Word String" operation is then performed and the data is verified in the same fashion. Access to multibus memory is done through the "D" segment by setting up the mapping RAM accordingly. The TRC will verify the "D" segment on the PROC board and will test the second RAM bank on each of the IOCs (i.e., if an IOCs shared RAM starts at 80000H, then the test verifies 90000H-92000H on that board). The TRC does not have system memory resident on its' board.

Error Code	Meaning
1	Byte write, byte read comparison failed
2	Byte write, word read comparison failed
3	Byte write, byte string comparison failed
4	Word write, byte read comparison failed
5	Word write, word read comparison failed
6	Word write, byte string comparison failed
7	NMI detected during test
10	Could not gain access to system memory

TEST 5 – IPI TEST

The IPI test first verifies that the IPI bit in the FF register can be set and cleared directly. The test then verifies that the interrupt was received at the Master PIC, and that no stray interrupts occurred.

Error Code	Meaning
1	Cannot clear IPI bit in FF register
2	Cannot set IPI bit in FF register
3	IPI bit not set by I/O write
4	FF-IPI interrupt not received
5	Stray interrupt detected Word 1: Contents of Master PIC IRR
6	FF-IPI interrupt did not go away

TEST 6 – BRING-UP DIAGNOSTIC TEST

This test checks a status byte generated at power-up time that indicates the initial state of the Token-Ring chip-set. The Token-Ring chip-set goes through four phases at power-up time:

1 Bring-up diagnostics
2 Chip-set initialization and expansion memory verification using the Open command
3 Adapter Debug Software (ADS) download to the Token-Ring expansion memory
4 ADS stage 1 Lan Adapter bus verification

The bring-up diagnostic performs the following chip-set tests:

1 Test of the TMS38020 ROM
2 Instruction and interrupt test of the TMS38010
3 Transmit wrap test through the ring interface (loopback)
4 Register access test of the TMS 38030

The ADS Stage 1 diagnostic exercises the Token-Ring chip-set by going through five verification phases:

1 Reset Verification – verifies that the TMS38030 Communications Processor and on-chip oscillator are functional and that basic access to the ADS EPROM is successful
2 EPROM checksum verification – verifies that the ADS EPROMs and the LAN Adapter bus interface to the ADS EPROMs is fully functional
3 TMS38010 RAM verification – verifies that the RAM contained in the TMS38010 Communications Processor is fully functional
4 TMS38020 Protocol Handler register verification – verifies that the TMS38010 Communications Processor can read and write selected registers of the TMS38020 Protocol Handler
5 TMS38030 System Interface register verification – verifies that the TMS38010 can read and write selected registers of the TMS38030 System Interface

Error Code	Meaning
1	Bring-up diagnostics failed (chip-set failure)
2	Bring-up diagnostics hung
3	Token-Ring Adapter will not initialize
4	Token-Ring Adapter will not Open
5	Failure detected during Token Ring Open
6	Token Ring will not enter download state
7	Data miscompare in code download verification
8	ADS Stage 1 bus verification failure
9	Burned-in EPROM address invalid
10	Cannot read burned-in address

TEST 7 – DIRECT I/O INTERFACE TESTS

This test exercises the direct I/O interface to the chip-set by verifying that bits 0-6 (where 0 is the LSB) in the most significant byte of the interrupt register can be set by the processor, and by writing and comparing bit patterns 5555H and AAAAH to each of the internal chip-set RAM locations (0580H to 07FEH).

Error Code	Meaning
1	Invalid read of the TMS38030 interrupt register
2	Invalid read of the TMS38030 internal RAM
10	ADS software was not downloaded

TEST 8 – ADS STAGE 2 DMA TEST

This test verifies the proper operation of the chip set DMA using commands inherent to the ADS EPROMs. The following stage 2 commands are used to exercise the DMA:

1 Clear DMA RAM
2 Fill DMA RAM
3 Test DMA to chip-set
4 Test DMA from chip-set

The test exercises the DMA by transferring the TRCs FIB memory starting at FIB offset 00000 to the chip-set RAM (starting at location 8000H) 4000H bytes at a time, then DMAs the data back to the FIBs memory at location E0000H (FIB bank 0, page 0) for verification.

Error Code	Meaning
1	Clear DMA RAM test failed
2	Fill DMA RAM test failed
7	DMA to chip-set failure
8	DMA from chip-set failure
9	DMA verification failure
10	ADS software was not downloaded

TEST 9 – ADS STAGE 2 MISCELLANEOUS TESTS

This test uses commands inherent to the ADS EPROMs to exercise various miscellaneous parts of the chip-set. The following Stage 2 commands are used:

1 Set Interrupt Active
2 Test Expansion Memory (1000H-3FFEH, 8000H-FFFEH)
3 Test Wrap Function (loopback)

Error Code	Meaning
1	Could not activate chip-set interrupt
2	IPI4 not received from chip-set
3	Expansion memory test failed
4	Wrap function test failed
10	ADS Software was not downloaded

TEST 10 – ADS STAGE 2 EXTERNAL TESTS

This test runs diagnostics that require an external lobe media cable equipped with a self-shorting connector. These tests are comprised of a test of the watch dog time function implemented by the 74LS122 located between the TMS38020 and the ring interface, and a loopback test that causes frames to circulate on the lobe media cable.

Error Code	Meaning
1	Lobe function test failed (external loopback)
2	Watchdog timer test failed
10	ADS Software was not downloaded

NOTE: Tests 11 and 12 are not selected with the * specifier. They must be individually selected.

TEST 11 – INSERT FUNCTION TEST

This test activates the phantom drive of the ring interface to insert the PCB into a ring. The PCB must be connected to an external wiring concentrator through a lobe media cable.

Error Code	Meaning
1	Insert function test failed
10	ADS Software was not downloaded

TEST 12 – COMPREHENSIVE MEMORY TEST

This test may take from 10 to 20 minutes to complete, depending on the amount of memory instaled. This is a more rigorous memory test than test 2. A memory segment is initialized to all 0s, and a diagonal pattern of 1s is written. Before each word is written it is checked for its initial value. This identifies if a memory write alters any word other than the intended one. This is done in both forward and backward directions. The test its then repeated with memory initialized to all 1s using a diagonal pattern of marching 0s. The purpose of this test is to verify that no memory operation sets or clears a bit in any other memory word.

Error Code	Meaning
1	Memory Error

TOKEN-RING ADAPTER

NOTE: The cable between the control unit and the Token Ring must be disconnected prior to running the Token-Ring Adapter diagnostic tests. This cable must be disconnected at the Token Ring and remain connected to the control unit. Diagnostic tests may have adverse effects on the Token Ring if the control unit is attached.

TEST 1 – MEMORY TEST

This test verifies the integrity of the 64-Kbyte SRAM memory. The alternating word pattern 55AA AA55 is written to memory and verified, then the 1s complement pattern AA55 55AA is written and verified so that each bit position is tested. The parity generating circuitry is also verified by forcing bad parity at 0:0 (even byte) and 0:3 (odd byte). The TRA interrupt is verified at the IPI PIC on the PROC PCB.

Error Code	Meaning
1	Memory error – word write, word read
2	Memory error – word write byte read
3	Memory error – byte write, word read
4	Memory error – byte write, byte read
5	Bad parity detected during memory test
6	Could not force parity on even byte
7	Could not force parity on odd byte
8	Parity interrupt not received at PIC on PROC
9	Address Failure

TEST 2 – BRING-UP DIAGNOSTIC TEST

This test checks a status byte generated at power-up time that indicates the initial state of the Token-Ring chip-set. The Token-Ring chip-set goes through four phases at power-up time:

1 Bring-up diagnostics
2 Chip-set initialization and expansion memory verification using the Open command
3 Adapter Debug Software (ADS) download to the Token-Ring expansion memory
4 ADS stage 1 LAN Adapter bus verification

The bring-up diagnostic performs the following chip-set tests:

1 Test of the TMS38020 ROM
2 Instruction and interrupt test of the TMS38010
3 Transmit wrap test through the ring interface (loopback)
4 Register access test of the TMS 38030

The ADS Stage 1 diagnostic exercises the Token-Ring chip-set by going through five verification phases:

1 Reset Verification – verifies that the TMS38030 Communications Processor and on-chip oscillator are functional and that basic access to the ADS EPROM is successful
2 EPROM checksum verification – verifies that the ADS EPROMs and the LAN Adapter bus interface to the ADS EPROMs is fully functional
3 TMS38010 RAM verification – verifies that the RAM contained in the TMS38010 Communications Processor is fully functional

4 TMS38020 Protocol Handler register verification – verifies that the TMS38010 Communications Processor can read and write selected registers of the TMS38020 Protocol Handler
5 TMS38030 System Interface register verification – verifies that the TMS38010 can read and write selected registers of the TMS38030 System Interface

Error Code	Meaning
1	Bring-up diagnostics failed (chip-set failure)
2	Bring-up diagnostics hung
3	Token-Ring Adapter will not initialize
4	Token-Ring Adapter will not open
5	Failure detected during Token Ring Open
6	Token Ring will not enter download state
7	Data miscompare in code download verification
8	ADS Stage 1 bus verification failure
9	Burned-in EPROM address invalid
10	Cannot read burned-in address

TEST 3 – DIRECT I/O INTERFACE TESTS

This test exercises the direct I/O interface to the chip-set by verifying that bits 0-6 (where 0 is the LSB) in the most significant byte of the interrupt register can be set by the processor, and by writing and comparing bit patterns 5555H and AAAAH to each of the internal Adapter RAM locations (0580H to 07FEH).

Error Code	Meaning
1	Invalid read of the TMS38030 interrupt register
2	Invalid read of the TMS38030 internal RAM
10	ADS software was not downloaded

TEST 4 – ADS STAGE 2 DMA TEST

This test verifies the proper operation of the chip set DMA using commands inherent to the ADS EPROMs. The following stage 2 commands are used to exercise the DMA:

1 Clear DMA RAM
2 Fill DMA RAM
3 Test DMA to chip-set
4 Test DMA from chip-set

After verifying the Clear and Fill functions of the Chip-set DMA, the multiple access to the DRAM is verified by performing a DMA from memory to the adapter while concurrently accessing DID and also exercising a separate section of memory. The test then exercises the Chip-set DMA by transferring the contents of the TRA memory from 0 to 7FFFH to the Chip-set RAM (starting at RAM location 1000H) 4000H bytes at a time, verifying the transfer each time by DMAing the 4000H data back to location 0:0 and comparing the two memory blocks.

Error Code	Meaning
1	Clear DMA RAM test failed
2	Fill DMA RAM test failed
3	Direct I/O failed during concurrent DMA
4	Memory failed during concurrent DMA
5	DMA hung during concurrent DIO, memory test
6	DMA failed during concurrent DIO, memory test
7	DMA to chip-set failure
8	DMA from chip-set failure
9	DMA verification failure
10	ADS software was not downloaded
11	Parity error detected during test

TEST 5 – ADS STAGE 2 MISCELLANEOUS TESTS

This test uses commands inherent to the ADS EPROMs to exercise various miscellaneous parts of the chip-set. The following Stage 2 commands are used:

1 Set Interrupt Active
2 Test Expansion Memory (1000H-3FFEH, 8000H-FFFEH)
3 Test Wrap Function (loopback)

Error Code	Meaning
1	Could not activate chip-set interrupt
2	Interrupt not received from chip-set
3	Expansion memory test failed
4	Wrap function test failed
10	ADS Software was not downloaded

TEST 6 – ADS STAGE 2 EXTERNAL TESTS

This test runs diagnostics that require an external lobe media cable equipped with a self-shorting connector. These tests are comprised of a test of the watch dog time function implemented by the 74LS122 located between the TMS38020 and the ring interface, and a loopback test that causes frames to circulate on the lobe media cable.

Error Code	Meaning
1	Lobe function test failed (external loopback)
2	Watchdog timer test failed
10	ADS Software was not downloaded

NOTE: Test 7 is not selected with the * specifier. It must be individually selected.

TEST 7 – INSERT FUNCTION TEST

This test activates the phantom drive of the ring interface to insert the PCB into a ring. The PCB must be connected to an external wiring con centrator through a lobe media cable.

Error Code	Meaning
1	Insert function test failed
10	ADS Software was not downloaded